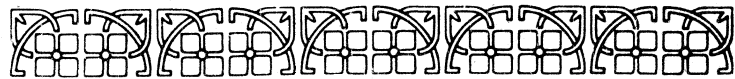
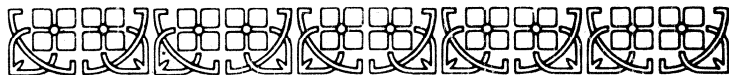


MOTOROLA Semiconductor Products Inc.



LINEAR

INTEGRATED CIRCUITS DATA BOOK



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LINEAR INTEGRATED CIRCUITS DATA BOOK

Linear Integrated Circuits have achieved a level of maturity which now rivals that of their digital counterparts. In all market categories and for a wide variety of applications functions, linear ICs are serving the needs of equipment manufacturers to reduce cost and improve equipment form, factor and reliability.

They've matured, too, from the standpoint of availability. The number of off-the-shelf linear circuits and their varying capabilities makes them highly useful as building blocks for system design. Moreover, the now-prevalent practice of second sourcing assures competitive pricing and quantity delivery.

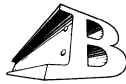
The Motorola Semiconductor Products Division has been in the forefront of linear IC development since the inception of integrated circuit technology. This Linear Integrated Circuit Data Book, therefore, contains data sheets for one of the largest selections of linear ICs in the industry. Included are devices that were developed by the various Motorola R&D groups, as well as an extensive second-source inventory of the most popular circuits developed elsewhere. In addition, some of the linear ICs available as packaged units are also sold in the form of unencapsulated "chips", encompassing conventional chips (MCC prefix), beam-lead chips (MCBC prefix) and flip-chips (MCCF prefix). The chips described by data sheets included in this book are available as standard, off-the-shelf product. Other Motorola manufactured linear circuits can be obtained as conventional chips (designed for conventional wire bonding) on special order.

For easy reference, the data sheets in this book are in alpha-numeric sequence, without regard as to product category or applications. However, to provide the user with a quick overview of Motorola's complete line of standard linear ICs, the General Information section (Section I) contains a number of selector guides in which the total line has been split up into market and functional divisions. This provides a quick comparison of similar devices, spelling out the most significant differences. Other useful data included in the General Information section consists of cross-reference tables of second-source devices and other product-related information.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent rights of any manufacturer.

Second Edition
December, 1972

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† Trademark of Columbia Broadcasting Systems, Inc.

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‡ For complete Data Sheet information please contact your Motorola distributor or salesman.

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MC?

UNDERSTANDING MOTOROLA'S DEVICE NUMBERING SYSTEM

A great deal of information is given in the device number on Motorola ICs. This section will present the meanings of the prefixes, numbers and suffixes used to designate Motorola linear ICs. Normally the package style and operating temperature range may be obtained from the device number.

Although there are exceptions to many of the codes listed below, these codes are generally true and can provide the user with pertinent information on the particular device type.

Prefix

| | |
|------|--|
| MC | Packaged Integrated Circuits |
| MCC | Unencapsulated Integrated Circuit chips |
| MFC | Low cost Integrated Circuits packaged in Motorola's unique "Functional Circuits" plastic package. (Package suffix not used in this device series.) |
| MCBC | Beam-lead Integrated Circuit chips |
| MCB | Packaged Beam-lead Integrated Circuits. (Followed by F suffix when in flat pack.) |
| MCCF | Flip-Chip Linear Integrated Circuits |
| MLM | Pin-for-pin equivalent to Linear Integrated Circuits made by National Semiconductor |
| MCH | Hybrid Integrated Circuit in hermetic package |
| MHP | Hybrid Integrated Circuit in plastic package |

Body Number for Motorola Proprietary Devices

| | |
|-----------|--|
| 1500-1599 | Military temperature grade (-55 to +125°C) Linear ICs |
| 1400-1499 | Equivalent to devices above but with Industrial temperature range (0 to +70°C) |
| 3400-3399 | |
| 1300-1399 | Linear ICs aimed at the Consumer industry |
| 3300-3399 | |

Package Suffix

| | |
|--------|--|
| L | Ceramic dual in-line case (14 or 16 pin) |
| G | Metal can package (TO-5 types) |
| R | Metal power package (TO-66 type) |
| K | Metal power package (TO-3 type) |
| F | Flat package |
| P | Plastic package |
| P1, P2 | Used when an IC is available in more than one plastic package. i.e. P1 = 8 lead plastic DIP, P2 = 14 pin plastic DIP |
| PQ | ICs packaged in staggered-lead plastic DIP packages (Consumer device types only) |
| C | Designates limited temperature, or limited performance device. Followed by package designation suffix, i.e. MC1709CL |
| A | Designates improved or modified IC type, followed by package suffix, i.e. MC1489AL. |

The first part of the document discusses the importance of maintaining accurate records and the role of the auditor in this process. It highlights the need for transparency and accountability in financial reporting, particularly in the context of public sector organizations.

The second part of the document focuses on the specific requirements for the audit process, including the selection of auditors, the scope of the audit, and the reporting requirements. It emphasizes the need for a clear and concise audit report that provides a fair and objective assessment of the organization's financial position.

The third part of the document discusses the challenges faced by auditors in their work, such as the complexity of financial transactions and the need for specialized expertise. It also addresses the issue of the independence of auditors and the potential for conflicts of interest.

The fourth part of the document provides a detailed overview of the audit process, from the initial planning stage to the final reporting stage. It includes a discussion of the various types of audits and the specific procedures used in each.

The fifth part of the document discusses the role of the auditor in the broader context of the organization's governance and risk management. It highlights the importance of the auditor's findings and recommendations in helping the organization improve its financial performance and reduce its risk.

The sixth part of the document discusses the future of auditing and the need for ongoing innovation and improvement in the profession. It highlights the importance of staying up-to-date with the latest developments in accounting and finance, and the need for a strong ethical foundation.

The seventh part of the document discusses the role of the auditor in the public sector and the need for a high level of transparency and accountability. It highlights the importance of the auditor's findings and recommendations in helping the public sector organizations improve their financial performance and reduce their risk.

The eighth part of the document discusses the role of the auditor in the private sector and the need for a high level of transparency and accountability. It highlights the importance of the auditor's findings and recommendations in helping the private sector organizations improve their financial performance and reduce their risk.

The ninth part of the document discusses the role of the auditor in the non-profit sector and the need for a high level of transparency and accountability. It highlights the importance of the auditor's findings and recommendations in helping the non-profit organizations improve their financial performance and reduce their risk.

The tenth part of the document discusses the role of the auditor in the global context and the need for a high level of transparency and accountability. It highlights the importance of the auditor's findings and recommendations in helping the global organizations improve their financial performance and reduce their risk.



Highlights

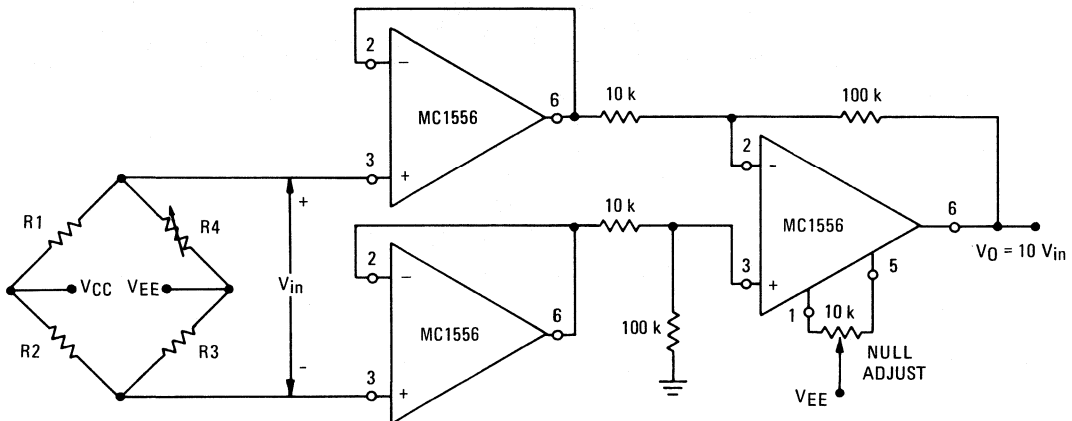
...A small cross-section of new and/or unique devices from Motorola's extensive linear IC product lines that merit special attention.

OPERATIONAL AMPLIFIERS

The operational amplifier has always been the most popular and versatile Linear IC type. Op amps have found wide usage in control circuitry, signal processing equipment, active filters for communications systems, Modems, and many other types of equipment. With the addition of a few external components, this basic feedback type amplifier can be transformed into a multitude of functions ranging from summing amplifiers and simple inverters to integrating amplifiers and Sample and Hold circuits.

Motorola offers a broad line of op amp types. Both proprietary and popular industry-standard types are covered. The range of high precision to low cost plastic-packaged multiple op amps is spanned by over 45 device types. Two representative devices are discussed here. An overview of the entire line appears on page 3-1.

HIGH IMPEDANCE BRIDGE AMPLIFIER



Precision Op Amp (MC1556/1456)

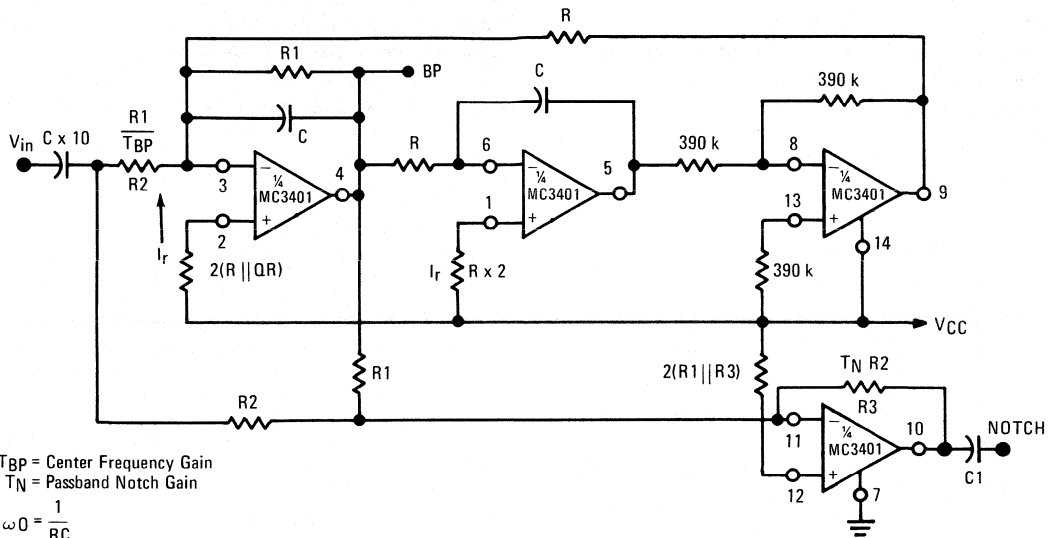
When very high source impedance and high slew rate requirements must be met with an op amp, the MC1556 is a logical choice. This advanced op amp uses super-beta bipolar input transistors to dramatically reduce input bias current (15 mA max). In the past, these low current ratings could be achieved only through the use of field-effect transistors at the input. However, unlike FET input op amps, the super-beta approach does not require that offset voltage drift with temperature be compromised to obtain the low bias currents.

Other features of the MC1556 include a large

power bandwidth of 40 kHz typical, a typical voltage gain of 200,000, low power consumption of 45 mW max, offset-voltage zeroing capability, and output short-circuit and input overvoltage protection. Unity gain slew rate is 2.5 V/ μ s and input offset voltage is 2.0 mV.

Applications include summing, high-impedance bridge, and logarithmic amplifiers. The MC1556 can also be used as a high input-impedance, high-speed voltage follower. In this application, the device shows high tolerance to common-mode voltages at its input, and has a well-balanced large-signal response.

BASIC BANDPASS AND NOTCH FILTER



T_{BP} = Center Frequency Gain
 T_N = Passband Notch Gain
 $\omega_0 = \frac{1}{RC}$
 $R_1 = QR$
 $R_2 = \frac{R_1}{T_{BP}}$
 $R_3 = \frac{R_1}{T_N R_2}$

Lowest Cost Quad Op Amp (MC3301/3401)

At a time when ultra-performance op amps for specialized applications make up the majority of new introductions, a need exists for a low cost, modest performance op amp for industrial and automotive uses. The MC3301/MC3401 provides four such amplifiers in a single plastic package and at cost of less than a dollar in 100-up quantities. The new device is intended for use in industrial control systems and active filters in communication systems. It operates from the power supply

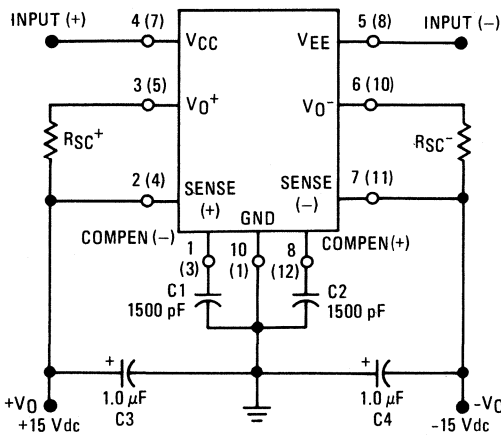
voltages commonly available in these systems. Specifically, the device can be used with 4 to 28 Vdc power supplies without the common mode input voltage problems usually encountered when conventional op amps are operated from a single power supply. Output voltage swing is approximately one volt less than the power supply voltage, while channel separation between the individual amplifiers within a package is 65 dB at 1 kHz.

A number of common applications such as logic gates, differentiators, flip-flops, and multivibrators are given on the device data sheets.

VOLTAGE REGULATORS

The sensitivity of semiconductor devices to voltage and temperature changes makes the voltage regulator circuit an important integral part of many critical systems and subsystems. Today's designer has considerable choice in integrated regulators, with a variety of characteristics, capabilities, and prices. The integrated circuit voltage regulator offers ease of design, simplified assembly and improved performances over discrete transistor designs. Motorola offers a series of IC voltage regulators with a variety of specifications, see page 3-10. Highlighted here are two circuits that merit special attention.

BASIC 50-mA REGULATOR



Op Amp Companion

Most IC operational amplifiers and analog multipliers require symmetrical ± 15 V power supplies. Although a multitude of low-cost IC op amps are now available, the new MC1568 is one of the first low-cost IC voltage regulators specifically designed to supply the required symmetrical voltages. This monolithic dual tracking regulator is preset for ± 15 V (within ± 200 mV) although it may be programmed to outputs of ± 14.5 V through ± 20 V by adding two suitable external resistors. At ± 15 V, the absolute value of output voltages agree within a maximum of 1%.

Thus the designer needs only one IC package, a few passive components (no precision resistors) and a transformer-rectifier assembly capable of providing between ± 17 and ± 30 V to obtain the ± 15 V power source for control circuitry. Without external current boosting transistors, this regulator can provide output currents up to ± 100 mA, sufficient for most op amp applications. The device features remote sensing and externally adjustable current limiting.

Unique "Floating" Regulator

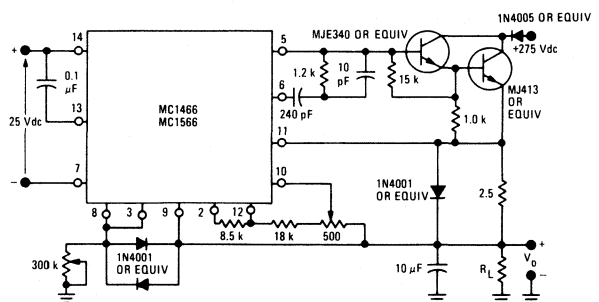
While most IC voltage regulators are limited to output voltages less than 50 V and output currents below a few amperes, the MC1566 uses a unique approach that has virtually no limits in the range of practical applications.

The regulator is designed to control an external power transistor and will operate at any voltage or current level that the power transistor can handle. In addition, performance is on the level of laboratory-type supplies.

Some of the features of the circuit include: voltage and/or current adjustable to zero, automatic crossover (goes from constant voltage to constant current regulation — not just current limiting), remote sensing, remote programming, line voltage regulation of $0.01\% + 1$ mV, load voltage regulation $0.01\% + 1$ mV, current regulation $0.1\% + 1$ mA, and a temperature coefficient that is typically $0.004\%/^{\circ}\text{C}$.

The high voltage capability is due to the "floating" nature of the circuit, with operating voltage for the circuit obtained from a separate, isolated supply (about 25 Vdc). Voltage regulation is accomplished by comparing the power output voltage to a reference voltage generated by passing

0-TO-250 VDC, 0.1-AMPERE REGULATOR



an adjustable current through a voltage-setting resistor. Since the entire output voltage is compared to the reference voltage, the MC1566L always operates at maximum loop gain, establishing excellent regulation over the entire voltage range.

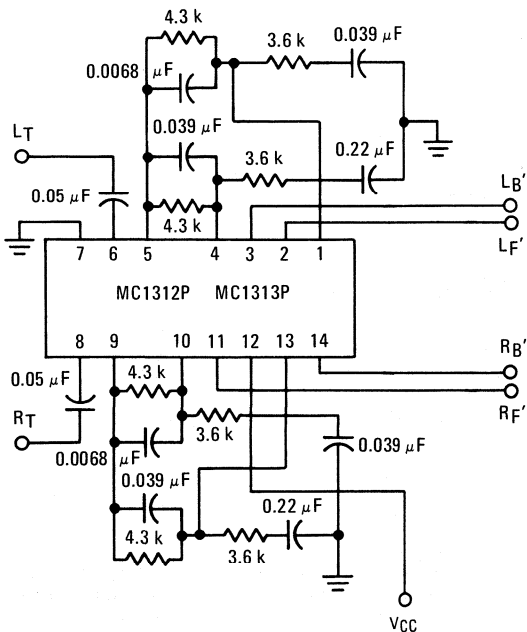
Since the series pass transistor is external to the integrated circuit, power dissipation of the IC is constant, preventing degradation of regulation due to heating.

For Audio . . .

Linear ICs are rapidly penetrating the audio amplifier stages of television, radio, and stereo phonographs. Both low level and power amplifier applications are realizing greater performance and lower total cost due to the reduced assembly requirements and the ability to use more complex circuitry with these advanced ICs. A wide range of IC types permits the designer a wide latitude of flexibility to create the exact system performance and costs he requires.

New Audio devices include . . .

- The new MC1339 replacement for the popular 239 type preamplifier has joined the existing MC1303 stereo preamp.
- Power audio amplifiers are presently limited to about two-watt levels, although higher power units are on the drawing boards.
- Highlighted below is Motorola's entry into the Quad-Stereo field. This unit is the first in a series of four channels ICs. Upcoming quad-stereo products are previewed on page 4-1.



An IC for the Quad Sound

The quad sound is the newest trend in audio! To meet this trend, Motorola has introduced the MC1312/1313 quadraphonic decoder — the first IC for the CBS developed SQ matrix system.

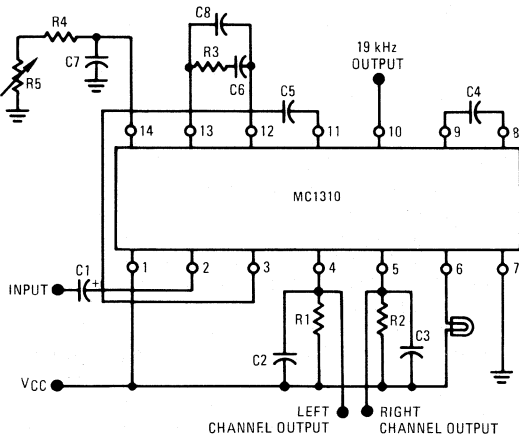
The device consists of two preamplifiers which are fed with left total, L_T , and right total, R_T , signals. The preamplifiers each feed two all-pass networks which are used to generate two L_T signals in quadrature and two R_T signals in quadrature. The four signals are matrixed to yield left front, left back, right front, and right back signals (L_F , L_B , R_F , R_B).

The MC1312 is expected to find wide use in low-cost audio equipment and, with the addition of logic circuitry to enhance quadraphonic separation, it may be used in even the most sophisticated "component type" systems. The MC1313 version is specifically intended for use in automotive audio equipment.

For Radio

Two sections in FM radios have lent themselves well to integration: The IF amplifier and detector, and the stereo multiplex decoder sections. In both high-quality tuners and in low-priced table radios, the high performance of these ICs and lower assembly costs they make possible, permit more efficient designs.

Specifically highlighted is a new stereo decoder which promises to become the new industry standard decoder circuit. Other devices for use in both AM and FM radio are listed in the selector guide on page 3-14.



tunable inductors, the new circuit offers a significant savings in component and assembly costs and improved long term performance.

The new device makes use of the advanced phase locked loop principle to lock onto the 19 kHz pilot signal provided by the stereo broadcaster and to create a signal which is in phase with the pilot signal and of exactly double the frequency. This 38 kHz subcarrier is then used to demodulate the stereo information.

An automatic stereo-mono switching circuit is provided to disable the decoder during monaural broadcasts or weak stereo broadcasts. This switch also controls a lamp driver which employs 6 dB of hysteresis to avoid flickering of the stereo indicator lamp due to variations in signal level.

Performance of the new decoder is as good or better than the usual frequency doubler type of stereo demodulators. Stereo separation is 40 dB at 1 kHz with total harmonic distortion at typically 0.3% for a 560 mV level of composite input.

No coils needed with this Stereo Decoder

The new MC1310 is the second generation stereo decoder circuit. This decoder provides high performance, low external parts count and reduced alignment requirements. It requires no tuned circuits and only one non-critical adjustment is necessary after assembly. Until now, IC decoders usually required three tuned circuits which had to be adjusted at the factory in each individual stereo tuner. Performance could be degraded if any one of the tuned circuits became detuned due to vibration or component aging. By eliminating the

INTERFACE CIRCUITS

Interface circuits is the name applied to devices that operate with both linear signals and digital logic levels. Most have both linear and digital properties. Examples of interface circuits are D/A and A/D converters, memory sense amplifiers, comparators, and line driver and receivers.

The rapidly expanding fields of data communications and digital instrumentation make wide use of these interface devices. Line drivers, and receiver, for example, are used whenever data must be transmitted over long distances in a computer or piece of peripheral equipment. Also, the industry standard MC1488-89 devices provide the level translation between a Modem and a computer terminal in accordance with the EIA RS-232C specifications. Likewise comparators are used as voltage level detectors in control and instrumentation applications.

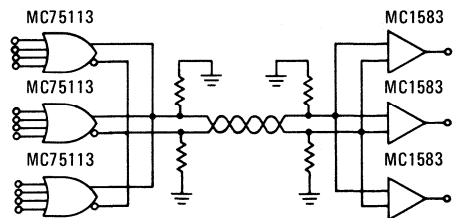
Motorola offers a broad line of interface circuits. Two of the newest interface devices are discussed below while the complete lineup is outlined beginning on page 3-3.

New Line Driver for Computer Systems

The MC75113 was primarily designed to be used for transmitting data at high speeds over long distances in systems where numerous drivers and receivers share a common twisted-pair line in a "Party-Line" mode.

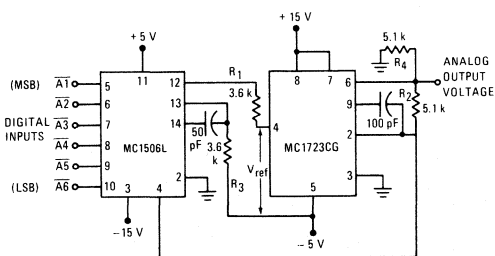
The device provides two output currents of equal but opposite polarities. This technique offers several advantages over most IC drivers employing a single polarity output current. With the matched currents used in the MC75113, both wires in the twisted pair transmission line carry equal and opposite currents thereby minimizing cross-talk radiation. Likewise, the matched currents reduce ground loop currents which can generate voltages that reduce the useful common mode range of drivers and receivers in a system.

This new technique produces twice the differential voltage at the opposite end of the transmission line as single-ended drivers of equal



output rating, thus promoting reduced data errors and greater noise immunity.

Specifically, the MC75113 features a TTL compatible four input OR gate and output currents of nominally ± 20 mA.



$$V_o = V_{ref} \left(\frac{R_2}{R_1} \right) \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} \right]$$

A Low Cost D/A Converter

Most D/A converters are either hybrid or modular units. This often prevents them from selling at a modest price. However, the MC1506, 6-bit converter uses a high-yield monolithic fabrication technique whereby literally hundreds of units are built on a single silicon wafer. This allows the MC1506 to sell for much less than many comparable units.

The MC1506 uses the popular R-2R resistor ladder network whose stringent requirements have

prevented their manufacture on the same chip with the active devices in the past. In order to use diffused resistors, unique design techniques were adopted to avoid variations in conversion speed due to the parasitic capacitances associated with diffused resistors.

A current mode output was chosen for the IC converter rather than a voltage mode output to allow faster conversion speed. Nevertheless, a voltage output is easily obtained by adding an external operational amplifier. The device may also be used as a digitally-controlled attenuator to produce the product of a digital word and an analog signal which is applied to the reference input. This is possible due to the "multiplying" nature of the converter.

In particular, the MC1506 features TTL and DTL compatible inputs and a relative accuracy of at least 0.78% over a range of -55 to 125°C . Output current drift is held to about $0.002\%/^\circ\text{C}$ and the output current is 2.0 mA maximum. Settling time to within 1/2 of the least significant bit is 200 ns.

Several other products are planned in the A/D, D/A area. An 8-bit D/A converter and a control element for use with a D/A converter to produce an A/D converter are previewed on page 4-5.

OPERATIONAL AMPLIFIERS

Motorola offers a broad line of operational amplifiers to meet a wide range of usages. From low-cost, industry standard types to high precision circuits the span encompasses a large range of performance capabilities.

These linear integrated circuits are available as single, dual, and quad monolithic devices in a variety of package styles as well as standard and beam-lead chips.

OPERATIONAL AMPLIFIERS

Listed in order of increasing input bias current within temperature group. (See reverse side of sheet for dual and quad operational amplifiers and drivers.)

INTERNALLY COMPENSATED

| I _B (μ A max) | V _{IO} (mV max) | I _{IO} (nA max) | A _{vol} (V/V min) | V _O @ (V _{pk} min) | R _L & V _{CC} , V _{EE} (k Ω) (Vdc) | f _c (MHz typ) | BW _p (kHz typ) | SR (V/ μ s typ) | Case | Type | |
|--|-----------------------------|-----------------------------|-------------------------------|---|---|-----------------------------|------------------------------|------------------------|------|-------------------|------------|
| -55 to +125°C Temperature Range | | | | | | | | | | | |
| 0.015 | 4.0 | 2.0 | 100,000 | 12 | 2.0 | ± 15 | 1.0 | 40 | 2.5 | 601 | MC1556 |
| 0.02 | 5.0 | 3.0 | 100,000 | 22 | 5.0 | ± 28 | 1.0 | 23 | 2.0 | 601 | MC1536* |
| 0.075 | 2.0 | 10 | 50,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.5 | 601 | MLM107 |
| 0.5 | 5.0 | 200 | 50,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.8 | 601,606,632,665** | MC1741***† |

-25 to +85°C Temperature Range

| | | | | | | | | | | | |
|-------|-----|----|--------|----|-----|----------|-----|-----|-----|-----|--------|
| 0.003 | 4.0 | — | Unity | 10 | 10 | ± 15 | 20 | 300 | 30 | 601 | MLM210 |
| 0.075 | 2.0 | 10 | 50,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.5 | 601 | MLM207 |

0 to +70°C Temperature Range

| | | | | | | | | | | | |
|-------|-----|-----|--------|----|-----|----------|-----|-----|------|---------------------|------------|
| 0.007 | 7.5 | — | Unity | 10 | 10 | ± 15 | 20 | 300 | 30 | 601 | MLM310 |
| 0.03 | 10 | 10 | 70,000 | 11 | 2.0 | ± 15 | 1.0 | 40 | 2.5 | 601 | MC1456 |
| 0.04 | 10 | 10 | 70,000 | 20 | 5.0 | ± 28 | 1.0 | 23 | 2.0 | 601 | MC1436* |
| 0.09 | 12 | 30 | 25,000 | 10 | 2.0 | ± 15 | 1.0 | 40 | 2.5 | 601 | MC1456C |
| 0.09 | 12 | 25 | 50,000 | 20 | 5.0 | ± 28 | 1.0 | 23 | 2.0 | 601 | MC1436C |
| 0.25 | 7.5 | 50 | 25,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.57 | 601 | MLM307 |
| 0.5 | 6.0 | 200 | 20,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.8 | 601,606,626,632,646 | MC1741C**† |

NONCOMPENSATED

| I _B (μ A max) | V _{IO} (mV max) | I _{IO} (nA max) | A _{vol} (V/V min) | V _O @ (V _{pk} min) | R _L & V _{CC} , V _{EE} (k Ω) (Vdc) | f _c (MHz typ) | BW _p (kHz typ) | SR (V/ μ s typ) | Case | Type | |
|--|-----------------------------|-----------------------------|-------------------------------|---|---|-----------------------------|------------------------------|------------------------|------|-------------------|------------|
| -55 to +125°C Temperature Range | | | | | | | | | | | |
| 0.075 | 2.0 | 10 | 50,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.5 | 601 | MLM101A |
| 0.15 | 10 | 25 | 2,500 | 4.5 | 1.0 | ± 6.0 | 2.0 | 100 | 1.4 | 602B,606 | MC1531 |
| 0.5 | 3.0 | 60 | 50,000 | 10 | 1.0 | ± 15 | 2.0 | 50 | 4.2 | 601,632 | MC1539* |
| 0.5 | 5.0 | 200 | 50,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.8 | 601,606** | MC1748*** |
| 0.5 | 5.0 | 200 | 25,000 | 10 | 2.0 | ± 15 | 0.5 | 4.0 | 0.25 | 601,606,632,665** | MC1709***† |
| 1.0 | 5.0 | 150 | 40,000 | 11 | 2.0 | ± 15 | 0.8 | 2.0 | 2.0 | 602B,606,632 | MC1533 |
| 2.0 | 10 | 100 | 1,000 | 3.5 | 7.0 | ± 6.0 | 10 | 150 | 5.0 | 602A,606 | MC1520 |
| 5.0 | 2.0 | 500 | 2,500 | 3.5 | 10 | +12,-6.0 | 7.0 | 10 | 1.5 | 601,606,632 | MC1712 |
| 10 | 5.0 | 2000 | 4,500 | 4.5 | 1.0 | ± 6.0 | 3.0 | 100 | 1.7 | 602B,606 | MC1530 |

-25 to +75°C Temperature Range

| | | | | | | | | | | | |
|-------|-----|----|--------|----|-----|----------|-----|----|-----|-----|---------|
| 0.075 | 2.0 | 10 | 50,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.5 | 601 | MLM201A |
|-------|-----|----|--------|----|-----|----------|-----|----|-----|-----|---------|

0 to +75°C Temperature Range

| | | | | | | | | | | | |
|------|-----|------|--------|-----|-----|-----------|-----|-----|------|---------------------|------------|
| 0.25 | 7.5 | 50 | 25,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.5 | 601,626 | MLM301A |
| 0.3 | 15 | 100 | 1,500 | 4.0 | 1.0 | ± 6.0 | 2.0 | 100 | 1.4 | 602B,606,646 | MC1431 |
| 0.5 | 6.0 | 200 | 20,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.8 | 601 | MC1748C* |
| 1.0 | 7.5 | 100 | 15,000 | 10 | 2.0 | ± 15 | 2.0 | 50 | 4.2 | 601,632,646 | MC1439* |
| 1.5 | 7.5 | 500 | 15,000 | 10 | 2.0 | ± 15 | 0.5 | 4.0 | 0.25 | 601,606,626,632,646 | MC1709C**† |
| 2.0 | 7.5 | 500 | 30,000 | 10 | 2.0 | ± 15 | 0.8 | 2.0 | 2.0 | 602B,606,632,646 | MC1433 |
| 4.0 | 15 | 200 | 750 | 3.0 | 7.0 | ± 6.0 | 10 | 150 | 5.0 | 602A,606 | MC1420 |
| 7.5 | 5.0 | 2000 | 2,000 | 3.5 | 10 | +12,-6.0 | 7.0 | 10 | 1.5 | 601,606,632 | MC1712C |
| 15 | 10 | 4000 | 3,000 | 4.0 | 1.0 | ± 6.0 | 3.0 | 100 | 1.7 | 602B,606,646 | MC1430 |

*Use MCC prefix for nonencapsulated chip.

**Use MCBC prefix for nonencapsulated beam-lead device, use MCB prefix for beam-lead device in flat ceramic package.

†Use MCCF prefix for nonencapsulated flip-chip.

DEFINITIONS

| | | | |
|-----------------|------------------------|------------------|--------------------------------|
| SR | Slew Rate @ Unity Gain | A _{vol} | Open-Loop Voltage Gain |
| V _{IO} | Input Offset Voltage | V _O | Output Voltage Swing |
| I _B | Input Bias Current | f _c | Unity Gain Crossover Frequency |
| I _{IO} | Input Offset Current | BW _p | Power Bandwidth |

OPERATIONAL AMPLIFIERS (Continued)

DUAL OPERATIONAL AMPLIFIERS

Listed in increasing order of input bias current.

INTERNALLY COMPENSATED

| I _{IB} (μ A max) | V _{IO} (mV max) | I _{IO} (nA max) | A _{vol} (V/V min) | V _O @ R _L & V _{CC} , V _{EE} (V _{pk} min) | (k Ω) | (Vdc) | f _c (MHz typ) | BW _p (kHz typ) | SR (V/ μ s typ) | Case | Type |
|--|-----------------------------|-----------------------------|-------------------------------|--|---------------|----------|-----------------------------|------------------------------|------------------------|---------|----------|
| -55 to +125°C Temperature Range | | | | | | | | | | | |
| 0.5 | 5.0 | 200 | 50,000 | 10 | 2.0 | ± 15 | 1.1 | 14 | 0.8 | 601,632 | MC1558*† |
| 0.5 | 5.0 | 200 | 50,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.5 | 632 | MC1747 |

0 to +75°C Temperature Range

| | | | | | | | | | | | |
|-----|-----|-----|--------|-----|-----|----------|-----|----|-----|-----------------|----------|
| 0.5 | 6.0 | 200 | 20,000 | 10 | 2.0 | ± 15 | 1.1 | 14 | 0.8 | 601,626,632,646 | MC1458*† |
| 0.5 | 6.0 | 200 | 25,000 | 10 | 2.0 | ± 15 | 1.0 | 10 | 0.5 | 632 | MC1747C |
| 0.7 | 10 | 300 | 20,000 | 9.0 | 2.0 | ± 15 | 1.1 | 14 | 0.8 | 601,626,632,646 | MC1458C |

*Use MCC prefix for nonencapsulated chip.

†Use MCCF prefix for nonencapsulated flip-chip.

NONCOMPENSATED

| I _{IB} (μ A max) | V _{IO} (mV max) | I _{IO} (nA max) | A _{vol} (V/V min) | V _O @ R _L & V _{CC} , V _{EE} (V _{pk} min) | (k Ω) | (Vdc) | f _c (MHz typ) | BW _p (kHz typ) | SR (V/ μ s typ) | Case | Type |
|--|-----------------------------|-----------------------------|-------------------------------|--|---------------|-----------|-----------------------------|------------------------------|------------------------|--------------|--------|
| -55 to +125°C Temperature Range | | | | | | | | | | | |
| 0.5 | 5.0 | 200 | 25,000 | 12 | 10 | ± 15 | 1.0 | 3.0 | 0.25 | 632 | MC1537 |
| 3.0 | 3.0 | 300 | 4,000 | 2.5 | 10 | ± 6.0 | 1.0 | 40 | 0.013 | 602B,607,632 | MC1535 |

0 to +75°C Temperature Range

| | | | | | | | | | | | |
|-----|-----|-----|--------|-----|----|-----------|-----|-----|-------|------------------|--------|
| 1.5 | 7.5 | 500 | 15,000 | 12 | 10 | ± 15 | 1.0 | 3.0 | 0.25 | 632,646 | MC1437 |
| 5.0 | 5.0 | 500 | 3,500 | 2.3 | 10 | ± 6.0 | 1.0 | 40 | 0.013 | 602B,607,632,646 | MC1435 |

QUAD OPERATIONAL AMPLIFIERS

Internally Compensated

... for automotive applications

| I _{IB} (μ A max) | V _{IO} (mV max) | I _{IO} (nA max) | A _{vol} (V/V min) | V _O @ R _L & V _{CC} , V _{EE} (V _{pk} min) | (k Ω) | (Vdc) | f _c (MHz typ) | BW _p (kHz typ) | SR (V/ μ s typ) | Case | Type |
|-----------------------------------|-----------------------------|-----------------------------|-------------------------------|--|---------------|-------|-----------------------------|------------------------------|------------------------|------|--------|
| 0.3 | - | - | 1,000 | 10 | 5.0 | +15 | 4.0 | 20 | 0.6 | 646 | MC3301 |

... for industrial applications

| | | | | | | | | | | | |
|-----|---|---|-------|----|-----|-----|-----|----|-----|-----|--------|
| 0.3 | - | - | 1,000 | 10 | 5.0 | +15 | 5.0 | 20 | 0.6 | 646 | MC3401 |
|-----|---|---|-------|----|-----|-----|-----|----|-----|-----|--------|

POWER DRIVERS

INTERNALLY COMPENSATED

| I _{IB} (μ A max) | V _{IO} (mV max) | I _{IO} (nA max) | A _{vol} (V/V min) | V _O @ R _L & V _{CC} , V _{EE} (V _{pk} min) | (Ω) | (Vdc) | f _c (MHz typ) | BW _p (kHz typ) | SR (V/ μ s typ) | Case | Comments | Type |
|--|-----------------------------|-----------------------------|-------------------------------|--|--------------|----------|-----------------------------|------------------------------|------------------------|------|--|----------|
| -55 to +125°C Temperature Range | | | | | | | | | | | | |
| 200 | - | - | 900 | 12 | 300 | ± 15 | - | 1500 | 75 | 614 | High current gain (70 dB) op ampl power booster I _O = 300 mA max | MC1538 |
| 0.5 | 5.0 | 200 | 50,000 | 12 | 300 | ± 15 | 1.1 | 12 | 0.8 | 614 | MC1741 with high current capability, ± 300 mA max | MCH2870M |

0 to +75°C Temperature Range

| | | | | | | | | | | | | |
|-----|-----|-----|--------|----|-----|----------|-----|------|-----|-----|---|----------|
| 300 | - | - | 850 | 11 | 300 | ± 15 | - | 1500 | 75 | 614 | High current gain (70 dB) op ampl power booster, I _O = 300 mA max | MC1438 |
| 0.5 | 6.0 | 200 | 20,000 | 11 | 300 | ± 15 | 1.1 | 12 | 0.8 | 614 | MC1741 with high current capability, ± 300 mA max | MCH2870C |

3

INTERFACE CIRCUITS

Interface circuits fit in the gray area between the linear and digital realms. Usually these IC's perform the necessary translation between an analog signal input and the required digital logic levels or vice versa. To aid in

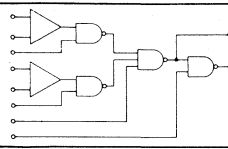
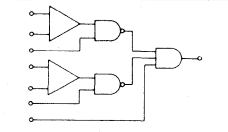
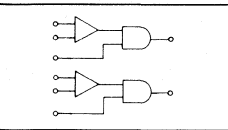
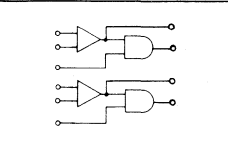
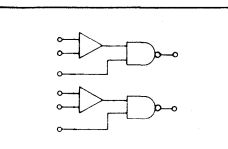
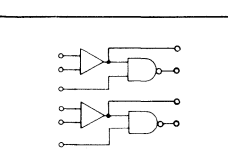
selection, the devices have been divided into five main categories: Sense Amplifiers, Drivers, Receivers, Comparators, and D/A Converters.

SENSE AMPLIFIERS

The sense amplifiers listed provided the necessary translation from the outputs of core or plated-wire memories to MTTL (unless otherwise noted) logic levels. Unless noted, all devices are designed to operate from

±5.0 volt power supplies. The output of these sense amplifiers changes logic states when the differential input voltage exceeds a specified threshold level, regardless of input polarity.

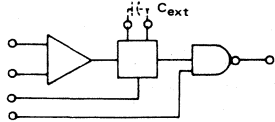
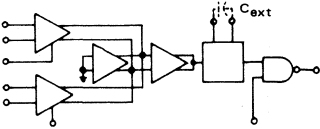
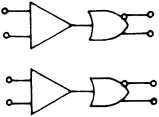
CORE MEMORY

| Function | Threshold Voltage @ | | V _{ref} (mV) | Propagation Delay (ns max) | Case | Type | |
|--|---------------------|----------|-----------------------|----------------------------|-----------|---------------|------------|
| | min | max | | | | -55 to +125°C | 0 to +70°C |
|  Dual channel with independent gating, complementary outputs, memory data register | 11 36 | 19 44 | 15 40 | 55 | 620 | — | MC7520 |
| | 8.0 33 | 22 47 | 15 40 | 55 | 620 | — | MC7521 |
|  Dual channel with open-collector output, high sink current capability | 11 36 | 19 44 | 15 40 | 45 | 620 | — | MC7522 |
| | 8.0 33 | 22 47 | 15 40 | 45 | 620 | — | MC7523 |
|  Dual with independent strobing | 11 36 | 19 44 | 15 40 | 40 | 620 | — | MC7524 |
| | 8.0 33 | 22 47 | 15 40 | 40 | 620 | — | MC7525 |
|  Same as MC7524-25 except amplifier test points included | 11 36 | 19 44 | 15 40 | 40 | 620, 648* | — | MC7528 |
| | 10 35 | 20 45 | 15 40 | 40 | 620 | MC5528 | — |
| | 8.0 33 | 22 47 | 15 40 | 40 | 620, 648* | MC5529 | MC7529 |
|  Same as MC7524-25 except NAND outputs | 11 36 | 19 44 | 15 40 | 40 | 620, 648* | — | MC7534 |
| | 10 35 | 20 45 | 15 40 | 40 | 620 | MC5534 | — |
| | 8.0 33 | 22 47 | 15 40 | 40 | 620, 648* | MC5535 | MC7535 |
|  Same as MC7528-29 except NAND outputs | 11 36 | 19 44 | 15 40 | 40 | 620, 648* | — | MC7538 |
| | 10 35 | 20 45 | 15 40 | 40 | 620 | MC5538 | — |
| | 8.0 33 | 22 47 | 15 40 | 40 | 620, 648* | MC5539 | MC7539 |

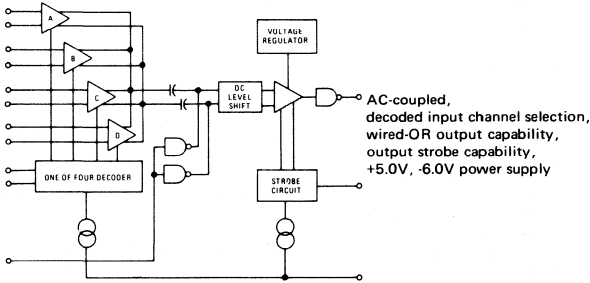
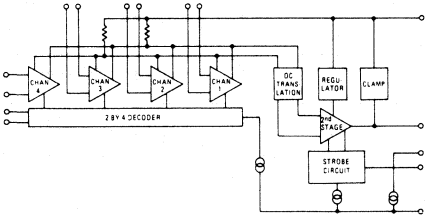
*Case 648 used with commercial-temperature-range devices only.

INTERFACE CIRCUITS (Continued)

SENSE AMPLIFIERS (continued) CORE MEMORY (Continued)

| Function | Threshold Voltage (mV) @ | | V_{ref} (mV) | Propagation Delay (ns max) | Case | Type | |
|---|--------------------------|-----|----------------|----------------------------|----------------------|---------------|------------|
| | min | max | | | | -55 to +125°C | 0 to +75°C |
|  <p>0.5μs cycle time, 20ns typ response time, ±6.0V power supply</p> | 14 | 20 | -6.0V | 30 | 602B, 606, 632 | MC1540 | MC1440 |
|  <p>0.4μs cycle time, 1.5V common-mode inputs, 1.0mV typ input offset</p> | 14 | 20 | -5.0V | 30 | 607, 632 | MC1541 | MC1441 |
|  <p>Compatible with MECL, +5.0V, -5.2V power supplies, threshold insensitive to supply variations, complementary outputs</p> | 17 | 23 | 540 | 35 | 632 | MC1543 | — |

PLATED WIRE MEMORIES

| Function | Threshold Voltage (mV - typ) | Propagation Delay (ns - max) | Case | Type | |
|---|------------------------------|------------------------------|------|---------------|------------|
| | | | | -55 to +125°C | 0 to +75°C |
|  <p>AC-coupled, decoded input channel selection, wired-OR output capability, output strobe capability, +5.0V, -6.0V power supply</p> | 1.0 | 25 | 620 | MC1544 | MC1444 |
|  <p>DC-coupled, decoded input, 0.5 mV input offset, output strobe capability, +5.0V, -6.0V power supply</p> | 3.0 | 18 | 620 | MC1546 | MC1446 |

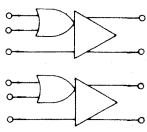
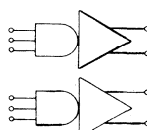
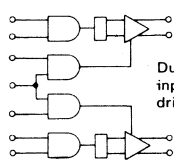
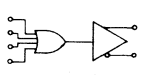
INTERFACE CIRCUITS (Continued)

DRIVERS

Several types of interface drivers are tabulated in this section: twisted-pair drivers for transmitting data over long lines, RS-232 drivers for interfacing modems and

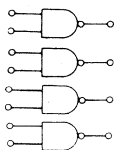
terminals, peripheral drivers for driving lamps, relays and memories, and MOS clock drivers for providing the required clock pulses to highly-capacitive loads.

TWISTED-PAIR LINE DRIVERS

| Function | Compatibility | I _{O(on)} mA (min/max) | I _{O(off)} (μA - max) | t _{PLH} /t _{PHL} Input to Output (ns - typ) | Case | Type | |
|--|------------------|---------------------------------------|-----------------------------------|---|------------------------|--------------------|--------------------|
| | | | | | | -55 to +125°C | 0 to +70°C |
|  <p>Dual Driver/Receiver with MECL Bias Supply</p> | MDTL, MECL, MRTL | 6.9/10.4 | 5.0 | 13/13 | 632 | MC1580 | - |
|  <p>Dual 3-Input Driver</p> | MDTL, MTTL, MRTL | 6.9/10.4 | 5.0 | 15/13 | 632 | MC1582 | - |
|  <p>Dual Driver with inhibit inputs for party-line driver applications</p> | MTTL | 3.5/7.0 6.5/15 | 100 100 | 9.0/9.0 9.0/9.0 | 632, 646# 632, 646# | MC55109 MC55110 | MC75109 MC75110 |
|  <p>Differential Party-Line Driver with push-pull outputs</p> | MDTL | 18/26 | - | 25/15 | 632 | - | MC75113† |

#Case 646 used with industrial-temperature-range devices only.
† 0 to +75°C Temperature Range

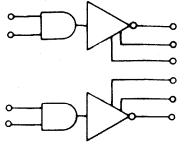
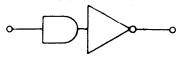
RS-232 LINE DRIVER

| Function | Compatibility | V _{OL} V _d c min | & V _{OH} V _d c min | & V _{CC} V _d c | & V _{EE} V _d c | t _{PLH} /t _{PHL} ns typ | Case | Type 0 to +75°C |
|---|---------------|--|---|--|--|---|------|--------------------|
|  <p>Quad Line Driver</p> | MDTL, MTTL | -6.0 -9.0 | +6.0 +9.0 | +9.0 +13.2 | -9.0 -13.2 | 150/65* | 632 | MC1488 |

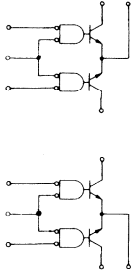
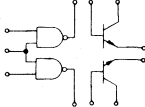
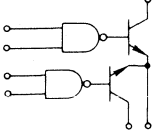
* @ 3000 ohms, 15 pF

INTERFACE CIRCUITS (Continued)

DRIVERS (continued)
MOS CLOCK DRIVERS

| Function | Input Compatibility | PRR (max) C = 1000 pF @ V_{CC}/V_{EE} (volts) | | Switching Times C = 1000 pF, ns-typ | | | | Temperature (°C) | Case | Type |
|---|---------------------|---|---------|--|-----------|-----------|-----------|---------------------|------|---------|
| | | | | t_{PLH} | t_{TLH} | t_{PHL} | t_{THL} | | | |
| Dual MOS Clock Driver with Strobe  | MDTL, MTTL | 2.0 MHz | 5.0/-20 | 55 | 50 | 25 | 22 | -55 to +125 | 632 | MC1585 |
| High-Speed Hybrid MOS Clock Driver  | MTTL | 4.0 MHz | 5.0/-12 | 13 | 40 | 23 | 35 | 0 to +70 | 646 | MHP 401 |

PERIPHERAL DRIVERS

| Function | Compatibility | $I_{O(on)}$ (mA - max) | t_{PLH}/t_{PHL} Input to Output (ns - typ) | Case | Type | |
|--|---------------|---------------------------|---|--------------|---------------|------------|
| | | | | | -55 to +125°C | 0 to +70°C |
| Dual Memory Driver with logic inputs, 24-volt output capability  | MDTL, MTTL | 600 | 25/25 (to source collectors) 20/20 (to sink outputs) | 620, 648# | MC55325 | MC75325 |
| Dual Peripheral Positive AND Driver, plus two noncommitted NPN output transistors  | MDTL, MTTL | 300* | 21/16 | 632 646 | - | MC75450 |
| Dual Peripheral Positive AND Driver with logic gate outputs internally connected  | MDTL, MTTL | 300* | 17/18 | 626 | - | MC75451 |

*Case 648 used with industrial-temperature-range devices only.

*Each transistor

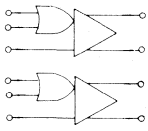
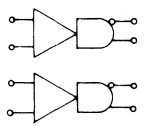
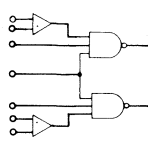
INTERFACE CIRCUITS (Continued)

RECEIVERS

Mating with the driver types listed in the previous section are the receivers tabulated in this section:

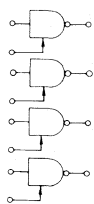
twisted-pair receivers for computer applications, and RS-232 receivers to interface with similar drivers.

TWISTED-PAIR LINE RECEIVERS

| Function | Compatibility | Input Threshold (mV - typ) | Input Common Mode Range (V - min) | t _{PLH} /t _{PHL} Input to Output (ns - typ) | Case | Type | | |
|---|------------------------|----------------------------|-----------------------------------|---|-------|---------------|-----------------|---|
| | | | | | | -55 to +125°C | 0 to +70°C | |
|  <p>Dual Driver/Receiver with MECL Bias Supply</p> | MDTL, MECL, MRTL, MTTL | ±40 | ±3.5 | 13/13 | 632 | MC1580 | - | |
|  <p>Dual Line Receiver</p> | MECL | ±10 | ±3.5 | 15/25 | 632 | MC1581 | - | |
| | Open Collector Outputs | MDTL, MRTL, MTTL | ±2.0 | ±3.5 | 24/34 | 632 | MC1583 | - |
| | Active Pullup | MDTL, MTTL | ±40 | ±3.5 | 32/28 | 632 | MC1584 | - |
|  <p>Dual Line Receiver with strobe inputs</p> | Active Pullup | MTTL | ±25 | ±3.0 | 17/17 | 632, 646# | MC55107 MC75107 | |
| | Open Collector Output | MTTL | ±25 | ±3.0 | 19/19 | 632, 646# | MC55108 MC75108 | |

#Case 646 used with industrial-temperature-range devices only.

RS-232 LINE RECEIVERS

| Function | Compatibility | Input Turn-On Threshold (V _{dc} - max) | Input Turn-Off Threshold (V _{dc} - max) | Input Hysteresis (mV - typ) | t _{PLH} /t _{PHL} (ns - typ) | Case | Type 0 to +75°C |
|---|---------------|---|--|-----------------------------|---|------|-----------------|
|  <p>Quad Line Receiver</p> | MDTL, MTTL | 1.5 | 1.25 | 250 | 25/25 | 632 | MC1489 |
| | MDTL, MTTL | 2.25 | 1.25 | 1150 | 25/25 | 632 | MC1489A |

INTERFACE CIRCUITS (continued)

COMPARATORS

A comparator provides a logical output in response to the polarity of the differential voltage applied to the inputs of the device. All comparators shown are intended for operation from +12 V and -6.0 V power

supplies, and interface to saturated logic levels. Maximum differential input voltage is ± 5.0 V and propagation delay time is 40 ns for all device types shown.

| A_{vol} (V/V min) | V_{IO} (mVdc max) | I_{IB} (μ A max) | V_{OH} (Vdc) | | V_{OL} (Vdc) | | I_{Os} (mA min) | t_p (ns typ) | Case | Type | Features |
|--|------------------------|----------------------------|-------------------|-----|-------------------|-----|----------------------|-------------------|----------------|-----------|---|
| | | | min | max | min | max | | | | | |
| -55 to +125°C Temperature Range | | | | | | | | | | | |
| 1,250 | 2.0 | 20 | 2.5 | 4.0 | -1.0 | 0 | 2.0 | 40 | 601,606,632 | MC1710*** | Output impedance = 200 ohms |
| 1,250 | 2.0 | 20 | 2.5 | 4.0 | -1.0 | 0 | 2.8 | 40 | 632 | MC1514 | Dual, strobe capability |
| 750 | 3.5 | 75 | 2.5 | 5.0 | -1.0 | 0 | 0.5 | 40 | 603-02,606,632 | MC1711* | Dual with outputs wired OR, strobe capability |

0 to +75°C Temperature Range

| | | | | | | | | | | | |
|-------|-----|-----|-----|-----|------|---|-----|----|--------------------|----------|--|
| 1,000 | 5.0 | 25 | 2.5 | 4.0 | -1.0 | 0 | 1.6 | 40 | 601,606,632,646 | MC1710C* | Output impedance = 200 ohms |
| 1,000 | 5.0 | 25 | 2.5 | 4.0 | -1.0 | 0 | 1.6 | 40 | 632,646 | MC1414 | Dual, strobe capability |
| 700 | 5.0 | 100 | 2.5 | 5.0 | -1.0 | 0 | 0.5 | 40 | 603-02,606,632,646 | MC1711C* | Dual with outputs wired OR strobe capability |

QUAD COMPARATOR

| V_{IO} (mVdc max) | I_{IB} (μ A max) | V_{OL} (Vdc max) | Output Leakage Current (μ A max) | I_{Os} (mA typ) | V_{IDR} (Vdc max) | Case | Type |
|------------------------|----------------------------|-----------------------|--|----------------------|------------------------|------|------|
|------------------------|----------------------------|-----------------------|--|----------------------|------------------------|------|------|

-40 to +85°C Temperature Range

| | | | | | | | |
|----|-----|-----|----|-----|--------------|-----|--------|
| 10 | 0.5 | 0.4 | 10 | 5.0 | $\pm V_{CC}$ | 646 | MC3302 |
|----|-----|-----|----|-----|--------------|-----|--------|

Features

These comparators are designed specifically for single positive-power-supply operation from +2.0 to +28 Vdc. Each monolithic device contains four independent comparators, yet total package power supply current drain is 1.5 mA max.

*Use MCC prefix for nonencapsulated chip.

**Use MCBC prefix for nonencapsulated beam-lead device; use MCB prefix for beam-lead device in ceramic flat package.

DEFINITIONS

| | | | |
|-----------|----------------------------|----------|-------------------------|
| A_{vol} | Open-Loop Voltage Gain | V_{OH} | Positive Output Voltage |
| V_{ID} | Differential Voltage Range | V_{OL} | Negative Output Voltage |
| V_{IO} | Input Offset Voltage | I_{Os} | Output Sink Current |
| I_{IB} | Input Bias Current | t_p | Propagation Delay Time |

D/A CONVERTERS

The low-cost D/A converter described here finds wide usage in communications, control, and instrumentation systems. It provides a current output which is the

product of a digital word and an analog reference voltage. Device types specified to greater accuracy and resolution limits will be introduced in the near future.

DIGITAL-TO-ANALOG CONVERTERS

| Function | Compatibility | E_r (% - max) | I_O (mA - max) | t_S (ns - typ) | t_p (ns - max) | Case | Type | |
|--|---------------|--------------------|---------------------|---------------------|---------------------|------|---------------|------------|
| | | | | | | | -55 to +125°C | 0 to +70°C |
| 6-Bit Multiplying Digital-to-Analog Converters | MDTL, MTTL | 0.78 | 2.0 | 200 | 50 | 632 | MC1506 | MC1406 |

REGULATORS

Motorola offers a broad line of voltage regulators ranging from low-cost "Functional Circuits" to high-precision units. Regulators for positive and negative voltages are available as well as a unique floating

regulator, type MC1566L, whose maximum output voltage and current are limited only by the external pass transistor.

POSITIVE VOLTAGE REGULATORS

| V _O (Vdc) | | I _O (mA dc max) | V _{in} - V _O (Vdc) | | V _{in} (Vdc) | | I _B (mA dc max) | Reg _{in} (%V _O /V _{in} max) | Reg _L (%V _O max) | P _D (W max) | | Case | Type |
|--|-----|-------------------------------|---|-----|--------------------------|-----|-------------------------------|--|---|---------------------------|------------------------|----------------------|------------|
| min | max | | min | max | min | max | | | | T _C = 25°C | T _A = +25°C | | |
| -55 to +125°C Temperature Range | | | | | | | | | | | | | |
| 4.5 | 40 | 20 | 3.0 | 30 | 8.5 | 50 | 2.0 | 0.06 | 0.05 mV | — | 0.68 | 601 | MLM105 |
| 2.5 | 37 | 200 | 2.7 | 40 | 8.5 | 40 | 9.0 | 0.015 | 0.13 | 1.8 | 0.68 | 602A | MC1569* |
| | | 500 | | | | | | | 0.05 | 17.5 | 3.0 | | |
| 2.5 | 37 | 200 | 2.7 | 40 | 8.5 | 40 | 9.0 | 0.015 | 0.13 | 1.8 | 0.68 | 602A | MC1561 |
| | | 500 | | | | | | | 0.05 | 17.5 | 3.0 | | |
| 2.5 | 17 | 200 | 2.7 | 20 | 8.5 | 20 | 9.0 | 0.015 | 0.13 | 1.8 | 0.68 | 602A | MC1560 |
| | | 500 | | | | | | | 0.05 | 12 | 3.0 | | |
| 2.0 | 37 | 150 | 3.0 | 38 | 9.5 | 40 | 3.5 | 0.030 | 0.15 | — | 0.8 | 603-03, 632,607** | MC1723* ** |

-25 to +85°C Temperature Range

| | | | | | | | | | | | | | |
|-----|----|----|-----|----|-----|----|-----|------|---------|---|------|-----|--------|
| 4.5 | 40 | 20 | 3.0 | 30 | 8.5 | 50 | 2.0 | 0.06 | 0.05 mV | — | 0.68 | 601 | MLM205 |
|-----|----|----|-----|----|-----|----|-----|------|---------|---|------|-----|--------|

-10 to +75°C Temperature Range

| | | | | | | | | | | | | | |
|-----|----|-----|-----|---|-----|----|---|------|-----|---|-----|------|----------|
| 4.6 | 32 | 200 | 3.0 | — | 9.0 | 35 | — | 0.03 | 0.2 | — | 1.0 | 206A | MFC4060A |
| 4.6 | 32 | 200 | 3.0 | — | 9.0 | 35 | — | 0.03 | 0.2 | — | 1.0 | 643A | MFC6030A |
| 4.6 | 32 | 200 | 3.0 | — | 9.0 | 35 | — | 0.06 | 0.4 | — | 1.0 | 206A | MFC4062A |
| 4.6 | 32 | 200 | 3.0 | — | 9.0 | 35 | — | 0.06 | 0.4 | — | 1.0 | 643A | MFC6032A |
| 4.6 | 17 | 200 | 3.0 | — | 9.0 | 20 | — | 0.03 | 0.2 | — | 1.0 | 206A | MFC4063A |
| 4.6 | 17 | 200 | 3.0 | — | 9.0 | 20 | — | 0.03 | 0.2 | — | 1.0 | 643A | MFC6033A |
| 4.6 | 17 | 200 | 3.0 | — | 9.0 | 20 | — | 0.06 | 0.4 | — | 1.0 | 206A | MFC4064A |
| 4.6 | 17 | 200 | 3.0 | — | 9.0 | 20 | — | 0.06 | 0.4 | — | 1.0 | 643A | MFC6034A |

0 to +70°C Temperature Range

| | | | | | | | | | | | | | |
|-----|----|-----|-----|----|-----|----|-----|-------|---------|------|------|----------------|----------|
| 4.5 | 30 | 20 | 3.0 | 30 | 8.5 | 40 | 2.0 | 0.06 | 0.05 mV | — | 0.68 | 601 | MLM305 |
| 2.5 | 32 | 200 | 3.0 | 35 | 9.0 | 35 | 12 | 0.030 | 0.13 | 1.8 | 0.68 | 602A | MC1469* |
| | | 500 | | | | | | | 0.05 | 17.5 | 3.0 | | |
| 2.5 | 32 | 200 | 3.0 | 35 | 9.0 | 35 | 12 | 0.030 | 0.13 | 1.8 | 0.68 | 602A | MC1461 |
| | | 500 | | | | | | | 0.05 | 17.5 | 3.0 | | |
| 2.5 | 17 | 200 | 3.0 | 20 | 9.0 | 20 | 12 | 0.030 | 0.13 | 1.8 | 0.68 | 602A | MC1460 |
| | | 500 | | | | | | | 0.05 | 12 | 3.0 | | |
| 2.0 | 37 | 150 | 3.0 | 38 | 9.5 | 40 | 4.0 | 0.030 | 0.20 | — | 0.8 | 603-03, 632 | MC1723C* |

* Also available as nonencapsulated chip, use MCC prefix.

** Also available as nonencapsulated beam-lead device, use MCBC prefix, use MCB prefix for device in ceramic flat package.

FIXED OUTPUT POSITIVE VOLTAGE REGULATORS

| V _O (Vdc) | | I _O (mA dc max) | V _{in} - V _O (Vdc) | | V _{in} (Vdc) | | I _B (mA dc max) | Reg _{in} (mV max) | Reg _L (mV max) | P _D (W max) | | Case | Type |
|---|------|-------------------------------|---|-----|--------------------------|-----|-------------------------------|-------------------------------|------------------------------|---------------------------|------------------------|--------|-----------|
| min | max | | min | max | min | max | | | | T _C = +25°C | T _A = +25°C | | |
| -55 to +150°C Junction Temperature Range | | | | | | | | | | | | | |
| 4.7 | 5.3 | 1000 | 2.0 | 30 | 7.0 | 35 | 10 | 50 | 100 | 20 | 3.5 | 11 | MLM109K |
| -25 to +125°C Junction Temperature Range | | | | | | | | | | | | | |
| 4.7 | 5.3 | 1000 | 2.0 | 30 | 7.0 | 35 | 10 | 50 | 100 | 20 | 3.5 | 11 | MLM209K |
| 0 to +125°C Junction Temperature Range | | | | | | | | | | | | | |
| 4.8 | 5.2 | 1000 | 2.0 | 30 | 7.0 | 35 | 10 | 50 | 100 | 20 | 3.5 | 11 | MLM309K |
| 4.8 | 5.2 | 1500 | 2.0 | 30 | 7.0 | 35 | 8.0 | 100 | 100 | 15 | 2.0 | 199-04 | MC7805C * |
| 5.75 | 6.25 | 1500 | 2.0 | 29 | 8.0 | 35 | 8.0 | 120 | 120 | 10 | 2.0 | 199-04 | MC7806C * |
| 7.7 | 8.3 | 1500 | 2.5 | 27 | 10.5 | 35 | 8.0 | 160 | 160 | 10 | 2.0 | 199-04 | MC7808C * |
| 11.5 | 12.5 | 1500 | 2.5 | 23 | 14.5 | 35 | 8.0 | 240 | 240 | 10 | 2.0 | 199-04 | MC7812C * |
| 14.4 | 15.6 | 1500 | 2.5 | 20 | 17.5 | 35 | 8.0 | 300 | 300 | 10 | 2.0 | 199-04 | MC7815C * |
| 17.3 | 18.7 | 1000 | 3.0 | 17 | 21 | 35 | 8.0 | 360 | 360 | 10 | 2.0 | 199-04 | MC7818C * |
| 23 | 35 | 1000 | 3.0 | 16 | 27 | 40 | 8.0 | 480 | 480 | 10 | 2.0 | 199-04 | MC7824C * |

* For complete Data Sheet information please contact your Motorola salesman or distributor.

DEFINITIONS

| | | | |
|----------------------------------|-----------------------------------|-----------------------------|---|
| V _O | Output Voltage Range | I _B | Input Bias (Standby) Current |
| I _O | Output Current | Reg _{in} | Line Regulation Voltage |
| V _{in} - V _O | Input-Output Voltage Differential | Reg _L | Load Regulation Voltage |
| V _{in} | Input Voltage | TC _{V_O} | Temperature Coefficient of Output Voltage |
| V _{ref} | Reference Voltage | P _D | Power Dissipation |

REGULATORS (Continued)

NEGATIVE VOLTAGE REGULATORS

| V _O (Vdc) | | I _O (mA dc max) | V _{in} -V _O (Vdc) | | V _{in} (Vdc) | | I _{JB} (mA dc max) | Reg _{in} %V _O /V _{in} (max) | Reg _L (%V _O max) | P _D (W max) | | Case | Type |
|--|-----|----------------------------|---|-----|-----------------------|-----|-----------------------------|--|--|------------------------|------------------------|-------------|---------|
| min | max | | min | max | min | max | | | | T _C = 25°C | T _A = +25°C | | |
| -55 to +125°C Temperature Range | | | | | | | | | | | | | |
| -3.6 | 37 | 200 500 | -2.7 | 35 | -8.5 | -40 | 11 | 0.015 | 0.13 0.05 | 1.8 9.0 | 0.68 2.4 | 602A 614 | MC1563* |
| -0.015 | -40 | 20 | 2.0 | 50 | -8.0 | -50 | 5.0 | 0.1 | 0.05 | 1.8 | 0.68 | 603-02 | MLM104 |
| -25 to +85°C | | | | | | | | | | | | | |
| -0.015 | -40 | 20 | 2.0 | 50 | -8.0 | -50 | 5.0 | 0.1 | 0.05 | 1.8 | 0.68 | 603-02 | MLM204 |
| 0 to +70°C Temperature Range | | | | | | | | | | | | | |
| -3.8 | -32 | 200 500 | -3.0 | 40 | -9.0 | -35 | 14 | 0.030 | 0.13 0.05 | 1.8 9.0 | 0.68 2.4 | 602A 614 | MC1463* |
| -0.035 | -30 | 20 | 2.0 | 40 | -8.0 | -40 | 5.0 | 0.1 | 0.05 | 1.8 | 0.68 | 603-02 | MLM304 |

*Also available as nonencapsulated chip, use MCC prefix.

DUAL VOLTAGE REGULATORS

| V _{OR} [†] (Vdc) | | I _O (mA dc max) | V _{in} -V _O (Vdc) | | V _{in} (Vdc) | | I _{JB} (mA dc max) | Reg _{in} %V _O /V _{in} (max) | Reg _L (%V _O max) | P _D (W max) | | Case | Type |
|--|-------|----------------------------|---|-------|-----------------------|-----------|-----------------------------|--|--|------------------------|-----------------------|--------|------|
| min | max | | min | max | min | max | | | | T _C = 25°C | T _A = 25°C | | |
| -55 to +125°C Temperature Range | | | | | | | | | | | | | |
| ±14.8 | ±15.2 | 100 | 2.0 | ±17.2 | ±30 | +4.0,-3.0 | 0.006 | 0.07 | 2.1 2.5 9.0 | 0.8 1.0 2.4 | 603-03 632 614 | MC1568 | |
| 0 to +75°C Temperature Range | | | | | | | | | | | | | |
| ±14.5 | ±15.5 | 100 | 2.0 | ±17.5 | ±30 | +4.0,-3.0 | 0.01 | 0.07 | 2.1 2.5 9.0 | 0.8 1.0 2.4 | 603-03 632 614 | MC1468 | |

†Preset Voltage Range; range is adjustable by adding external resistors from ±14.5 to ±20 Vdc.

SPECIAL-PURPOSE REGULATORS

| V _O | | Reg _{in} (max) | Reg _L (max) | Current Regulation | P _D (W max) | Case | Type | Features |
|--|-------|-------------------------|------------------------|--------------------|------------------------|------|--------|---|
| min | max | | | | | | | |
| -55 to +125°C Temperature Range | | | | | | | | |
| 0 | 1000* | 0.01% +1mV | 0.01% +1mV | 0.1% +1mA | 0.300 | 632 | MC1566 | A floating regulator, can be used as a voltage controlled current source. |
| 0 to +75°C Temperature Range | | | | | | | | |
| 0 | 1000* | 0.03% +3mV | 0.03% +3mV | 0.02% +1mA | 0.360 | 632 | MC1466 | A floating regulator, can be used as a voltage controlled current source. |

*Limited only by the characteristics of the external series pass transistor.

HIGH FREQUENCY AMPLIFIERS

Motorola's high-frequency amplifiers simplify the design of receivers and signal processors. Many offer

AGC capability or several gain options to provide extra design flexibility.

HIGH FREQUENCY AMPLIFIERS

| Bandwidth (MHz) | V _{OS} (V _{p-p}) | z _{in} (k Ω @ kHz) | | z _o (Ω @ kHz) | | A _V S (dB) | G _p @ 60 MHz (dB) | Diff. Input and Output | AGC | V _{CC} , V _{EE} (V _{dc}) | Case | Type | |
|--|-------------------------------------|--------------------------------------|-------------------|------------------------------------|-------|-----------------------|------------------------------|------------------------|-----|--|----------------|---------------|------------|
| | | 6.0 | 20 | 35 | 20 | | | | | | | -55 to +125°C | 0 to +75°C |
| dc to 40 | 4.5 | 6.0 | 20 | 35 | 20 | 90 (fixed) | — | Yes | No | ±6.0 | 601 | MC1510 | MC1410 |
| dc to 75 | 2.5 | 10 | 50 | 25 | 50 | 18 (fixed) | — | Yes | Yes | ±5.0 | 602A, 607, 632 | MC1545 | MC1445 |
| 22 min | 6.0 | 1.8 | 1.0 M | 100 k | 1.0 M | 26 (AGC = 0) | 25 | No | Yes | +6.0 | 602B, 606 | MC1550 | — |
| 40 @ A _v = 34 dB 35 @ A _v = 40 dB | 4.2 | 10 | 100 | 16 | 100 | 30 - 40 (fixed) | — | No | No | +6.0 | 602B | MC1552 | — |
| 35 @ A _v = 46 dB 15 @ A _v = 52 dB | 4.2 | 10 | 100 | 16 | 100 | 46 - 52 (fixed) | — | No | No | +6.0 | 602B | MC1553 | — |
| 100 @ A _v = 4.0 dB 60 @ A _v = 25 dB | 7.0 | 3.0 | 1.0 M | 100 k | 1.0 M | 44 (AGC = 0) | 45 | Yes | Yes | +12 | 601 | MC1590 | — |
| 40 @ A _v = 52 dB 90 @ A _v = 40 dB 120 @ A _v = 20 dB | 4.0 | 4.0 30 250 | 1.0 1.0 1.0 | 20 | 1.0 | 52 40 20 | — | Yes | No | ±6.0 | 603-02 632 | MC1733 | MC1733C |

3

SPECIAL-PURPOSE CIRCUITS

The linear-integrated-circuits listed in this section were developed by Motorola for the system design engineer to fill special-purpose requirements as indicated

by the subheadings. Temperature ranges and package availability are also tailored to provide versatility.

MULTIPLIERS

| Function | Linearity Error (typ) | Input Voltage Range (Vdc min) | Case | Type | |
|--|----------------------------------|-------------------------------|------|---------------|------------|
| | | | | -55 to +125°C | 0 to +70°C |
| A four-quadrant multiplier designed to operate with ±15-volt supplies; has internal level-shift circuitry and voltage regulator. | ±0.3% | ±10 | 620 | MC1594 | — |
| | ±0.5% | ±10 | 620 | — | MC1494 |
| Applications include multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control. | X Input = 0.5% Y Input = 1.0% | ±10 | 632 | MC1595* | — |
| | X Input = 1.0% Y Input = 2.0% | ±10 | 632 | — | MC1495* |

*Also available as a nonencapsulated chip. use MCC prefix.

BALANCED MODULATOR/DEMODULATOR

| Function | Carrier Suppression dB @ f (MHz) (typ) | | Common-Mode Rejection (dB typ) | Case | Type | |
|--|--|----|--------------------------------|-----------|--------|--------|
| | 65 | 50 | | | 0.5 | 10 |
| Balanced modulator/demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). | 65 | 50 | 85 | 602A, 632 | MC1596 | MC1496 |

LOW FREQUENCY CIRCUITS

| Function | Output Power (W typ) | Voltage Gain — typ (V/V typ) | Total Harmonic Distortion (% typ) | Case | Type | |
|---|----------------------|------------------------------|-----------------------------------|------|---------------|------------|
| | | | | | -55 to +125°C | 0 to +70°C |
| A power amplifier device capable of single or split supply operation. | 1.0 | 10, 18, 36 | 0.4 | 602B | MC1554 | MC1454 |

POWER CONTROL CIRCUITS

| Function | Temperature | Case | Type |
|---|--------------|------|---------|
| Zero voltage switch for use in ac power switching with output capable of triggering triacs. | -10 to +75°C | 644A | MFC8070 |

POWER DRIVERS

| Function | BVCEO (Vdc) | IO (A typ) | hFE (typ) | ton/toff (ns) | Temperature | Case | Type |
|---|-------------|------------|-----------|---------------|---------------|------|---------|
| Darlington hybrid power driver | 30 typ | — | 1000 | 350/450 max | -55 to +125°C | 628 | MCH2005 |
| Dual power driver for use with hammer, solenoids, relays, lamps, paper tape punches, etc. | 120 min | 6.0 | — | 260/1800 typ | 0 to +70°C | 685 | MCH2890 |

CONSUMER APPLICATION SELECTOR GUIDE

...reflecting Motorola's continuing commitment to semiconductor products necessary for consumer system designs. The tabulation contains data for a large number of components designed principally for entertainment

product applications. It is arranged to simplify first-order of linear integrated circuit device lineups to satisfy primary functions for Television, Audio, Radio, Automotive and Organ applications.

TELEVISION CIRCUITS

SOUND

| Function | Features | Case | Type |
|--|---|---------|--------|
| Sound IF, Detector, Limiter, Audio Preamplifier | 80 μ V, 3 dB Limiting Sensitivity, 3.5 V(RMS) Output, Sufficient for Single Transistor Output Stage | 646,647 | MC1351 |
| Sound IF Detector | Interchangeable with ULN2111A | 646,647 | MC1357 |
| Sound IF Detector, DC Volume Control, Preamplifier | Excellent AMR, Interchangeable with CA3065 | 646,647 | MC1358 |

VIDEO

| | | | |
|--|---|------------|--------|
| 1st and 2nd Video IF Amplifier | IF Gain @ 45 MHz – 60 dB typ AGC Range – 70 dB min | 626 | MC1349 |
| | IF Gain @ 45 MHz – 46 dB typ, AGC Range – 60 dB min | 626 | MC1350 |
| 1st and 2nd Video IF, AGC Keyer and Amplifier | IF Gain @ 45 MHz – 53 dB typ, AGC Range – 65 dB min, "Forward AGC" Provided for Tuner | 646,647 | MC1352 |
| | Same as MC1352, with Opposite AGC for Tuner | 646 | MC1353 |
| 3rd IF and Video Detector | Low-Level Detection, Low Harmonic Generation, Reduced Circuit Cost and Complexity, Reduced Shielding | 626 | MC1330 |
| AGC Keyer, AGC Amplifier, Noise Gate, Sync Separator | High-Quality Noise Gate, One IF AGC Output and Two Tuner AGC Outputs, Adjustable AGC Delay | 646 | MC1345 |
| Automatic Fine Tuning | High Gain AFT System, Interchangeable with CA3064 | 646 686 | MC1364 |

CHROMA

| | | | |
|---|--|-------------------|--------|
| Chroma IF Amplifier and Subcarrier System | Includes Complete Chroma IF, AGC, dc Gain and Tint Controls, Injection Locked Oscillator, Low Peripheral Parts Count | 646 | MC1398 |
| Chroma Subcarrier System | Interchangeable with CA3070, APC Chroma Reference System | 648 | MC1370 |
| Chroma IF Amplifier | Interchangeable with CA3071, Automatic and Manual Gain Control | 646 | MC1371 |
| Chroma Demodulators | Similar to MC1328 but with Luminance and Blanking Inputs, Internal Matrix Provides RGB Outputs | 646,647 | MC1326 |
| | Industry Standard Demodulator, Low Differential Output dc Drift | 603-02 646,647 | MC1328 |
| Dual Chroma Demodulator | Dual Doubly Balanced Demodulator with RGB Output Matrix and PAL Switch | 646,647 | MC1327 |

AUDIO CIRCUITS

PREAMPLIFIERS

| Function | V _{CC} (Vdc - max) | A _{vol} (dB min) | THD (% typ) | z _o (Ohms typ) | Case | Type |
|-----------------------------|--------------------------------|------------------------------|----------------|------------------------------|------|---------|
| Dual Preamplifier | ±15 | 80 | 0.1 | 100 | 632 | MC1303 |
| Dual Low-Noise Preamplifier | 16 | 63 | 0.1 | 100 | 646 | MC1339 |
| Low-Noise Preamplifier | 33 | 80 | 0.1 | 100 | 644A | MFC8040 |

DRIVERS

| Function | V _{CC} (Vdc) | Drive Current (mA) | A _{vol} (dB) | Case | Type |
|-----------------------|--------------------------|-----------------------|--------------------------|------|----------|
| Class A Audio Driver | 18 | 30 min | 42 min | 206A | MFC4050 |
| Class B Audio Drivers | 35 | 150 peak | 89 typ | 644A | MFC8020A |
| | 20 | 150 peak | 87 typ | 644A | MFC8021A |
| | 45 | 150 peak | 90 typ | 644A | MFC8022A |

POWER AMPLIFIERS

| Function | P _O (Watts) | V _{CC} (Vdc max) | i _{in} @ rated P _O (mV - max) | P _D (mA - max) | R _L (Ohms) | Case | Type |
|------------------------|---------------------------|------------------------------|---|------------------------------|--------------------------|------|----------|
| Audio Power Amplifiers | 0.5 | 12 | 3.0 | 4.0 | 8.0 | 626 | MC1306 |
| | 0.25 | 12 | 3.0 | 3.5 | 16 | 206A | MFC4000B |
| | 1.0 | 20 | 100 | 5.0 | 16 | 643A | MFC6070 |
| | 1.0 | 22 | 10 | 10 | 8.0 | 644A | MFC8010 |
| | 2.0 | 24 | 200 | 12 | 16 | 641 | MFC9020 |
| | | | | | | | |

RADIO CIRCUITS

IF AMPLIFIERS

| Function | Gain @ 10.7 MHz (dB - typ) | 3 dB Limiting @ 10.7 MHz (mV(RMS) typ) | AMR (dB - typ) | Recovered Audio Output Δf = 75 kHz (mV(RMS)) | Power Supply (Volts - max) | Case | Type |
|--------------------------------------|----------------------------------|--|-------------------|---|----------------------------------|---------|----------|
| IF Amplifier | 58 | - | - | - | 18 | 626 | MC1350 |
| Limiting FM-IF Amplifier | - | 0.175 | 60 | 690 | 18 | 646,647 | MC1355 |
| Limiting IF Ampl/Quadrature Detector | 53 | 0.600 | 45 | 480 | 16 | 646,647 | MC1357 |
| IF Amplifier | 42 | 0.4 | - | - | 18 | 206A | MFC4010A |
| IF Amplifier, Nonsaturating Limiter | 40 | 60 | 50 | 500 | 20 | 643A | MFC6010 |

DECODERS

| Function | Channel Separation (dB - typ) | THD (% - typ) | Stereo - Indicator Lamp Driver (mA - max) | Features | Case | Type |
|------------------------------|-------------------------------------|------------------|---|------------------------------|---------|--------|
| FM Multiplex Stereo Decoders | 45 | 0.5 | 40 | Audio Muting | 646 | MC1304 |
| | 45 | 0.5 | 40 | Audio Muting | 646 | MC1305 |
| | 40 | 0.5 | 40 | - | 646/647 | MC1307 |
| | 40 | 0.3 | 75 | Coilless Operation | 646 | MC1310 |
| Four-Channel SQ Decoders | 45 | 0.1 | - | V _{CC} = 20 Vdc nom | 646 | MC1312 |
| | 45 | 0.25 | - | V _{CC} = 12 Vdc nom | 646 | MC1313 |

AUTOMOTIVE CIRCUITS

OPERATIONAL AMPLIFIER

| Function | V _{CC} Range (Vdc) | A _{vol} (V/mV - typ) | I _{IB} (μA - max) | Unity Gain Bandwidth (MHz - typ) | R _{in} (MegΩ typ) | Case | Type |
|----------------------------|-----------------------------------|----------------------------------|-------------------------------|--|-------------------------------|------|--------|
| Quad Operational Amplifier | 4.0 to 28 | 2.0 | 0.3 | 4.0 | 1.0 | 646 | MC3301 |

COMPARATOR

| Function | V _{CC} Range (Vdc) | V _{IDR} (Vdc) | I _{IB} (μA - max) | Output Leakage Current (mA - max) | Sink Current | Case | Type |
|-----------------|-----------------------------------|---------------------------|-------------------------------|---|--------------|------|--------|
| Quad Comparator | 2.0 to 28 | ±V _{CC} | 0.5 | 10 | 6.0 | 646 | MC3302 |

CONSUMER APPLICATION SELECTOR GUIDE (Continued)

ORGAN CIRCUITS

FREQUENCY DIVIDERS

| Function | V _{CC} Range (V _{dC}) | f _{Tog} (MHz - typ) | V _{OH} (V _{dC} - min) | Case | Type |
|-----------------------|--|------------------------------|---|------|---------|
| Toggle Flip-Flop | 4.0 to 16 | 1.0 | 15.5 | 206A | MFC4040 |
| Dual Toggle Flip-Flop | 4.0 to 16 | 1.0 | 15.5 | 643A | MFC6020 |

RHYTHM

| | | | | | |
|----------------------------------|-----------|-----|------|------|---------|
| Dual Toggle Flip-Flop with Reset | 4.0 to 16 | 1.0 | 15.5 | 643A | MFC6050 |
| 3-Input AND Gate | 4.0 to 16 | - | 15 | 643A | MFC6060 |
| R-S Flip-Flop | 4.0 to 16 | 1.0 | 15.5 | 643A | MFC6080 |
| J-K Flip-Flop | 4.0 to 16 | 1.0 | 15.5 | 644A | MFC8050 |

ATTENUATOR

| Function | V _{CC} Range (V _{dC}) | THD (% - typ) | A _V (dB - typ) | Attenuation Range (dB - typ) | Case | Type |
|-----------------------|--|---------------|---------------------------|------------------------------|------|---------|
| Electronic Attenuator | 9.0 to 18 | 0.6 | 13 | 90 | 643A | MFC6040 |

3

Preview of Upcoming Products

The products described in this section are presently under development and are expected to be introduced soon. All specifications are tentative. Additional information on these devices and their availability may be obtained from your Motorola representative.

INDUSTRIAL PRODUCTS

Most of the traditional linear IC types are designed for industrial applications. Several new op amps and a timing circuit are discussed below. These devices further the diversity of Motorola's product line-up.

MLM108A Operational Amplifier

The MLM108A series of high precision operational amplifiers is designed to provide high input impedance, low input bias currents and low offset voltages, thus making it possible to eliminate offset adjustments in most applications. The devices operate on supply voltages from ± 2 V to ± 20 V and have sufficient supply rejection to use unregulated supplies. Feed forward compensation techniques can be applied to provide increased slew rates for maximized performance in high speed Sample-and-Hold circuits and precision high-speed summing amplifiers.

FEATURES:

- Offset voltage guaranteed less than 0.5 mV
- Low input offset current — 400 pA maximum
- Low input bias currents — 3.0 nA maximum
- Guaranteed maximum input offset drift 5 $\mu\text{V}/^\circ\text{C}$

MC1555 Adjustable Timer

The MC1555 is a highly stable timing circuit designed to provide accurate time delays or oscillations. Both trigger and reset provisions are available for increased flexibility. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor.

FEATURES:

- Timing from microseconds through hours
- Output can source or sink 200 mA
- TTL compatible
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Temperature stability of 0.005% per $^\circ\text{C}$
- Normally on and normally off output

MC1776 Programmable Low Power Operational Amplifier

The MC1776 offers the user high-input impedance, low-power supply currents, and low-input noise over a wide range of operating supply voltages. Power consumption, input current, and noise resulting from both input voltage and current can be optimized by the selection of a single resistor or current source that sets the chip quiescent currents for microwatt power consumption.

FEATURES:

- Micropower consumption
- ± 1.2 V to ± 18 V operation
- Low input bias currents
- High slew rate
- Offset null capability

MC1741S Operational Amplifier

The MC1741S is an internally compensated, high-performance monolithic operational amplifier designed to provide a wide power bandwidth. It is similar in other electrical characteristics and pin compatible with the MC1741. Application possibilities include A/D converters, oscillators, active filters or general purpose amplifiers.

FEATURES:

- 10 V/ μs slew rate
- Pin compatible with MC1741 op amp
- 500 kHz power bandwidth

CONSUMER PRODUCTS

The rapid trend to ICs in television, stereo and FM radio equipment has permitted the development of many new, advanced ICs for these product types. Particularly in television the diversity of available functions is rapidly expanding. A number of device types which will be introduced in the near future are summarized below.

MC1391 TV Horizontal Processor

The MC1391 TV horizontal processor packs the phase detector, oscillator and pre-driver functions into a single, convenient 8-lead plastic package. The new unit provides the entire low-level horizontal signal processing function and may be used with either transistor or vacuum tube output stages. This device is one of the first inroads of ICs into the television deflection circuitry.

FEATURES:

- Internal shunt regulator
- Preset Hold control capability
- ± 300 Hz typical pull-in range
- Balanced phase detector
- Variable output duty cycle for driving tube or transistor
- Low thermal frequency drift
- Small static phase error

MC1359 TV Sound System

The MC1359 is a complete sound system for a television receiver. It includes the IF amplifier, detector, electronic volume control, and audio amplifier. The IC provides two watts of audio output. All this is packed into a single plastic package with two heat dissipating tabs.

The dc voltage-controlled volume attenuator saves the necessity of long lengths of shielded cable between the volume control and the audio amplifier circuitry. This advanced system provides 80 dB of audio attenuation range.

FEATURES:

- Excellent AM rejection
- DC volume control with 80 dB typical attenuation range
- Signal to noise ratio = 63 dB typical
- Few external components required

MC1344 TV Signal Processor

The MC1344 TV signal processor provides a collection of common television processing functions. It combines the sync separator, advanced noise inverter, AGC comparator and both positive and negative-going RF AGC delay amplifier into a single package.

This device is an improved version of the MC1345. It features greater thermal noise performance and modified negative RF amplifier AGC response. A number of important features are tabulated below.

FEATURES:

- Video internally delayed for total noise inversion
- Low impedance, noise cancelled sync output
- Refined AGC gate
- Small IF AGC output change during RF AGC internal
- Positive and negative going RF AGC outputs
- Noise threshold may be externally adjusted
- Time constants for sync separator externally chosen
- Stabilized for $\pm 10\%$ supply voltage variations

4

MC1315 CBS SQ Logic Circuits

The MC1315 provides the basic logic function for enhancing the front to back separation in the CBS SQ four channel decoding system. The new IC is designed to interface with the MC1312 decoder and MC1314 balance control unit. The MC1315 provides variable logic enhancement control and supplies the dc gain control and balance signals to the MC1314.

This unit extends the performance of the basic SQ system to the levels desired for top-of-the-line systems.

FEATURES:

- Provides logic enhancement to extend front to back separation to 12 dB
- Low external parts count
- Provisions for enhancement controls
- Provides dc gain control signals to the MC1314

MC1314 CBS SQ Logic Circuits

The MC1314 is a gain control and balance adjustment unit for use with the CBS SQ system decoders. It consists of four amplifiers, with the gain of each being adjustable by varying a dc voltage. Thus with four variable resistors, the master volume and L_F/R_F , L_B/R_B and F/B balance may be controlled.

The unit also has inputs which may be connected to the MC1315 logic enhancement unit to provide increased front to back separation. This feature is highly desirable in high performance four channel stereo systems.

FEATURES:

- DC controlled gain
- Four separate audio preamplifiers
- Compatible with MC1312 decoder and MC1315 logic enhancement unit

MC1311 FM Stereo Demodulator

The MC1311 phase locked loop stereo demodulator is an modified version of the popular MC1310 type. The new circuit provides emitter follower outputs and 6 dB of gain. It retains the low external parts count (no inductors), simplified alignment and high performance of its predecessor.

The new IC also contains a stereo indicator lamp driver which incorporates 6 dB of hysteresis to avoid flickering due to noise.

FEATURES:

- Emitter follower outputs
- Requires no inductors
- Low external part count
- Includes 6 dB typical gain

MC1375 FM IF Circuit

Combining several functions required in solid-state FM receivers, the MC1375 provides the IF amplifier, limiter, FM detector and audio preamplifier in a single 14-lead package. The unit requires a minimum of external components.

The IF amplifier/limiter section provides excellent AM rejection and uses an internal zener diode voltage regulator. The detector is a differential peak design which promotes simplified single-coil alignment. The audio preamplifier supplies a voltage gain of ten.

FEATURES:

- Good sensitivity: input limiting voltage (Knee) = 250 μ V typical
- Excellent AM rejection: 55 dB typical at 10.7 MHz
- Internal zener diode regulation for the IF amplifier section
- Low harmonic distortion
- Differential peak detection: permits simplified single-coil timing
- Audio preamplifier voltage gain: 21 dB typical

LINEAR DIGITAL INTERFACE PRODUCTS

The rapid expansion in computer-control, data communications and digital instrumentations has led to the development of a myriad of new analog-digital interface ICs. A few of the most recent developments in Motorola's efforts in this field will be discussed below.

MC1504 Quad Current Switch

The MC1504 is a monolithic quad current switch designed for an optimum combination of accuracy, switching speed and stability as required in precision D/A converters. Several units may be cascaded with a 16:1 interquad attenuation to make complete converters with up to 12 bit accuracy. The current switch is coupled with an external ladder network to produce the D/A function. A reference transistor is included for use in temperature compensating circuitry.

FEATURES:

- $\pm 0.01\%$ maximum nonlinearity
- 40 ns switching time
- 200 ns settling time
- 1 ppm/ $^{\circ}\text{C}$ temperature coefficient

MC1507 A/D Converter Subsystem

The MC1507 is a monolithic subsystem designed for use in A/D converters and instrumentation applications. It consists of a high slew rate, wide-bandwidth op amp and a dual threshold voltage comparator. The comparator features low input currents and separate outputs for both thresholds. A very economical tracking A/D system can be assembled using the MC1507 in conjunction with the MC1508 8-bit D/A converter and a TTL Up/Down counter.

FEATURES:

- Low input offset voltage
- Standard power supply: $\pm 15\text{ V}$ and $+5\text{ V}$
- Differential reference input sets both thresholds
- Op amp has 20 MHz bandwidth in unity gain mode

MC1508 8-Bit D/A Converter

The MC1508 monolithic 8-bit D/A converter is designed for use in applications requiring an output current which is the linear product of an analog input voltage and an 8-bit digital word. It is similar to the MC1506 6-bit D/A converter in basic design except that the new unit has non-inverting logic inputs and a faster reference amplifier for multiplying applications. An additional pin has been provided for extending the output voltage swing in the negative direction to -5 V .

FEATURES:

- Fast settling time
- Non-inverting operation
- Low power consumption
- Maximum error of $\pm 0.19\%$

MLMIII Series Voltage Comparator

The MLMIII voltage comparator is designed to operate over a wide range of supply voltages. The comparator may be operated from ± 15 V supplies as used with op amps or a single +5 V supply as used with digital logic systems. Both the inputs and outputs of the MLMIII can be isolated from system ground and the output can drive loads referenced to ground, the positive or the negative supply. Offset balancing and strobe capability are provided and outputs can be Wire-ORed.

FEATURES:

- May operate from single 5 V supply
- Input current: 150 nA maximum
- Offset current: 20 nA maximum
- Differential input voltage range: ± 30 V

MMH0026 Dual MOS Clock Driver

The MMH0026 is a monolithic, high-speed, two-phase MOS clock driver. The device accepts standard DTL/TTL inputs and converts them to MOS logic levels. It has the ability to drive large capacitive loads. The MMH0026 is intended for applications in which the output pulse width is logically controlled; i.e. the output pulse width is equal to the input pulse width.

FEATURES:

- Fast rise and fall times — 20 ns with 1000 pF load
- 20 V output swing
- ± 1.5 amps output current drive
- Drives to within 0.4 V of ground for RAM address drive applications

MC75452-MC75453-MC75454 Dual Peripheral Drivers

The MC75452, 453, 454 series of dual peripheral drivers are designed for use as general purpose interface functions in DTL/TTL systems. The drivers consist of two logic gates whose outputs are internally connected to the bases of two high current, high voltage NPN transistors. Typical applications include relay and lamp drivers, power drivers, MOS and memory drivers. The MC75452 is a positive NAND function, the MC75453 is a positive OR function while the MC75454 is a positive NOR function.

FEATURES:

- 300 mA output drive capability
- High output breakdown voltage: $BV_{CER} = 30$ V minimum
- DTL/TTL compatible inputs

MC75491, MC75492 MOS to VLED Segment & Digit Drivers

The MC75491 and MC75492 are monolithic drivers for use with visible light emitting diode (VLED) displays. They were designed to provide the interface between MOS logic and common cathode VLEDs in serially addressed, multi-digit displays. This time multiplexed system using a segment address and digit scan method of VLED drive minimizes the number of drivers required. The MC75491 devices have a separate connection for the emitter of each output transistor while the MC75492 devices have the emitters internally connected to the V_{DD} terminal.

FEATURES:

MC75491

- 50 mA source or sink current capability
- Low input current for MOS compatibility
- Low stand-by power
- Quad high-gain Darlington circuits

MC75492

- 250 mA sink current capability
- Low input current for MOS capability
- Low stand-by power
- Hex high-gain Darlington Circuits

LINEAR

INTEGRATED CIRCUITS

INTERCHANGEABILITY GUIDE

This interchangeability guide describes equivalent circuits in two ways: (1) the "Direct Replacement" which is both electrically and mechanically a direct replacement; and, (2) the "Functional Equivalent" that is generally superior in electrical characteristics, however may differ in package dimensions or lead configurations. When a functional equivalent circuit is used for a replacement, the specific data sheet should be consulted.

Packaging availability information for each Motorola device is listed in the Linear Application Selector Guides section and also appears on the individual data sheet for the device. Exact outline dimensions are shown in the Packaging Information section of this data book.

MANUFACTURERS REFERENCED

Fairchild Semiconductor
National Semiconductor
RCA
Signetics
Texas Instruments

FAIRCHILD INSTRUMENTS TO MOTOROLA

| FAIRCHILD DEVICE NUMBER | | MOTOROLA DIRECT EQUIVALENT | MOTOROLA FUNCTIONAL EQUIVALENT | FAIRCHILD DEVICE NUMBER | | MOTOROLA DIRECT EQUIVALENT | MOTOROLA FUNCTIONAL EQUIVALENT | |
|-------------------------|--------------|----------------------------|--------------------------------|-------------------------|--------------|----------------------------|--|----------|
| DEVICE TYPE | ORDER CODE | | | DEVICE TYPE | ORDER CODE | | | |
| μA702 | U3F 7702 312 | MC1712F | | μA748 | U3F 7748 312 | MC1748F | | |
| | U3F 7702 313 | MC1712CF | | | U3F 7748 313 | MC1748CF | | |
| | U5B 7702 312 | MC1712G | | | U5B 7748 312 | MC1748G | | |
| | U5B 7702 393 | MC1712CG | | | U5B 7748 393 | MC1748CG | | |
| | U6A 7702 312 | MC1712L | | | U6A 7748 312 | MC1748L | | |
| | U6A 7702 393 | MC1712CL | | | U6A 7748 393 | MC1748CL | | |
| μA703 | U5D 7703 312 | | MFC6010 MFC6010 MFC6010 | μA754 | U5E 7754 393 | | MC1355P MC1355P MC1350P MC1350P | |
| | U5D 7703 393 | | | | U6A 7754 394 | | | |
| | U5D 7703 394 | | | | U6A 7757 312 | | | |
| μA709 | U3F 7709 311 | MC1709F | | μA757 | U6A 7757 393 | | | |
| | U3F 7709 312 | MC1709F | | | U6A 7757 312 | | | |
| | U3F 7709 313 | MC1709CF | | | U6A 7757 393 | | | |
| | U5B 7709 311 | MC1709G | | | μA767 | U6A 7780 394 | | MC1307P |
| | U5B 7709 312 | MC1709G | | | μA780 | U6A 7781 394 | | MC1370P |
| | U5B 7709 393 | MC1709CG | | | μA781 | U6A 7795 312 | | MC1371P |
| | U6A 7709 311 | MC1709L | | | μA795 | U6A 7795 312 | | MC1595L |
| | U6A 7709 312 | MC1709L | | | μA796 | U6A 7795 393 | | MC1595CL |
| | U6A 7709 393 | MC1709CL | | | | U5E 7796 312 | | MC1596G |
| | μA710 | U3F 7710 312 | | | MC1710F | | | μA7524 |
| U3F 7710 313 | | MC1710CF | U7B 7524 392 | MC7524 | | | | |
| U5B 7710 312 | | MC1710G | U7B 7525 393 | MC7524 | | | | |
| U5B 7710 393 | | MC1710CG | μA7805 | UGH 7805 393 | MC7805CP | | | |
| U6A 7710 312 | | MC1710L | μA7806 | UGH 7806 393 | MC7806CP | | | |
| U6A 7710 393 | | MC1710CL | μA7808 | UGH 7808 393 | MC7808CP | | | |
| μA711 | U3F 7711 312 | MC1711F | | μA7812 | UGH 7812 393 | MC7812CP | | |
| | U3F 7711 313 | MC1711CF | | | μA7815 | UGH 7815 393 | | MC7815CP |
| | U5F 7711 312 | MC1711G | | | μA7818 | UGH 7818 393 | | MC7818CP |
| | U5F 7711 393 | MC1711CG | | | μA7824 | UGH 7824 393 | | MC7824CP |
| | U6A 7711 312 | MC1711L | | | μA9614 | U4L 9614 51X | | |
| | U6A 7711 393 | MC1711CL | | | | U4L 9614 59X | | |
| μA719 | U5F 7719 312 | | MC1357 MC1357 | μA9615 | U7B 9614 51X | | MC1582L MC1582L MC1582L MC1582L | |
| | U5F 7719 393 | | | | U7B 9614 59X | | | |
| μA723 | U5R 7723 312 | MC1723G | | μA9620 | U4L 9615 51X | | MC1584L MC1584L MC1584L MC1584L | |
| | U5R 7723 393 | MC1723CG | | | U4L 9615 59X | | | |
| | U6A 7723 312 | MC1723L | | | U7B 9615 51X | | | |
| μA729 | U6A 7723 393 | MC1723CL | | μA9621 | U7B 9615 59X | | MC1580L MC1580L MC1580L MC1580L | |
| | U6A 7729 394 | MC1305P | | | U31 9620 51X | | | |
| μA732 | U6A 7732 394 | MC1304P | | μA9622 | U31 9620 59X | | MC1584L MC1584L MC1584L MC1584L | |
| | μA733 | U3F 7733 312 | | | MC1733F | U6A 9620 51X | | |
| U3F 7733 313 | | MC1733CF | U6A 9620 59X | | | | | |
| U5F 7733 312 | | MC1733G | μA9622 | U31 9622 51X | | | | |
| U5F 7733 393 | | MC1733CG | | U31 9622 59X | | | | |
| U6A 7733 312 | | MC1733L | U6A 9622 51X | | | | | |
| U6A 7733 393 | | MC1733CL | U6A 9622 59X | | | | | |
| μA739 | U6A 7739 312 | MC1303P | | CA3064 | CA 3064/5A | MC1364G | MC1358PQ MC1375P | |
| | U6A 7739 393 | MC1303P | | | CA3065 | CA 3065/7F | | |
| μA741 | U3F 7741 312 | MC1741F | | CA3075 | CA 3075/ | | | |
| | U3F 7741 313 | MC1741CF | | | | | | |
| | U5B 7741 312 | MC1741G | | | | | | |
| | U5B 7741 393 | MC1741CG | | | | | | |
| | U6A 7741 312 | MC1741L | | | | | | |
| | U6A 7741 393 | MC1741CL | | | | | | |
| μA746 | U6T 7741 393 | MC1741CP2 | | μA747 | U5F 7747 312 | | MC1328P | |
| | U9T 7741 393 | MC1741CP1 | | | U5F 7747 393 | | | |
| μA747 | U6A 7746 394 | MC1328P | | μA747 | U6W 7747 312 | | MC1558G MC1458G MC1558L MC1558CL MC1558L MC1558CL | |
| | μA747 | U5F 7747 312 | | | | U6W 7747 393 | | |
| | | U5F 7747 393 | | | | U7A 7747 312 | | |
| | | U6W 7747 312 | | | | U7A 7747 393 | | |
| | | U6W 7747 393 | | | | | | |
| | | U7A 7747 312 | | | | | | |
| U7A 7747 393 | | | | | | | | |

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NATIONAL TO MOTOROLA

| NATIONAL TYPE NUMBER | MOTOROLA DIRECT REPLACEMENT | MOTOROLA FUNCTIONAL EQUIVALENT | NATIONAL TYPE NUMBER | MOTOROLA DIRECT REPLACEMENT | MOTOROLA FUNCTIONAL EQUIVALENT |
|---|---|--|--|--|--|
| LH101F LH101H LH201H LM100H LM101H | MC1748G | MC1741F MC1741G MC1741G MC1723G | LM710CN LM711H LM711CH LM723D LM723H | MC1710CP MC1711G MC1711CG MC1723L MC1723G | |
| LM101AH LM102H LM104H LM105H LM106H | MLM101AG MLM110G MLM104G MLM105G | MC1710G | LM723CD LM723CH LM733D LM733H LM733CD | MC1723CL MC1723CG MC1733L MC1733G MC1733CL | |
| LM107H LM108H LM108AH LM109K LM110H | MLM107G MLM109K MLM110G | MC1556G MC1556G | LM733CH LM741D LM741F LM741H LM741CD | MC1733CD MC1741L MC1741F MC1741G MC1741CL | |
| LM112H LM118H LM200H LM201H LM201AH | MC1748CG MLM201AG | MC1556G MC1539G MC1723CG | LM741CH LM741CN LM741CN-14 LM746N LM747D | MC1741CG MC1741CP1 MC1741CP2 MC1328P MC1747L | |
| LM202H LM204H LM205H LM206G LM207H | MLM210G MLM204G MLM205G MLM207G | MC1710CG | LM747CC LM748H LM748CH LM1303N LM1304N | MC1747CL MC1748G MC1748CG MC1303L MC1304P | |
| LM208H LM209K LM210H LM212H LM218H | MLM209K MLM210G | MC1456G MC1456G MC1439G | LM1305N LM1310N LM1307N LM1351N | MC1305P MC1310P MC1307P MC1351P | |
| LM300H LM301AH LM301AN LM302H LM304H | MLM301AG MLM301API MLM310G MLM304G | MC1723CG | LM1414J LM1414N LM1458H LM1458N LM1489J | MC1414L MC1414L MC1458G MC1458P1 MC1489L | |
| LM305H LM306H LM307H LM308H LM308AH | MLM305G MLM307G | MC1710CG MC1456G MC1456G | LM1489AJ LM1496H LM1496N LM1514J LM1558H | MC1489AL MC1496G MC1496L MC1514L MC1558G | |
| LM309K LM310H LM312H LM318H | MLM309K MLM310G | MC1456G MC1439G | LM1596H LM2111N LM3064H LM3064N LM3065N | MC1596G MC1357P MC1364G MC1364P MC1358P | |
| LM350N LM351N LM370H LM370N LM371H | MC75453P | MC75450P MC1590G MC1350P MFC6010 | LM3067N LM3070N LM3071N LM3900N LM3901N LM5520J | MC1370P MC1371P MC3401P MC3302P | MC1328P |
| LM376N LM380N LM381N LM382N LM703LN | | MFC6030A MFC9020 MC1339P MC1339P MFC6010 | LM5521J LM5523J LM5525J LM5528J LM5529J | | MC7520L MC7521L MC7523L MC7525L MC7528L MC7529L |
| LM709H LM709CH LM709CN LM710H LM710CH | MC1709G MC1709CG MC1709CP2 MC1710G MC1710CG | | LM5534J LM5535J LM5538J LM5539J LM7520J | MC7520L | MC7534L MC7535L MC7538L MC7539L |

NATIONAL TO MOTOROLA (continued)

| NATIONAL TYPE NUMBER | MOTOROLA DIRECT REPLACEMENT | MOTOROLA FUNCTIONAL EQUIVALENT |
|---|---|--------------------------------------|
| LM7520N LM7521J LM7521N LM7522J LM7522N | MC7520L MC7521L ML7521L ML7522L MC7522L | |
| LM7523J LM7523N LM7524J LM7524N LM7525J | MC7523L MC7523L MC7524L MC7524L MC7525L | |
| LM7525N LM7528J LM7528N LM7529J | MC7525L MC7528L MC7528L MC7529L | |
| LM7529N LM7534J LM7534N LM7535J LM7535N | MC7529L MC7534L MC7534L MC7535L MC7535L | |
| LM7538J LM7538N LM7539J LM7539N LM75450AN | MC7538L MC7538L MC7539L MC7539L | MC75450P |
| LM75451AN LM75452N LM75453N | MC75452P MC75453P | MC75451P |

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RCA TO MOTOROLA

| RCA DEVICE NUMBER | MOTOROLA DIRECT EQUIVALENT | MOTOROLA FUNCTIONAL EQUIVALENT | RCA DEVICE NUMBER | MOTOROLA DIRECT EQUIVALENT | MOTOROLA FUNCTIONAL EQUIVALENT |
|----------------------|----------------------------------|--------------------------------------|----------------------|----------------------------------|--------------------------------------|
| CA3000 | | MC1550G | CA3047A | | MC1433L |
| CA3001 | | MC1550G | CA3048 | | MC3401P |
| CA3002 | | MC1550G | CA3052 | | MC1339P |
| CA3004 | | MC1550G | CA3053 | | MC1550G |
| CA3005 | | MC1550G | CA3055 | | MC1723G |
| CA3006 | | MC1550G | CA3056 | | MC1741CG |
| CA3007 | | MC1550G | CA3056A | | MC1741G |
| CA3008 | | MC1709F | CA3058 | | MFC8070 |
| CA3008A | | MC1709F | CA3059 | | MFC8070 |
| CA3010 | | MC1709G | CA3064 | MC1364 | |
| CA3010A | | MC1709G | CA3065 | MC1358 | |
| CA3011 | | MC1590G | CA3066 | | MC1398P |
| CA3012 | | MC1590G | CA3067 | | MC1328P |
| CA3013 | | MC1355P | CA3070 | MC1370P | |
| CA3014 | | MC1357P | CA3071 | MC1371P | |
| CA3015 | | MC1709G | CA3072 | MC1328P | |
| CA3015A | | MC1709G | CA3075 | | MC1351P |
| CA3016 | | MC1709F | CA3076 | | MC1590G |
| CA3016A | | MC1709F | CA3079 | | MFC8070 |
| CA3020 | | MC1554G | CA3085 | | MC1723G |
| CA3020A | | MC1554G | CA3085A | | MC1723G |
| CA3021 | | MC1590G | CA3085B | | MC1310P |
| CA3022 | | MC1590G | CA3090Q | | MC1741G |
| CA3023 | | MC1590G | CA3741T | | MC1741CG |
| CA3028A | | MC1550G | CA3741CT | | |
| CA3028B | | MC1550G | | | |
| CA3029 | | MC1709CP2 | | | |
| CA3029A | | MC1709CP2 | | | |
| CA3030 | | MC1709CP2 | | | |
| CA3030A | | MC1709CP2 | | | |
| CA3031 | MC1712 | | | | |
| CA3032 | MC1712L | | | | |
| CA3033 | | MC1533L | | | |
| CA3033A | | MC1533L | | | |
| CA3035 | | MC1352P | | | |
| CA3037 | | MC1709L | | | |
| CA3037A | | MC1709L | | | |
| CA3038 | | MC1709L | | | |
| CA3038A | | MC1709L | | | |
| CA3040 | | MC1510G | | | |
| CA3041 | | MC1351P | | | |
| CA3042 | | MC1357P | | | |
| CA3043 | | MC1357P | | | |
| CA3047 | | MC1433L | | | |

SIGNETICS TO MOTOROLA

| SIGNETICS TYPE NUMBER | MOTOROLA DIRECT REPLACEMENT | MOTOROLA FUNCTIONAL EQUIVALENT | SIGNETICS TYPE NUMBER | MOTOROLA DIRECT REPLACEMENT | MOTOROLA FUNCTIONAL EQUIVALENT |
|--|--|---|--|---|---|
| NE501A NE501K NE510A NE510J NE515A | | MC1733CL MC1733CG MFC8000P MFC8000P MC1420G | N7523B N7524B | MC7523P MC7524P | |
| NE515G NE515K NE516A NE516G NE516K | | MC1520F MC1420G MC1420G MC1520F MC1420G | N7525B SE501K SE510A SE510J SE515G | MC7525P | MC1733G MFC8000P MFC8000P MC1520F |
| NE518A NE518G NE518K NE528B | | MLM306G MLM306G MLM306G MC1444L | SE515K SE516A SE516G SE516K SE518A | | MC1520G MC1520G MC1520F MC1520G MLM106G |
| NE528E NE531G NE531T NE531V NE533G | | MC1444L MC1439G MC1439G MC1439PZ MC1776CG | SE518G SE518K SE528E SE528R SE531G | | MLM106G MLM106G MC1544L MC1544L MC1539G |
| NE533V NE533T NE537G NE537T PA239A | MC1339 | MC1776CG MC1776CG MC1456G MC1456G | SE531T SE533G SE533T SE537G SE537T | | MC1539G MC1776G MC1776G MC1556G MC1556G |
| NE540L NE550A NE550L N5070B N5071A | MC1370 MC1371 | MFC8020A MFC6030A MC1723CG | SE540L SE550L S5556T S5558T S5558F | MC1556G MC1558G MC1558L | MFC8020A MC1723G |
| N5072A N5111 N5556T N5556V N5558V | MC1328 MC1357 MC1456G | MC1456G | S5595F S5596K S5596F S5709G S5709T | MC1595L MC1596G MC1596L MC1709F MC1709G | |
| N5558T N5558F N5595A N5595F N5596A | MC1458G MC1458L MC1495L MC1495L MC1496L | | S5710T S5711K S5723T S5733K S5741T | MC1710G MC1711G MC1723G MC1733G MC1741G | |
| N5596K N5709A N5709G N5709T N5709V | MC1496G MC1709CP2 MC1709CF MC1709CG MC1709CP1 | | | | |
| N5710A N5710T N5711A N5711K N5723A | MC1710CP MC1710CG MC1711CP MC1711CG | MFC6030A | | | |
| N5723T N5733K N5741A N5741T N5741V | MC1723CG MC1733CG MC1741CP2 MC1741CG MC1741CP1 | | | | |
| N5747A N5747F N5748A N5748T | MC1747CL MC1747CL MC1748CG | MC1747CG | | | |
| N7520B N7521B N7522B | MC7520P MC7521P MC7522P | | | | |

TEXAS INSTRUMENTS TO MOTOROLA

| T.I. TYPE NUMBER | MOTOROLA DIRECT REPLACEMENT | MOTOROLA FUNCTIONAL EQUIVALENT | T.I. TYPE NUMBER | MOTOROLA DIRECT REPLACEMENT | MOTOROLA FUNCTIONAL EQUIVALENT |
|--|--|--------------------------------|---|--|--|
| SN5500F SN5510F SN5510L SN5511F SN5511L | MC1510F MC1510G | MC1510F MC1510G | SN55110J SN55325J SN56514L SN72301AL SN72301AN SN72301AP | MC55110L MC55325L MLM301AG MLM301AP1 MLM301AP1 | MC1596G |
| SN5524J SN5525J SN5528J SN5529J SN5534J | MC5528L MC5529L MC5534L | MC7524L MC7524L | SN72306L SN72307L SN72558L SN72558P SN72702F | MLM306L MLM307G MC1458G MC1458P1 MC1712CF | |
| SN5535J SN5538J SN5539J SN7510F SN7510L SN7511L | MC5535L MC5538L MC5539L MC1410F MC1410G | MC1410G | SN72702L SN72702N SN72709L SN72709N | MC1712CG MC1712CL MC1709CG MC1709CP2 | |
| SN7520J SN7520N SN7521J SN7521N SN7522J | MC7520L MC7520L MC7521L MC7521L MC7522L | | SN72709P SN72709S SN72710J SN72710L SN72710N | MC1709CP1 MC1709CF MC1710CL MC1710CG MC1710CP2 | |
| SN7522N SN7523J SN7523N SN7524J SN7524N | MC7522L MC7523L MC7523L MC7524L MC7524L | | SN72710S SN72711J SN72711L SN7271N SN72611S | MC1710CF MC1711CL MC1711CG MC1711CP2 MC1711CF | |
| SN7525J SN7525N SN7528J SN7528N SN7529J | MC7525L MC7525L MC7528L MC7528L MC7529L | | SN72720N SN72733L SN72733N SN72741J SN72741L | MC1414L MC1733CG MC1733CL MC1741CL MC1741CG | |
| SN7529N SN52101AL SN52106L SN52107L SN52558L | MC7529L MLM101AG MLM106G MLM107G MC1558G | | SN72741N SN72741P SN72741Z SN72747J SN72747N | MC1741CP2 MC1741CP1 MC1741CF MC1747CL MC1747CL | |
| SN52702F SN52702L SN52702N SN52702Z SN52709F | MC1712F MC1712G MC1712L MC1712F MC1709F | | SN72748L SN72770L SN72771L SN75107J SN75107N | MC1748CG MC75107L MC75107L | MC1456G MC1456G |
| SN52709L SN52710J SN52710L SN52710N SN52710S | MC1709G MC1710L MC1710G MC1710P MC1710F | | SN75108J SN75108N SN75109J SN75109N SN75110J | MC75108L MC75108L MC75109L MC75109L MC75110L | |
| SN52711J SN52711L SN52711S SN52733L SN52741J | MC1711L MC1711G MC1711F MC1733G MC1741L | | SN75110N SN75150J SN75150N SN75154J SN75154N | MC75110L | MC1488L MC1488L MC1489AL MC1489AL |
| SN52741L SN52741Z SN52747J SN52748J SN52748L | MC1741G MC1741F MC1747L MC1748G | MC1748G | SN75234J SN75235J SN75238J SN75239J SN75325J | MC7534L MC7535L MC7538L MC7539L MC75325L | |
| SN52770L SN52771L SN55107J SN55108J SN55109J | MC55107L MC55108L MC55109L | MC1556G MC1556G | SN75450N SN75450AN SN75451P SN75451AP | MC75450P2 MC75451P | MC75450P2 MC75451P |

TEXAS INSTRUMENTS TO MOTOROLA (continued)

| T.I. TYPE NUMBER | MOTOROLA DIRECT REPLACEMENT | MOTOROLA FUNCTIONAL EQUIVALENT |
|--|--|--------------------------------------|
| SN75452P SN75453P SN75454P SN76104N SN76105N | MC75452P MC75453P MC75454P MC1304P MC1305P | |
| SN76107N SN76242N SN76243N SN76246N SN76514L | MC1307P MC1370P MC1371P MC1328P | MC1496G |
| SN76514N SN76530P SN76564N SN76600P SN76642N | MC1330P MC1364P MC1350P MC1350P | MC1496L |
| SN76650N SN76651N SN76653N SN76665N SN76675N | MC1352P MC1351P MC1353P MC1358P MC1375P | |

GENERAL INFORMATION

STANDARD FEATURES for LINEAR INTEGRATED CIRCUIT CHIPS

(See MCC and MCCF prefix data sheets for device specifications)

All linear integrated circuit chips

- are 100% electrically tested to sufficient parameter limits (min/max) to permit distinct identification as either premium or industrial versions
- employ phosphosilicate passivation which protects the entire active surface area including metalization interconnects during shipping and handling
- are 100% visually inspected to the criteria of MIL-STD-883, Method 2010.1, Condition B
- incorporate a minimum of 4000 Å gold backing to insure positive adherence bonding.

FEATURES for BEAM-LEAD CHIPS

(See MCBC prefix data sheets for device specifications)

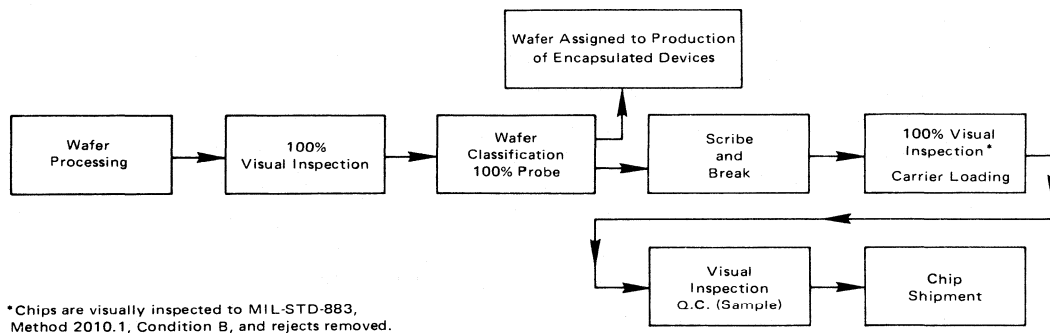
Beam lead linear integrated circuit chips

- are processed to the same criteria as the digital beam-lead integrated circuits to insure the same reliability and performance features.

STANDARD CHIP PROCESSING

The industry-standard linear integrated circuits offered in Motorola's Microcircuit Components line are subjected to the same in-process controls as Motorola's standard encapsulated devices. The chip processing and quality control requirements are designed to insure reliability and performance of the finished product.

The processing and quality control flow chart shows that all wafer processing is completed prior to wafer assignment for subsequent encapsulation or special testing required for unencapsulated devices.



*Chips are visually inspected to MIL-STD-883, Method 2010.1, Condition B, and rejects removed.

GENERAL INFORMATION

NON-STANDARD CHIP PROCESSING

The industry standard unencapsulated integrated circuits are selected to meet a wide variety of application requirements. Nevertheless, there may be occasions when a designer can benefit from a non-standard device for a specific circuit requirement. To satisfy these requirements, almost any device from Motorola's extensive line of linear integrated circuits may be obtained on a specially negotiated basis. Although the electrical specifications of these chips are limited by certain test limitations, the customer may negotiate additional tests. Moreover, various chip technologies such as solder-bump and chrome-silver backing are available on a specially negotiated basis.

HANDLING PRECAUTIONS

Metalization interconnect passivation on all chips provides protection in shipping and handling. However, care should be exercised to prevent damaging the bonding pads. A vacuum pickup is useful for this purpose, tweezers are not recommended.

There are four basic requirements for handling devices in the customer's establishment:

1. Store devices in a covered or sealed container.
2. Store devices in an environment of no more than 30% relative humidity.
3. Process devices in a non-inert atmosphere not exceeding 100^o, or in an inert atmosphere not exceeding 400^oC.
4. Processing equipment should conform to the minimum standards of equipment normally employed by semiconductor manufacturers.

Motorola's engineering staff is available for consultation in the event of correlation or processing problems encountered in the use of Motorola semiconductor chips. For assistance of this nature, please contact your nearest Motorola sales representative.

STANDARD CARRIER PACKAGES

The non-spill type shipping carrier consists of a compartmentalized tray and fitted transparent cover. Each chip is placed in its compartment, geometry side up, so that incoming visual inspection may be performed prior to breaking the carrier seal. The shipping carrier is designed to:

- provide maximum device protection
- permit the customer to remove only a portion of the devices — the carrier can be resealed
- provide a storage container for the unused devices.

Additional package techniques are under development to facilitate handling, visual inspection and chip storage.

Various packaging and shipping options are available on a negotiated basis. For more information on these options, please contact your Motorola sales representative.

RECOMMENDED INCOMING INSPECTION

Motorola certifies that the devices have been subjected to the visual criteria of MIL-STD-883, Method 2010.1, Condition B.

Should the lot fail the customer's incoming visual inspection, the entire lot, with the package seals intact, shall be returned to Motorola. Incoming visual inspection should be performed prior to breaking the package seals. In no case will Motorola accept a partial return of devices.

MC1303L

DUAL STEREO PREAMPLIFIER

MONOLITHIC DUAL STEREO PREAMPLIFIER

... designed for amplifying low-level stereo audio signals with two preamplifiers built into a single monolithic semiconductor.

Each Preamplifier Features:

- Large Output Voltage Swing – 4.0 V(rms) min
- High Open-Loop Voltage Gain = 6000 min
- Channel Separation = 60 dB min at 10 kHz
- Short-Circuit-Proof Design

DUAL STEREO PREAMPLIFIER INTEGRATED CIRCUIT MONOLITHIC SILICON EPITAXIAL PASSIVATED



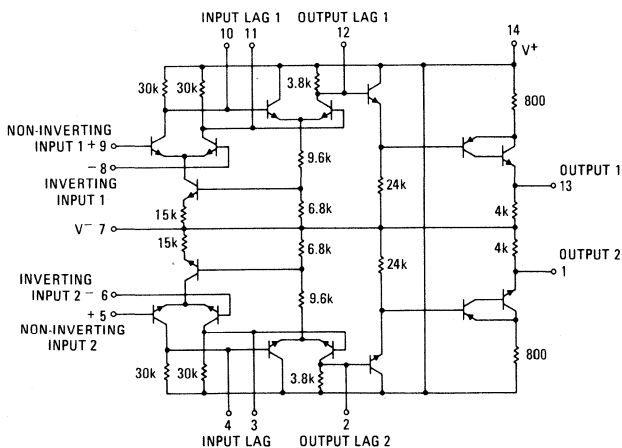
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

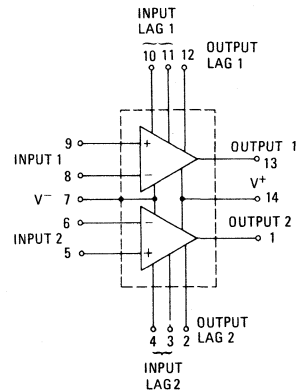
| Rating | Symbol | Value | Unit |
|---|----------------|----------|-------|
| Power Supply Voltage | V ⁺ | +15 | Vdc |
| | V ⁻ | -15 | Vdc |
| Power Dissipation (Package Limitation) Derate above 25°C | P _D | 625 | mW |
| | | 5.0 | mW/°C |
| Operating Temperature Range | T _A | 0 to +75 | °C |

Maximum Ratings as defined in MIL-S-19500, Appendix A.

CIRCUIT SCHEMATIC



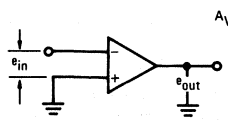
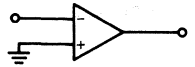
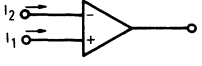
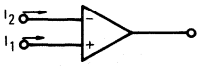
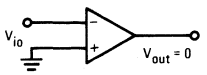
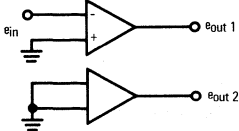
EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

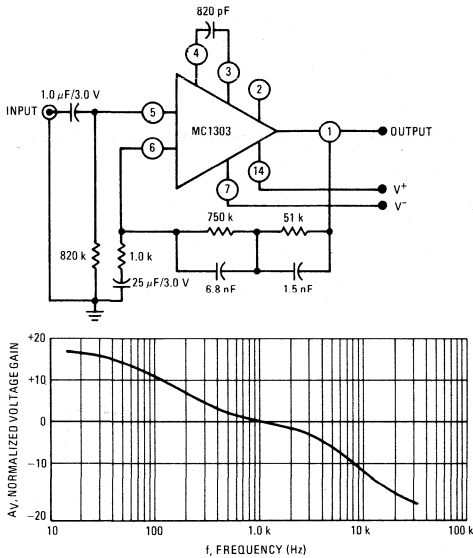
MC1303L (continued)

ELECTRICAL CHARACTERISTICS (Each Preamplifier) ($V^+ = +13$ Vdc, $V^- = -13$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic Definitions (linear operations) | Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---|-------------------------------|-------|--------|-----|---------------|
|  | Open Loop Voltage Gain | A_{VOL} | 6,000 | 10,000 | - | V/V |
|  | Output Voltage Swing ($R_L = 10$ k Ω) | V_{out} | 4.0 | 5.5 | - | V(rms) |
|  | Input Bias Current $I_b = \frac{I_1 + I_2}{2}$ | I_b | - | 1.0 | 10 | μA |
|  | Input Offset Current ($I_{io} = I_1 - I_2$) | I_{io} | - | 0.2 | 0.4 | μA |
|  | Input Offset Voltage | V_{io} | - | 1.5 | 10 | mV |
| | DC Power Dissipation (Power Supply = ± 13 V, $V_{out} = 0$) | P_D | - | - | 400 | mW |
|  | Channel Separation ($f = 10$ kHz) | $\frac{e_{out 1}}{e_{out 2}}$ | 60 | 70 | - | dB |

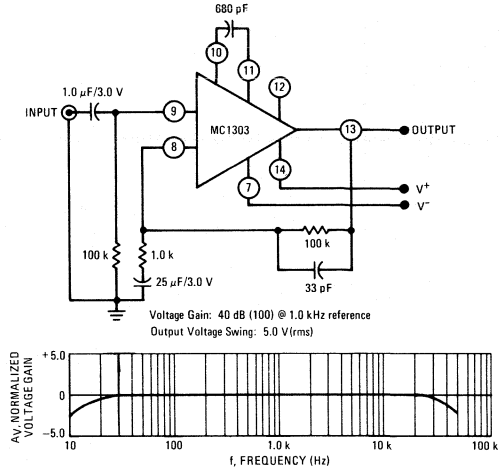
TYPICAL PREAMPLIFIER APPLICATIONS

FIGURE 1 — MAGNETIC PHONO PLAYBACK PREAMPLIFIER/RIAA EQUALIZED

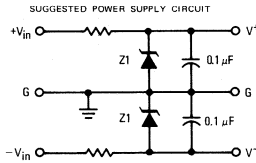


TYPICAL PERFORMANCE CHARACTERISTICS
 Voltage Gain : 34 dB (50) @ 1.0 kHz
 Input Overload Point : 100 mVrms @ 1.0 kHz
 Output Voltage Swing : 5.0 Vrms @ 1.0 kHz @ 0.1% THD
 Output Noise Level : Better Than 70 dB Below 10 mV Phono Input (Input Shorted)

FIGURE 2 — BROADBAND AUDIO AMPLIFIER

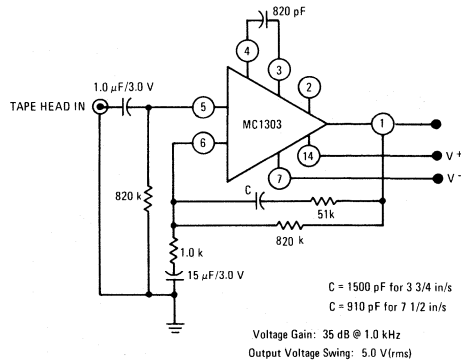
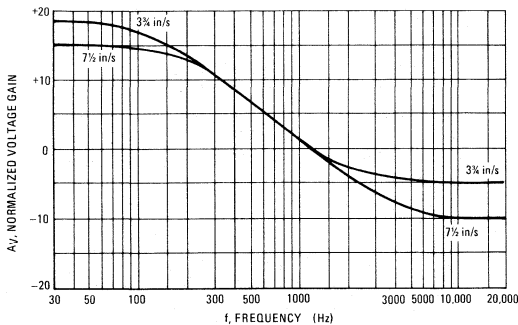


Voltage Gain: 40 dB (100) @ 1.0 kHz reference
 Output Voltage Swing: 5.0 V(rms)



Z1 = MZ 500-19 (13 V nom.)
 Select series R by allowing 11 mA for zener, and each dual I/C Preamplifier

FIGURE 3 — NAB TAPE HEAD EQUALIZATION



C = 1500 pF for 3 3/4 in/s
 C = 910 pF for 7 1/2 in/s
 Voltage Gain: 35 dB @ 1.0 kHz
 Output Voltage Swing: 5.0 V(rms)

FIGURE 4 – POWER DISSIPATION versus SUPPLY VOLTAGE

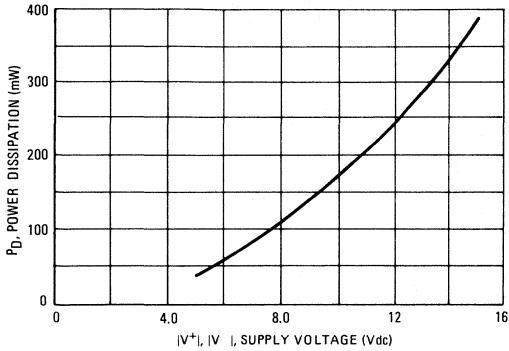


FIGURE 5 – OUTPUT LINEARITY

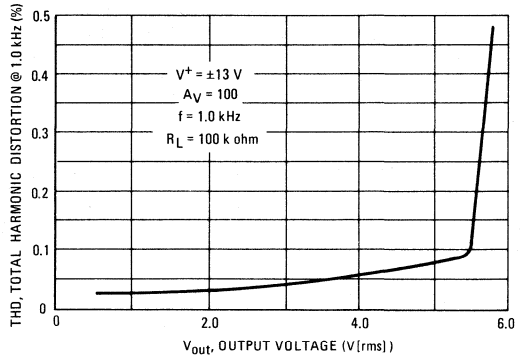
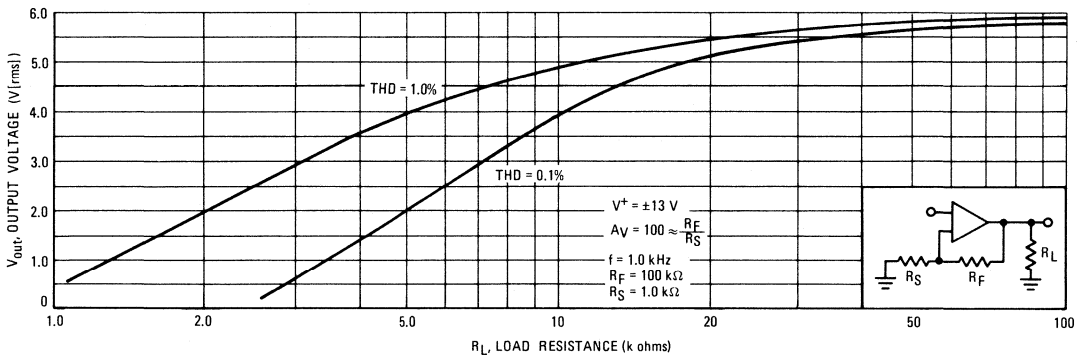


FIGURE 6 – INFLUENCE OF OUTPUT LOADING



NOISE CHARACTERISTICS

FIGURE 7A – INFLUENCE OF SOURCE RESISTANCE & BANDWIDTH

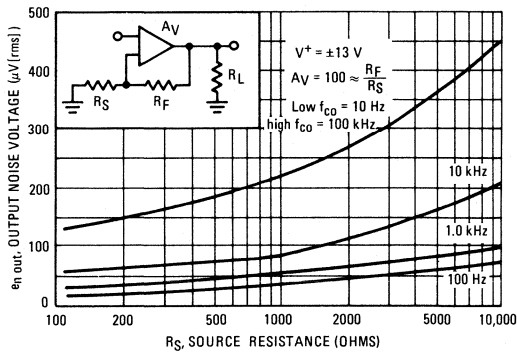
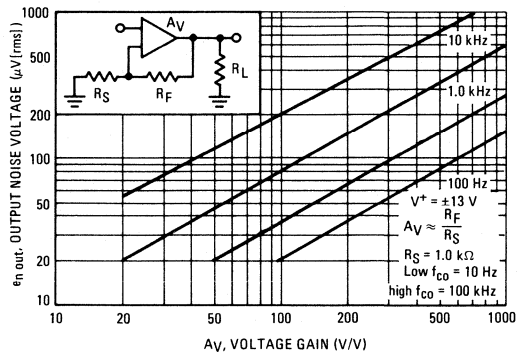


FIGURE 7B – INFLUENCE OF VOLTAGE GAIN & BANDWIDTH



STEREO DEMODULATOR

MC1304P MC1305P

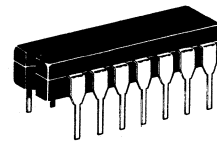
MONOLITHIC FM MULTIPLEX STEREO DEMODULATORS

... derive the left and right audio information from the detected composite signal. The MC1304P eliminates the need for an external stereo-channel separation control. The MC1305P is similar to the MC1304P but permits the use of an external stereo-channel separation control for maximum separation.

- Operation Practicable Over Wide Power-Supply Range, 8-14 Vdc
- Built-in Stereo-Indicator Lamp Driver
- Total Audio Muting Capability
- Automatic Switching – Stereo-Monaural
- Monaural Squelch Capability

FM MULTIPLEX STEREO DEMODULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS



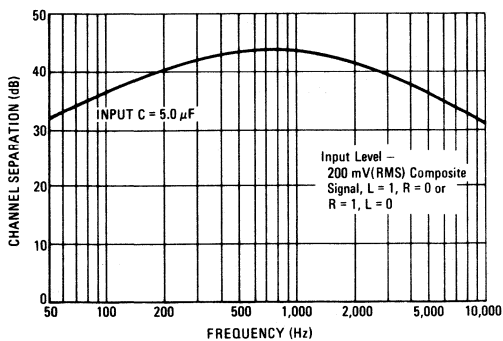
PLASTIC PACKAGE
CASE 646
TO-116

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

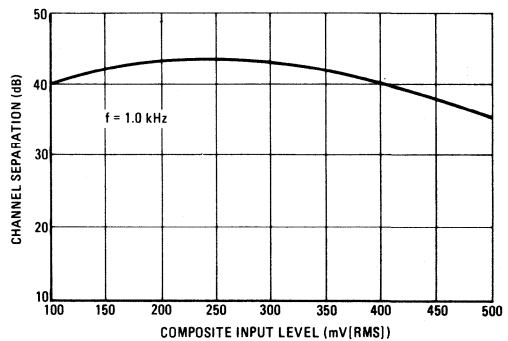
| Rating | Value | Unit |
|--|-------------|------------------|
| Power Supply Voltage (Pins 1, 6, 9,*11, 12) (Pin 7 is grounded) | +22 | Vdc |
| Lamp Driver Current | 40 | mAdc |
| Power Dissipation (Package Limitation) Plastic Package Derate above $T_A = 25^\circ\text{C}$ | 625 | mW |
| Operating Temperature Range (Ambient) | 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | -65 to +150 | $^\circ\text{C}$ |

* Pin 8 for MC1305P

CHANNEL SEPARATION versus FREQUENCY



CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL



See Packaging Information Section for outline dimensions.

MC1304P, MC1305P (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = 12 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted. Test made with $75 \mu\text{s}$ de-emphasis network ($3.9 \text{ k}\Omega$, $0.02 \mu\text{F}$) unless otherwise noted).

| Characteristics | Min | Typ | Max | Unit |
|---|-----------------|----------------|-----------------|------------------|
| Input Impedance ($f = 20 \text{ Hz}$) | 12 | 20 | — | $\text{k}\Omega$ |
| Stereo Channel Separation (See Notes 1 and 2) ($f = 100 \text{ Hz}$) ($f = 1.0 \text{ kHz}$) ($f = 10 \text{ kHz}$) | — — — | 35 45 30 | — — — | dB |
| Channel Balance (Monaural Input = 200 mV(RMS)), (Monaural, Left and Right Outputs) | — | 0.5 | — | dB |
| Total Harmonic Distortion (See Notes 1 and 3) (Modulation frequency - 1.0 kHz) | — | 0.5 | 1.0 | % |
| Ultrasonic Frequency Rejection (See Note 4) (19 kHz) (38 kHz) | — — | 25 20 | — — | dB |
| Inherent SCA Rejection (without filter) @ 60 kHz , 67 kHz and 74 kHz | — | 50 | — | dB |
| Lamp Indicator ($R_A = 120\Omega$) Minimum 19 kHz Input Level for lamp on Maximum 19 kHz Input Level for lamp off | — 5.0 | 16 14 | 25 — | mV(RMS) |
| Audio Muting Mute on (Voltage required at pin 5) Mute off (Voltage required at pin 5) Attenuation in Mute Mode (Note 5) | 0.6 1.3 — | — — 55 | 1.0 2.0 — | Vdc Vdc dB |
| Stereo-Monaural Switching Stereo (Voltage required at pin 4) Monaural (Voltage required at pin 4) | 1.3 — | — — | 2.0 1.0 | Vdc |
| Power Dissipation ($V_{CC} = 10 \text{ V}$) (Without lamp) (With lamp) | — — | 150 180 | 300 300 | mW |

Note 1 — Measurement made with 200 mV(RMS) Standard Multiplex Composite Signal and $L = 1$, $R = 0$ or $R = 1$, $L = 0$. Standard Multiplex Composite signal is here defined as a signal containing left and/or right audio information with a 10% (19 kHz) pilot signal in accordance with FCC regulations.

Note 2 — Stereo channel separation is adjustable for the MC1305P with a resistor from pin 9 to ground.

Note 3 — Distortion specification also applies to Monaural Signal.

Note 4 — Referenced to 1.0 kHz output signal with Standard Multiplex Composite Input Signal.

Note 5 — This is referenced to 1.0 kHz output signal with either Standard Multiplex Composite Signal or Monaural Input Signal.

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

FIGURE 1 — DISTORTION COMPONENTS IN AUDIO SIGNAL

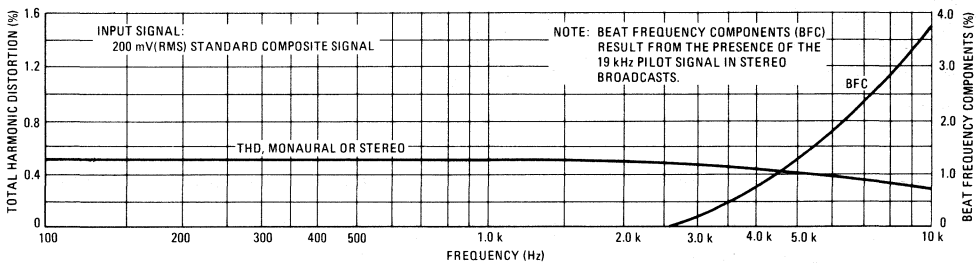


FIGURE 2 — TOTAL HARMONIC DISTORTION

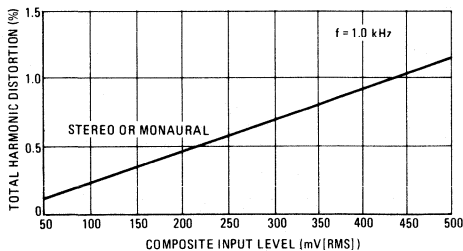
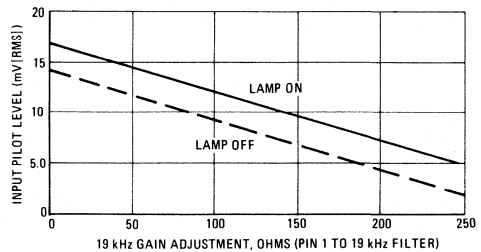


FIGURE 3 — MULTIPLEX SENSITIVITY



MC1304P, MC1305P (continued)

FIGURE 4 - MC1304 CIRCUIT SCHEMATIC

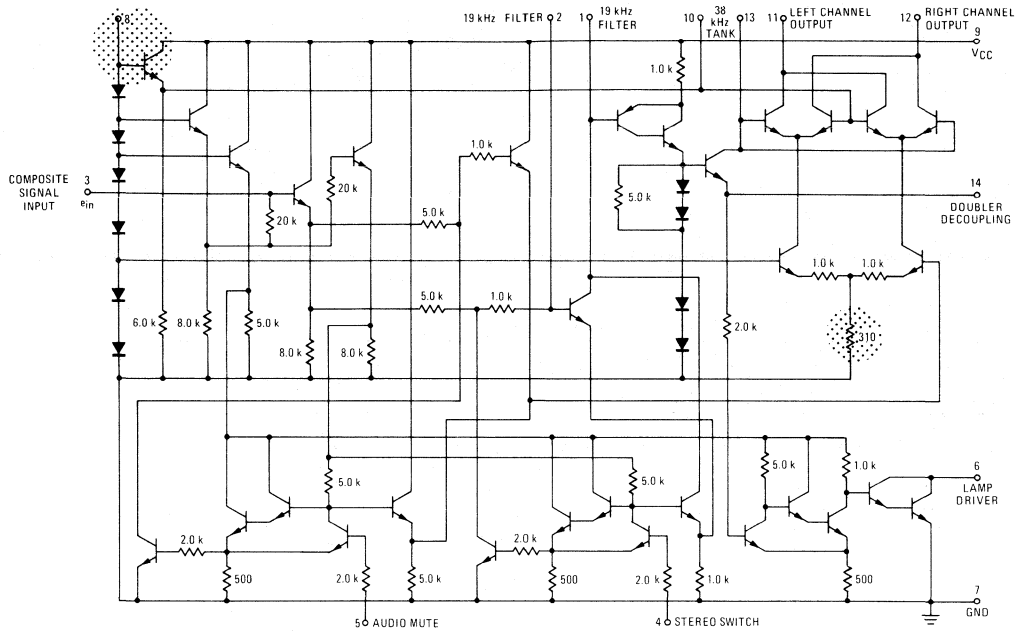
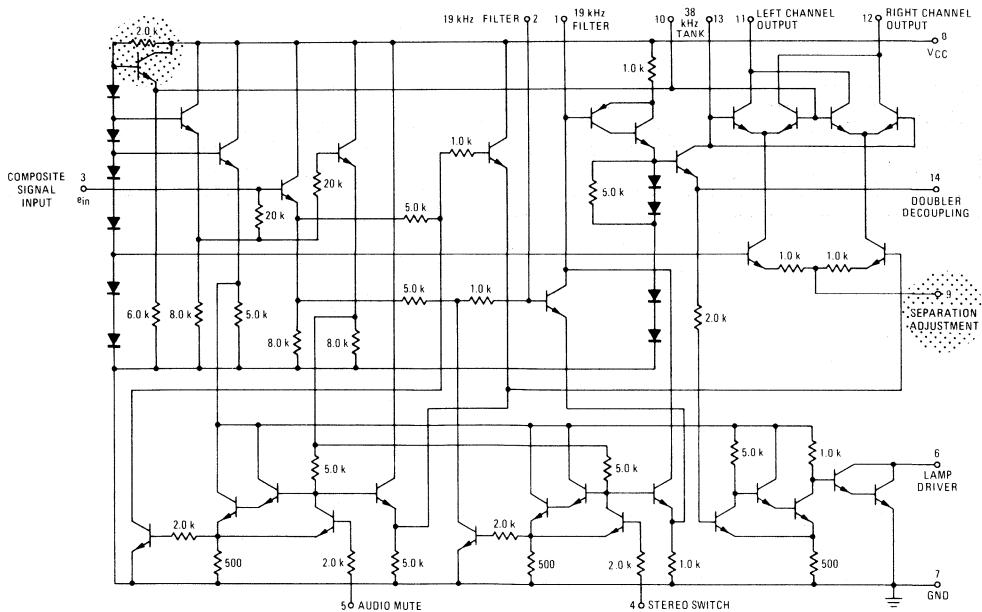


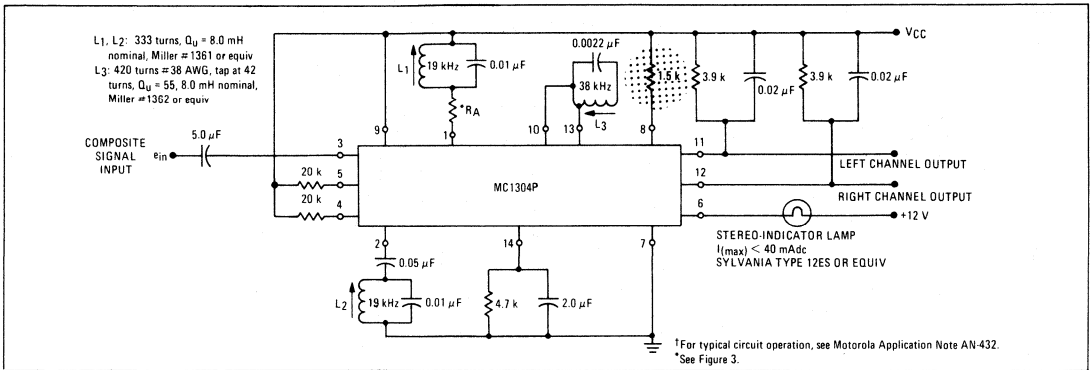
FIGURE 5 - MC1305 CIRCUIT SCHEMATIC



Portions of the circuits shown within the dotted areas pertain to the MC1304P or MC1305P as indicated by the titles of the circuits.

MC1304P, MC1305P (continued)

FIGURE 6 – MC1304P TYPICAL CIRCUIT CONFIGURATION†

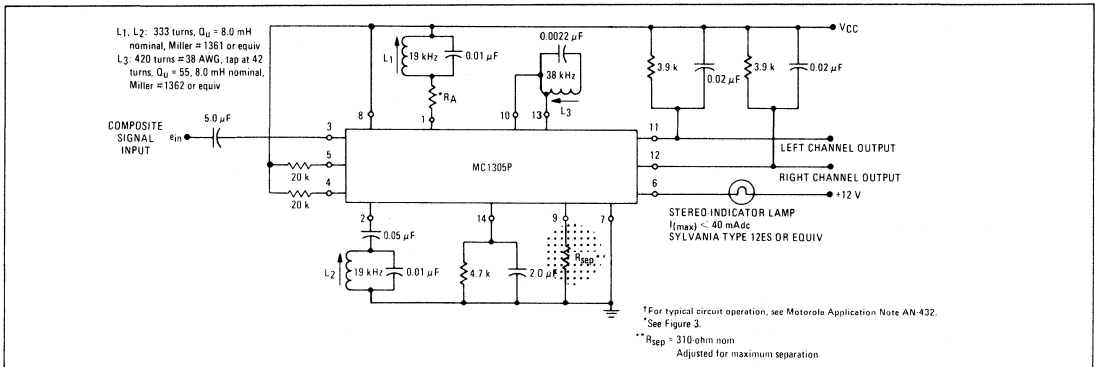


Typical dc voltages (All voltages measured with respect to ground, Pin 7, $R_A = 0$)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|--------------------|-----|-----|-----|-----|-----|-----|---|-------|-----|-----|-----|-----|-----|-----|
| $V_{CC} = 8.5$ Vdc | 8.5 | 2.0 | 2.8 | 1.6 | 1.6 | 0.8 | 0 | 4.6* | 8.5 | 3.9 | 6.3 | 6.3 | 3.9 | 1.9 |
| $V_{CC} = 12$ Vdc | 12 | 2.0 | 2.8 | 1.9 | 1.9 | 0.8 | 0 | 4.6** | 12 | 3.9 | 9.7 | 9.7 | 3.9 | 1.9 |

*1.5 k Ω in series with pin 8
 **2.7 k Ω in series with pin 8

FIGURE 7 – MC1305P TYPICAL CIRCUIT CONFIGURATION†



Typical dc voltages (All voltages measured with respect to ground (Pin 7))

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|--------------------|-----|-----|-----|-----|-----|-----|---|-----|------|-----|-----|-----|-----|-----|
| $V_{CC} = 8.5$ Vdc | 8.5 | 2.0 | 2.8 | 1.6 | 1.6 | 0.8 | 0 | 8.5 | 0.32 | 3.9 | 6.3 | 6.3 | 3.9 | 1.9 |
| $V_{CC} = 12$ Vdc | 12 | 2.0 | 2.8 | 1.9 | 1.9 | 0.8 | 0 | 12 | 0.36 | 3.9 | 9.7 | 9.7 | 3.9 | 1.9 |

Portions of the circuits shown within the dotted areas pertain to the MC1304P or MC1305P as indicated by the titles of the circuits.

MC1306P

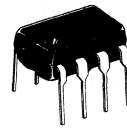
AUDIO AMPLIFIER

1/2-WATT AUDIO AMPLIFIER

The MC1306P is a monolithic complementary power amplifier and preamplifier designed to deliver 1/2-Watt into a loudspeaker with a 3.0 mV(rms) typical input. Gain and bandwidth are externally adjustable. Typical applications include portable AM-FM radios, tape recorder, phonographs, and intercoms.

- 1/2-Watt Power Output (9.0 Vdc Supply, 8-Ohm Load)
- High Overall Gain – 3.0 mV(rms) Sensitivity for 1/2-Watt Output
- Low Zero-Signal Current Drain – 4.0 mA dc @ 9.0 V typ
- Low Distortion – 0.5% at 250 mW typ

1/2-WATT AUDIO AMPLIFIER



PLASTIC PACKAGE
CASE 626

TYPICAL APPLICATIONS

FIGURE 1 – AM-FM RADIO, AUDIO SECTION

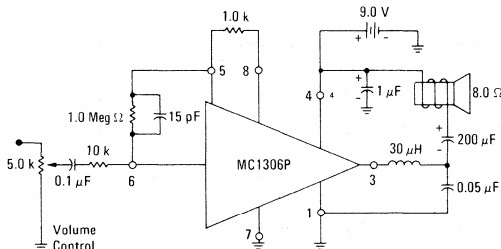
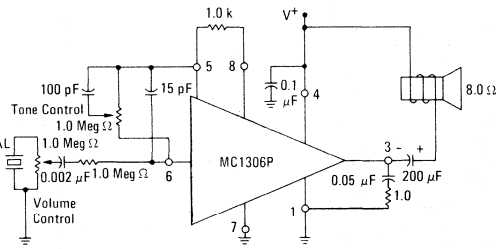
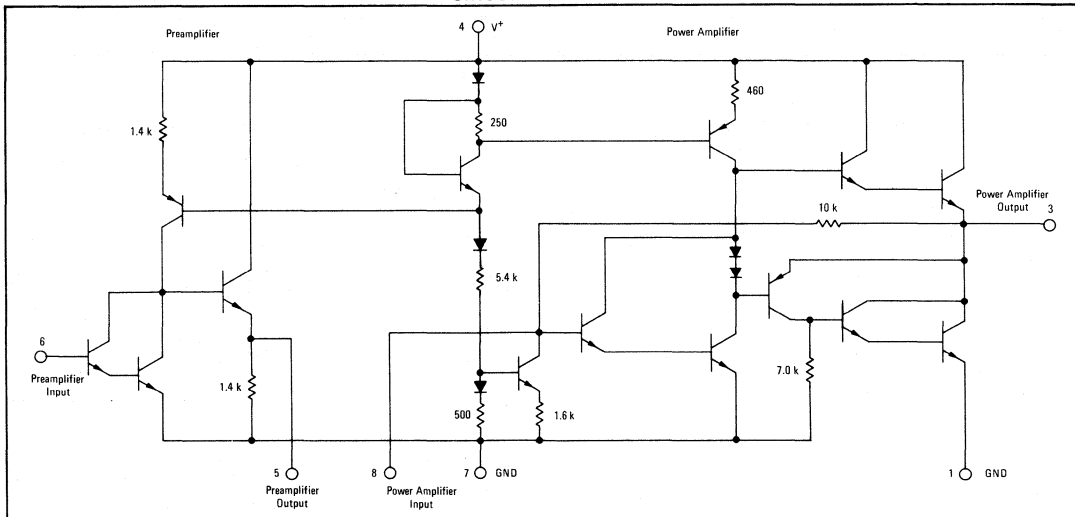


FIGURE 2 – PHONOGRAPH AMPLIFIER
(CERAMIC CARTRIDGE)



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MC1306P (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|-----------------|-------------|----------------------|
| Power Supply Voltage | V^+ | 12 | Vdc |
| Load Current | I_L | 400 | mAdc |
| Power Dissipation (Package Limitation) $T_A = +25^\circ\text{C}$ | P_D | 625 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | $1/\theta_{JA}$ | 5.0 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS ($V^+ = 9.0\text{ V}$, $R_L = 8.0\text{ ohms}$, $f = 1.0\text{ kHz}$, (using test circuit of Figure 3), $T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-----------|-----|------------|-----|----------|
| Open Loop Voltage Gain Pre-amplifier $R_L = 1.0\text{ k ohm}$ Power-amplifier $R_L = 16\text{ ohms}$ | A_{VOL} | — | 270 360 | — | V/V |
| Sensitivity ($P_O = 500\text{ mW}$) | S | — | 3.0 | — | mV (rms) |
| Output Impedance (Power-amplifier) | Z_O | — | 0.5 | — | Ohm |
| Signal to Noise Ratio ($P_O = 150\text{ mW}$, $f = 300\text{ Hz to }10\text{ kHz}$) | S/N | — | 55 | — | dB |
| Total Harmonic Distortion ($P_O = 250\text{ mW}$) | THD | — | 0.5 | — | % |
| Quiescent Output Voltage | V_O | — | $V^+/2$ | — | Vdc |
| Output Power (THD $\leq 10\%$) | P_O | 500 | 570 | — | mW |
| Current Drain (zero signal) | I_D | — | 4.0 | — | mA |
| Power Dissipation (zero signal) | P_D | — | 36 | — | mW |

FIGURE 3 – TEST CIRCUIT

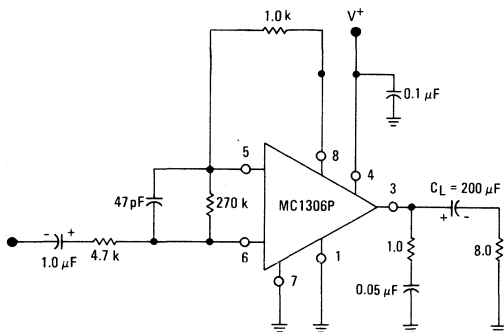
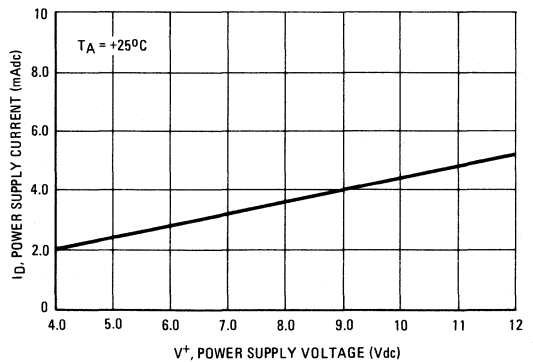


FIGURE 4 – ZERO SIGNAL BIAS CURRENT



TYPICAL CHARACTERISTICS

($V^+ = 9.0\text{ V}$, $f = 1.0\text{ kHz}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 5 – EFFICIENCY

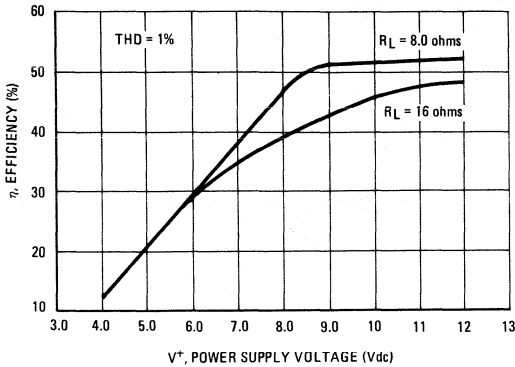


FIGURE 6 – OUTPUT POWER

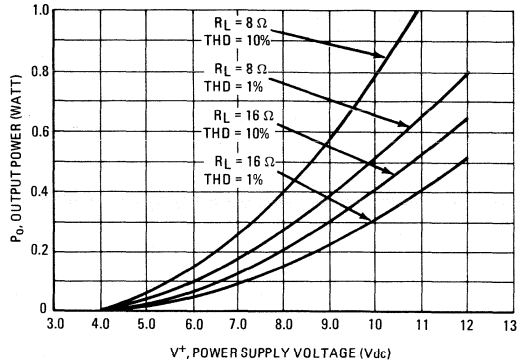


FIGURE 7 – TOTAL HARMONIC DISTORTION

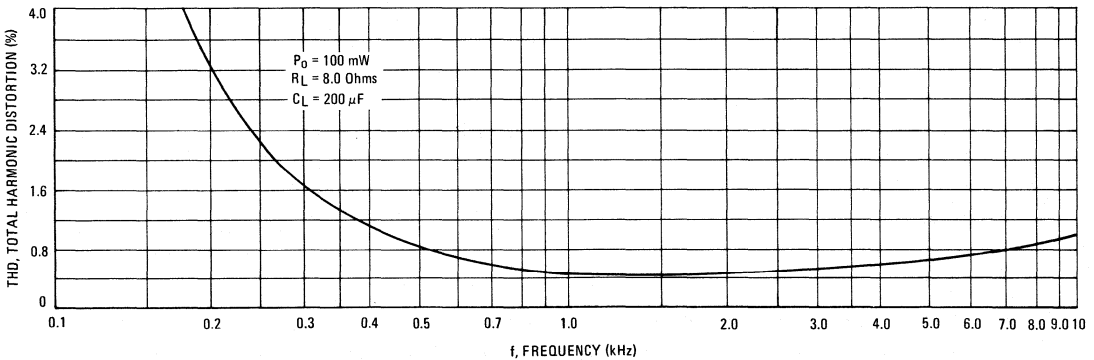


FIGURE 8 – EFFECT OF BATTERY AGING ON LOW-LEVEL DISTORTION

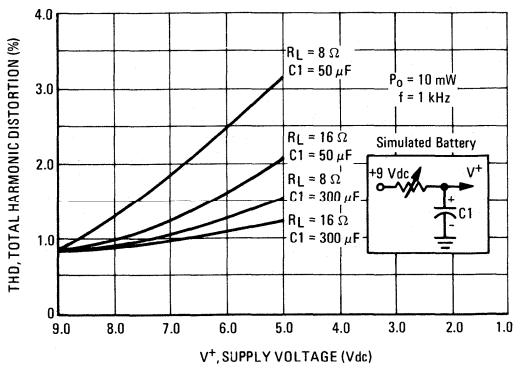


FIGURE 9 – DISTORTION

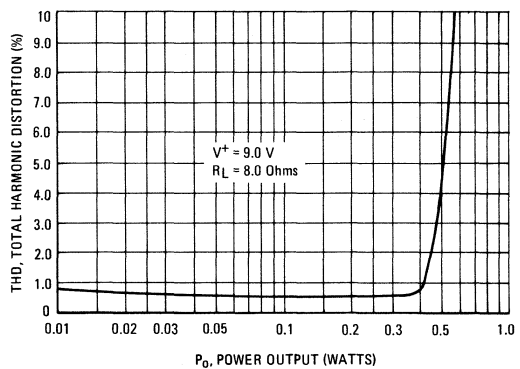
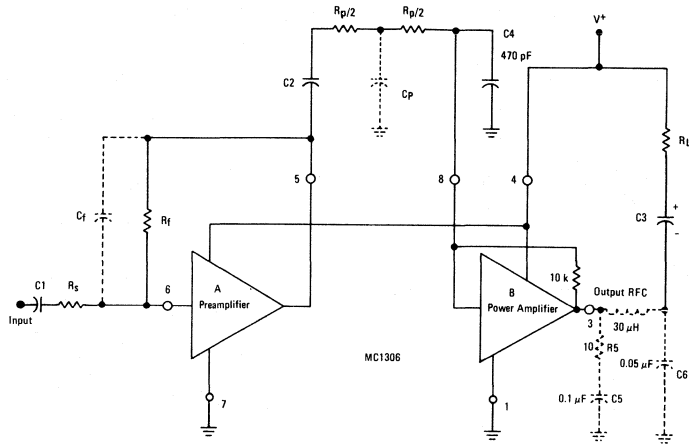


FIGURE 10 – TYPICAL CIRCUIT CONNECTION



DESIGN CONSIDERATIONS

The MC1306P provides the designer with a means to control preamplifier gain, power amplifier gain, input impedance, and frequency response. The following relationships will serve as guides.

1. Gain

The Preamplifier Stage Voltage Gain is:

$$A_{VA} \approx \frac{R_f}{R_s}$$

and is limited only by the open-loop gain (270 V/V). For good preamplifier dc stability R_f should be no larger than 1.0-megohm.

The Power Amplifier Voltage Gain is controlled in a similar manner where:

$$A_{VB} \approx \frac{10\text{ k}}{R_p}$$

The 10-k ohm feedback resistor is provided in the integrated circuit.

Recommended values of R_p range from 500-ohms to 3.3-k ohms. The low end is limited primarily by low-level distortion and the upper end is limited due to the voltage drive capabilities of the pre-amplifier. (A resistor can be added in the dc feedback loop, from pin 6 to ground, to increase this drive): The Overall Voltage Gain, then, is:

$$A_{VT} = \frac{R_f 10\text{ k}}{R_s R_p}$$

2. Input Impedance

The Preamplifier Input Impedance is:

$$Z_{inA} \approx R_s$$

and the Power Amplifier Input Impedance is:

$$Z_{inB} \approx R_p$$

3. Frequency Response

The low frequency response is controlled by the cumulative effect of the series coupling capacitors C1, C2, and C3. High-frequency response can be determined by the feedback capacitor, C_f , and the -3.0 dB point occurs when

$$X_{C_f} = R_f$$

Additional high frequency roll-off and noise reduction can be achieved by placing a capacitor from the center point of R_p to ground as shown in Figure 10.

Capacitor C4 and the RC network shown in dotted lines may be needed to prevent high frequency parasitic oscillations. The RF choke, shown in series with the output, and capacitor C6 are used to prevent the high-frequency components in a large-signal clipped audio output waveform from radiating into the RF or IF sections of a radio (Figure 10).

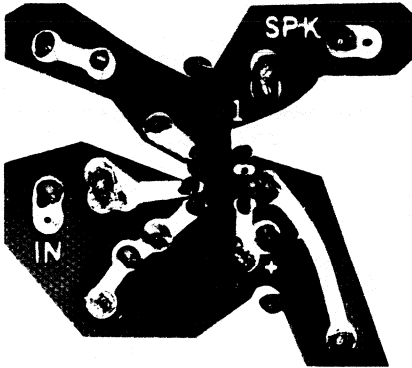
4. Battery Operation

The increase of battery resistance with age has two undesirable effects on circuit performance. One effect is the increasing of amplifier distortion at low signal levels. This is readily corrected by increasing the size of the filter capacitor placed across the battery (as shown in Figure 8; a 300- μ F filter capacitor gives distortions at low-tonal levels that are comparable to the "stiff" supply). The second effect of supply impedance is a lowering of power output capability for steady signals. This condition is not correctable, but is of questionable importance for music and voice signals.

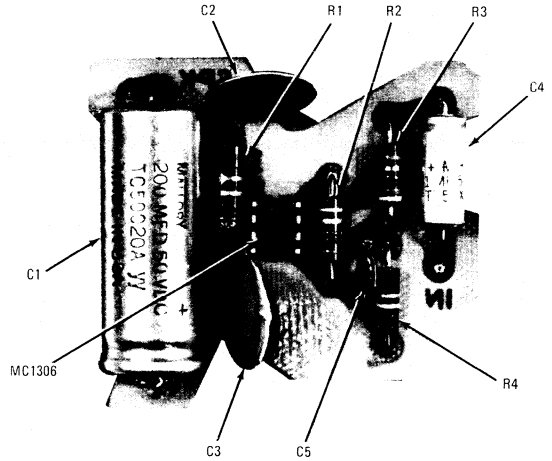
5. Application Examples: (1) The audio section of the AM-FM radio (Figure 1) is adjusted for a preamplifier gain of 100 with an input impedance of 10-k ohms. The power amplifier gain is set at 10, which gives an overall voltage gain of 1000. The bandwidth has been set at 10-kHz. (2) The phono amplifier (Figure 2) is designed for a preamplifier gain of unity and a power amplifier gain of 10. The input impedance is 1.0-megohm. An adjustable treble control is provided within the feedback loop.

MC1306P (continued)

TYPICAL PRINTED CIRCUIT BOARD LAYOUT



LOCATION OF COMPONENTS



See Figure 3 for schematic diagram.

PARTS LIST

| Component | Value |
|-----------|--------------|
| C1 | 200 μ F |
| C2 | 0.1 μ F |
| C3 | 0.05 μ F |
| C4 | 1.0 μ F |
| C5 | 47 pF |
| R1 | 1 ohm |
| R2 | 1 k ohm |
| R3 | 4.7 k ohms |
| R4 | 270 k ohms |
| MC1306 | — |
| PC Board | — |

STEREO DEMODULATOR

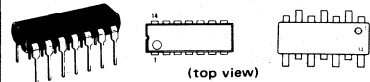
MC1307

MONOLITHIC FM MULTIPLEX STEREO DEMODULATOR

... designed to derive the left and right channel audio information from the detected composite signal.

- Capable of Operation Over a Wide Power Supply Range — 8.0 — 14 Vdc
- Built-in Stereo-Indicator Lamp Driver

FM MULTIPLEX STEREO DEMODULATOR SILICON MONOLITHIC INTEGRATED CIRCUIT

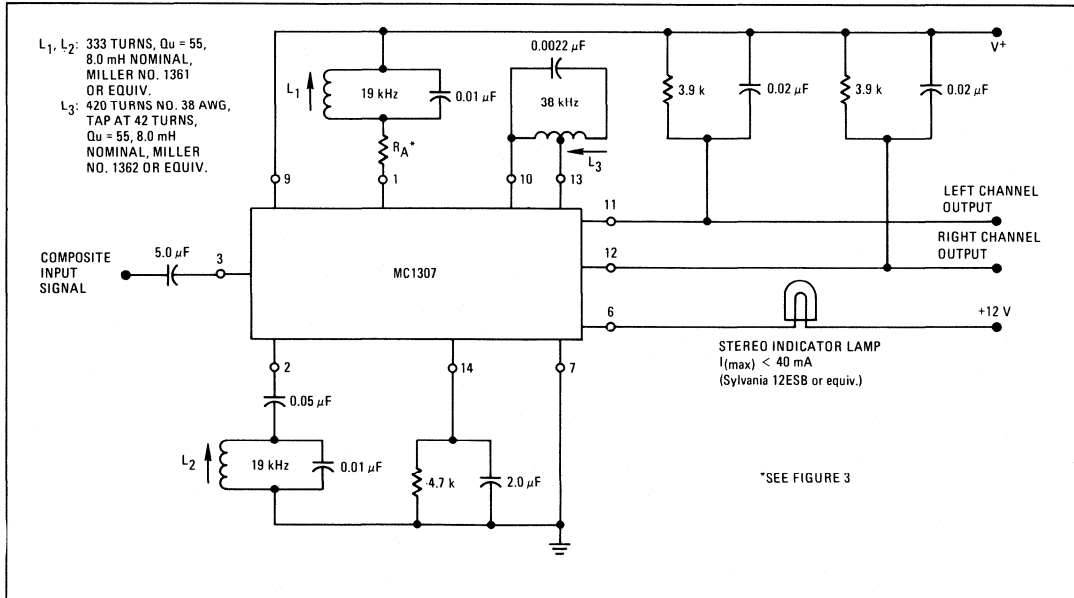


P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 — TYPICAL CIRCUIT CONFIGURATION

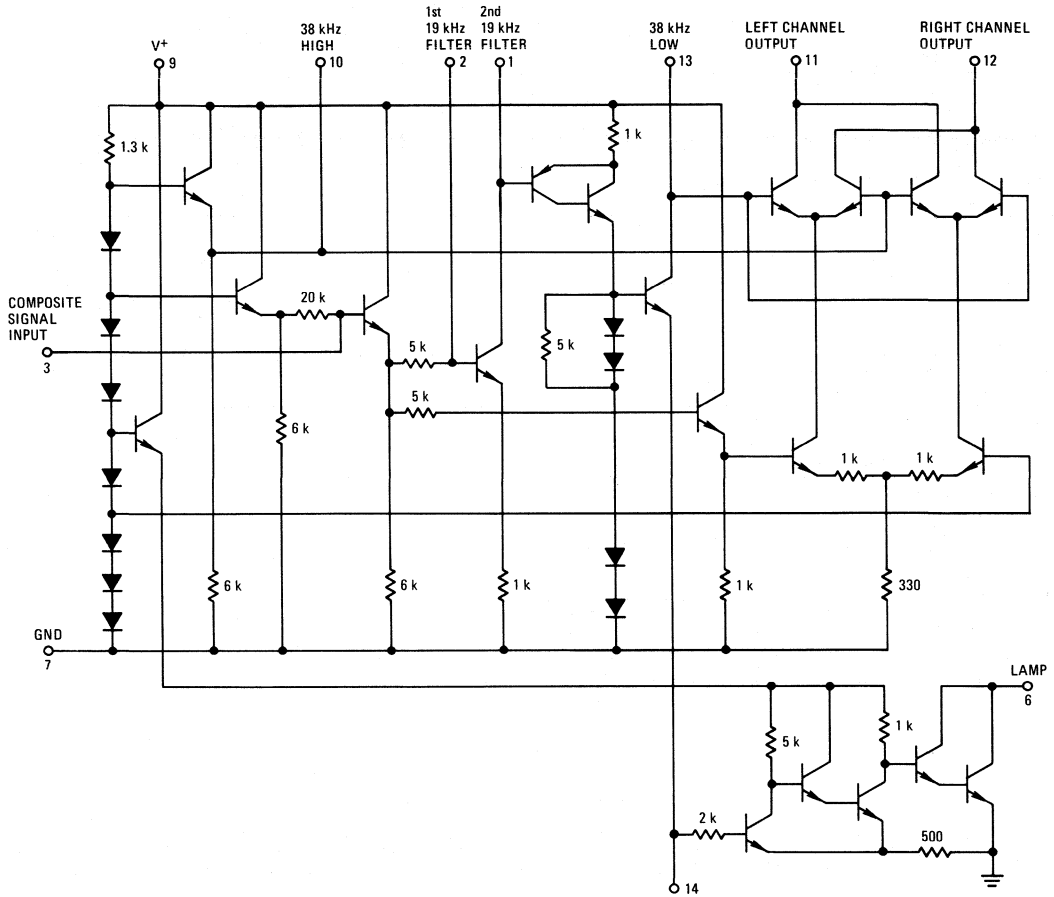


TYPICAL DC VOLTAGES (All measured using a VTVM with respect to Pin 7 (lamp on), R_D = 180 ohms, see Figure 3)

| Pin Numbers | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|--------------------------|-----|-----|-----|---|---|-----|---|---|-----|-----|-----|-----|-----|-----|
| V ⁺ = 8.5 Vdc | 8.5 | 2.7 | 3.6 | — | — | 0.8 | 0 | — | 8.5 | 4.4 | 6.2 | 6.2 | 4.4 | 1.5 |
| V ⁺ = 12 Vdc | 12 | 2.9 | 3.9 | — | — | 0.9 | 0 | — | 12 | 4.7 | 9.7 | 9.7 | 4.7 | 1.7 |

See Packaging Information Section for outline dimensions.

FIGURE 2 – CIRCUIT SCHEMATIC



MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

| Rating | Value | Unit |
|--|-------------|------------------------|
| Power Supply Voltage (Pins 1, 6, 9, 11, 12) (Pin 7 is grounded) | +22 | Vdc |
| Lamp Driver Current | 40 | mA _{dc} |
| Power Dissipation (Package Limitation) | 625 | mW |
| Derate above $T_A = +25^{\circ}\text{C}$ | 5.0 | mW/ $^{\circ}\text{C}$ |
| Operating Temperature Range (Ambient) | 0 to +75 | $^{\circ}\text{C}$ |
| Storage Temperature Range | -65 to +150 | $^{\circ}\text{C}$ |

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS ($V^+ = 12$ Vdc, $T_A = +25^\circ\text{C}$, tests made with a $75\ \mu\text{s}$ de-emphasis network ($3.9\ \text{k}\Omega$, $0.02\ \mu\text{F}$) unless otherwise noted)

| Characteristic | Min | Typ | Max | Unit |
|---|--------------|----------------|-------------|------------------|
| Input Impedance ($f = 1.0\ \text{kHz}$) | 12 | 20 | — | $\text{k}\Omega$ |
| Stereo Channel Separation (See Note 1) ($f = 100\ \text{Hz}$) ($f = 1.0\ \text{kHz}$) ($f = 10\ \text{kHz}$) | — 20 — | 35 40 30 | — — — | dB |
| Total Harmonic Distortion (See Notes 1 and 2) (Modulation Frequency = $1.0\ \text{kHz}$) | — | 0.5 | 1.0 | % |
| Channel Balance (Monaural Input = $200\ \text{mV}$ [rms]) (Monaural, Left and Right Outputs) | — | 0.5 | — | dB |
| Ultrasonic Frequency Rejection (See Note 3) ($19\ \text{kHz}$) ($38\ \text{kHz}$) | — — | 25 20 | — — | dB |
| Inherent SCA Rejection (without filter) ($f = 60\ \text{kHz}$, $67\ \text{kHz}$ and $74\ \text{kHz}$) (See Note 3) | — | 50 | — | dB |
| Lamp Indicator ($R_A = 180\ \Omega$) (Minimum $19\ \text{kHz}$ input level for lamp "on") (Maximum $19\ \text{kHz}$ input level for lamp "off") | — 5.0 | 16 14 | 25 — | mV(rms) |
| Power Dissipation ($V^+ = 12\ \text{V}$) (Without lamp) (With lamp) | — — | 140 170 | 300 300 | mW |

Note 1 — Measurement made with $200\ \text{mV}$ (rms) Standard Multiplex Composite Signal where $L = 1$, $R = 0$ or $R = 1$, $L = 0$. Standard Multiplex Composite Signal is here defined as a signal containing left and/or right audio information with a 10% ($19\ \text{kHz}$) pilot signal in accordance with FCC regulations.

Note 2 — Distortion specification also applies to Monaural Signal.

Note 3 — Referenced to $1.0\ \text{kHz}$ output signal with Standard Multiplex Composite Input Signal.

FIGURE 3 — DISTORTION COMPONENTS IN AUDIO SIGNAL

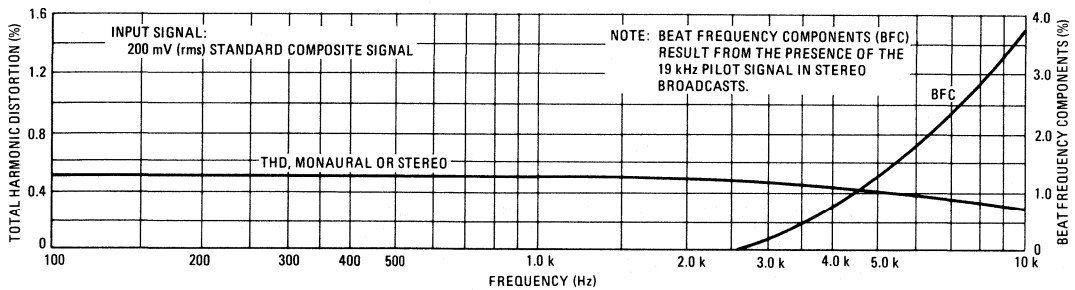


FIGURE 4 – TOTAL HARMONIC DISTORTION

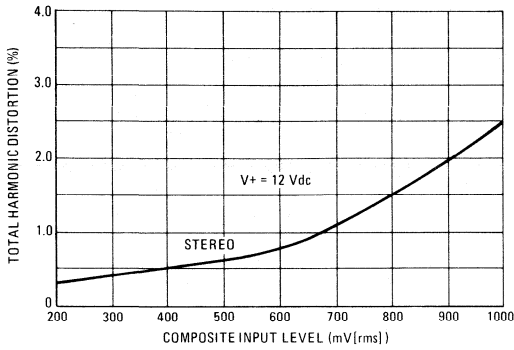


FIGURE 5 – MULTIPLEX SENSITIVITY

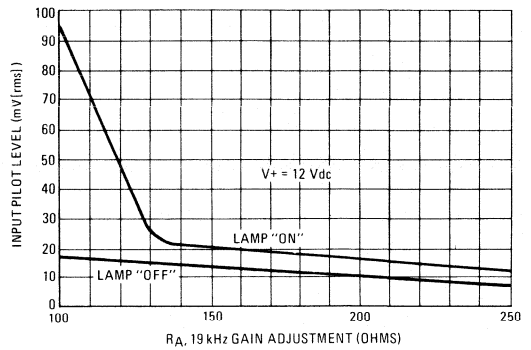


FIGURE 6 – CHANNEL SEPARATION

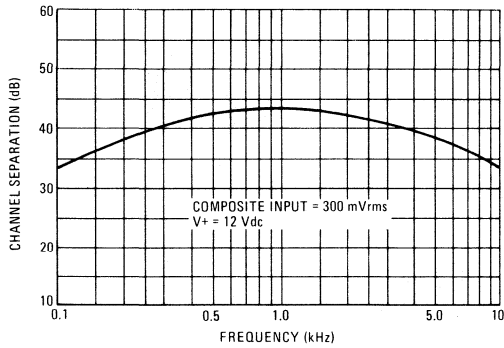
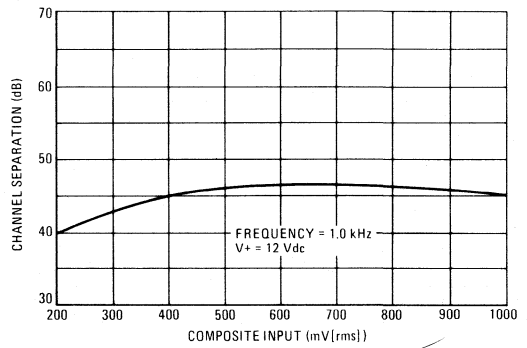


FIGURE 7 – CHANNEL SEPARATION



MC1310P

STEREO DEMODULATOR

FM STEREO DEMODULATOR

... a monolithic device designed for use in solid-state stereo receivers.

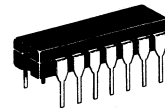
- Requires no Inductors
- Low External Part Count
- Only Oscillator Frequency Adjustment Necessary
- Integral Stereo/Monaural Switch 75 mA Lamp Driving Capability
- Wide Dynamic Range: 560 mV(RMS) maximum Composite Input Signal
- Wide Supply Range: 8-16 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range
- Low Distortion: Typically 0.3% THD at 560 mV (RMS) Composite Input Signal
- Excellent SCA Rejection

FM STEREO DEMODULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Value | Unit |
|---|-------------|------------------|
| Power Supply Voltage | 16 | Volts |
| Lamp Current (nominal rating, 12 V lamp) | 75 | mA |
| Power Dissipation (Package limitation) Derate above $T_A = +25^\circ\text{C}$ | 625 | mW |
| Operating Temperature Range (Ambient) | -40 to +85 | $^\circ\text{C}$ |
| Storage Temperature Range | -65 to +150 | $^\circ\text{C}$ |



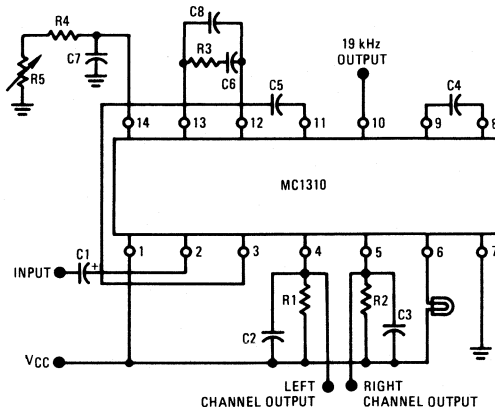
PLASTIC PACKAGE
CASE 646
TO-116

7

FIGURE 1 - TYPICAL APPLICATION

- PIN FUNCTIONS**
- | | |
|------------------------------|--------------------------------|
| Pin 1 = VCC | Pin 8 = Switch Filter |
| Pin 2 = Input | Pin 9 = Switch Filter |
| Pin 3 = Amplifier Output | Pin 10 = 19 kHz Output |
| Pin 4 = Left Channel Output | Pin 11 = Modulator Input |
| Pin 5 = Right Channel Output | Pin 12 = Loop Filter |
| Pin 6 = Lamp Indicator | Pin 13 = Loop Filter |
| Pin 7 = Ground | Pin 14 = Oscillator RC Network |

- PARTS LIST**
- | | |
|-------------------------------------|-------------------------------------|
| C ₁ = 2.0 μF | C ₈ = 0.25 μF |
| C ₂ = 0.02 μF | R ₁ = 3.9 k Ω |
| C ₃ = 0.02 μF | R ₂ = 3.9 k Ω |
| C ₄ = 0.25 μF | R ₃ = 1.0 k Ω |
| C ₅ = 0.05 μF | R ₄ = 16 k Ω |
| C ₆ = 0.5 μF | R ₅ = 5.0 k Ω |
| C ₇ = 470 pF | |



See Packaging Information Section for outline dimensions.

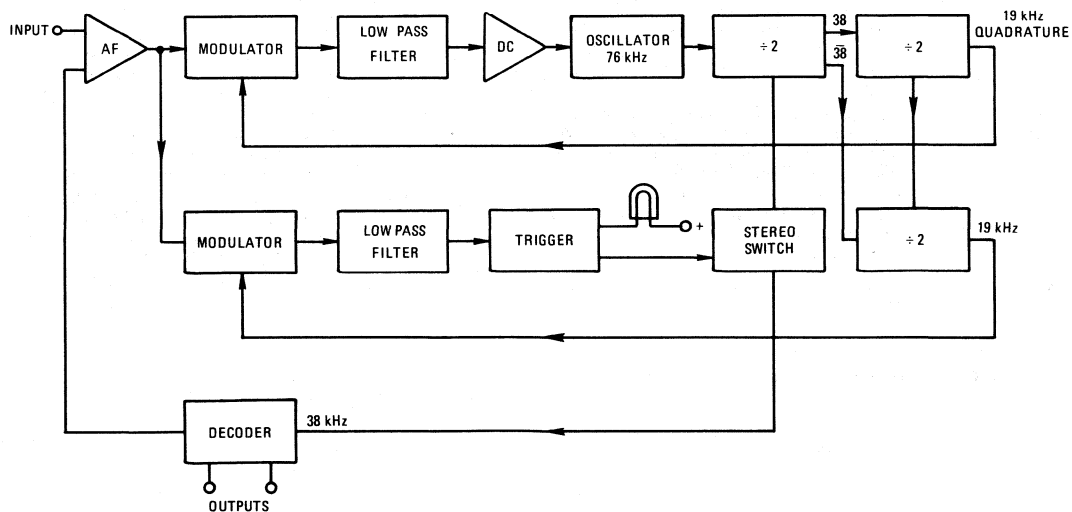
MC1310P (continued)

ELECTRICAL CHARACTERISTICS Unless otherwise noted; $V_{CC}^* = +12 \text{ Vdc}$, $T_A = +25^\circ\text{C}$, 560 mV(RMS) (2.8 Vp-p) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) (10% pilot level), using circuit of Figure 1.

| Characteristic | Min | Typ | Max | Unit |
|---|--------|-----------|-----|------------------|
| Maximum Standard Composite Input Signal (0.5% THD) | 2.8 | — | — | V _{p-p} |
| Maximum Monaural Input Signal (1.0% THD) | 2.8 | — | — | V _{p-p} |
| Input Impedance | — | 50 | — | k Ω |
| Stereo Channel Separation (50 Hz – 15 kHz) | 30 | 40 | — | dB |
| Audio Output Voltage (desired channel) | — | 485 | — | mV(RMS) |
| Monaural Channel Balance (pilot tone "off") | — | — | 1.5 | dB |
| Total Harmonic Distortion | — | 0.3 | — | % |
| Ultrasonic Frequency Rejection | 19 kHz | 34.4 | — | dB |
| | 38 kHz | 45 | — | |
| Inherent SC A Rejection (f = 67 kHz; 9.0 kHz beat note measured with 1.0 kHz modulation "off") | — | 80 | — | dB |
| Stereo Switch Level (19 kHz input level for lamp "on") | 12 | 16 | 20 | mV(RMS) |
| Hysteresis | — | 6.0 | — | dB |
| Capture Range (permissible tuning error of internal oscillator, reference circuit values of Figure 1) | — | ± 3.0 | — | % |
| Operating Supply Voltage (loads reduced to 2.7 k Ω for 8.0-volt operation) | 8.0 | — | 16 | Vdc |
| Current Drain (lamp "off") | — | 13 | — | mAdc |

*Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

FIGURE 2 – SYSTEM BLOCK DIAGRAM



7

CIRCUIT OPERATION

Figure 2, on the previous page, shows the system block diagram. The upper line, comprising the 38-kHz regeneration loop operates as follows: the internal oscillator running at 76-kHz and feeding through two divider stages returns a 19-kHz signal to the input modulator. There the returned signal is multiplied with the incoming signal so that when a 19-kHz pilot tone is received a dc component is produced. The dc component is extracted by the low pass filter and used to control the frequency of the internal oscillator which consequently becomes phase-locked to the pilot tone. With the oscillator phase-locked to the pilot the 38-kHz output from the first divider is in the correct phase for decoding a stereo signal. The decoder is essentially another modulator in which the incoming signal is multiplied by the regenerated 38-kHz signal. The regener-

ated 38-kHz signal is fed to the stereo decoder via an internal stereo switch. The stereo switch closes when a sufficiently large 19-kHz pilot tone is received. The pilot tone level is detected and the switch operated by the stereo switch section of the circuit in the following manner:

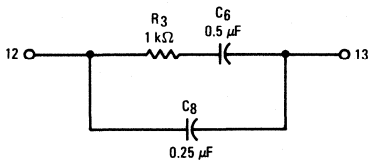
The 19-kHz signal returned to the 38-kHz regeneration loop modulator is in quadrature with the 19-kHz pilot tone when the loop is locked. With a third divider state appropriately connected, a 19-kHz signal in phase with the pilot tone is generated. This is multiplied with the incoming signal in the stereo switch modulator yielding a dc component proportional to the pilot tone amplitude. This component after filtering is applied to the trigger circuit which activates both the stereo switch and an indicator lamp.

APPLICATIONS INFORMATION
(Component numbers refer to Figure 1)

External Component Functions and Values

- C₁ Input coupling capacitor; 2.0 μF is recommended but a lower value is permissible if reduced separation at low frequencies is acceptable.
- R₁, R₂, C₂, C₃ Loads and de-emphasis capacitors, maximum permissible load resistors are related to minimum supply voltage as follows:
 Min Supply 8.0 10 12 Volts
 Max Load 2.7 4.3 6.2 Kilohms
 (±10% Tolerance)
- C₄ Filter capacitor for stereo switch level detector; time constant is C₄ x 53 kilohms ±30%, maximum dc voltage appearing across C₄ is 0.25 V (pin 8 positive) at 100 mV(RMS) pilot level. The signal voltage across C₄ is negligible.
- C₅ Internal coupling capacitor to modulators; 0.05 μF is recommended. This gives 1.75° phase lead at 19 kHz.
- R₃, C₆, C₈ Phase-lock loop filter components; the following network is recommended:

- R₄, R₅, C₇ Oscillator timing network, recommended values:
 C₇ = 470 pF 1%
 R₄ = 16 kΩ 1%
 R₅ = 5 kΩ Preset
 These values give ±3% typical capture range. Capture range may be increased by reducing C₇ and increasing R₄, R₅ proportionally but at the cost of increased beat-note distortion (due to oscillator-phase jitter) at high-signal levels.
- Stereo Lamp Nominal rating up to 75 mA at 12 V; the circuit includes surge limiting which restricts cold-lamp current to approximately 250 mA.
- 19 kHz-Output A buffered output providing a 3.0 V_{PK} positive-going square wave at 19 kHz is available at pin 10. A frequency counter may be connected to this point to measure the oscillator free-running frequency for alignment.



When less performance is required a simpler network consisting of R₃ = 100 ohms and C₆ = 0.25 μF may be used (omit C₈).

APPLICATIONS INFORMATION (continued)

External Monaural/Stereo Switching

The circuit can be maintained in monaural mode by connecting pin 8 negative or pin 9 positive by 0.3 V. Pin 8 may be grounded directly if desired. The dc impedance at pins 8 and 9 is 28 kilohms $\pm 30\%$. Note that the voltage across C_4 increases to 2.2 V with pin 9 positive when pin 8 is grounded.

Oscillator Killing

In AM-FM receivers it may be desirable to kill the 76-kHz internal oscillator during AM reception to prevent interference. This may be accomplished by either grounding pin 14 or by connecting it to the positive line via a current limiting resistor (3.3 kilohms is recommended).

Phase Compensation

Phase-shifts in the circuit cause the regenerated 38-kHz sub-carrier to lead the original 38 kHz by approximately 2° . The coupling capacitor C_5 generates an additional lead of 3.5° (for $C_5 = 0.05 \mu\text{F}$) giving a total lead of 5.5° .

It may be desirable that the regenerated 38 kHz lead or lag the original to compensate for receiver IF characteristics. Further

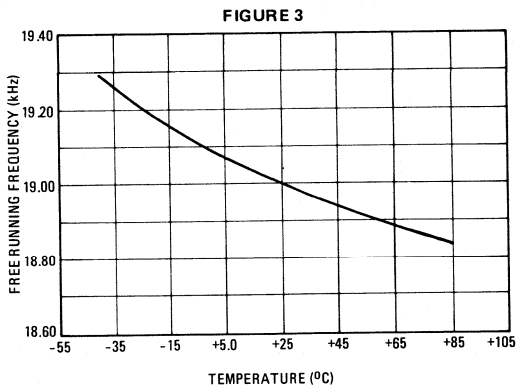
phase lead can be obtained if required by reducing C_5 , which couples into a 5.0-kilohm load.

The circuit is so designed that phase lag may be generated by adding a capacitor from pin 3 to ground. The source resistance at this point is 500 ohms. A capacitance of 820 pF compensates the 5.5° phase lead: increase above this value causes the regenerated sub-carrier to lag the original.

Note that these phase shifts occur within the phase-lock loop and affect only the regenerated 38-kHz sub-carrier: the circuit causes no significant phase or amplitude variation in the actual stereo signal prior to decoding.

Voltage Control Oscillator Compensation

Figure 3 illustrates uncompensated Oscillator Drift versus temperature. The recommended T_C of the R_4, R_5, C_7 combination is -200 ppm. This will hold the oscillator drift to approximately $\pm 0.5\%$ over a temperature range of -30 to $+85^\circ\text{C}$. Acceptable performance is obtained with up to 2.5% oscillator detuning, which with the compensation given above, allows $\pm 2\%$ for aging of the timing components.



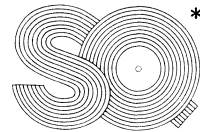
MC1312P MC1313P

MONOLITHIC CBS SQ* DECODER

... a matrix system designed to decode an SQ* encoded program into four separate channels. These devices conform to specifications for decoding quadraphonic records produced by the largest record companies in the world.

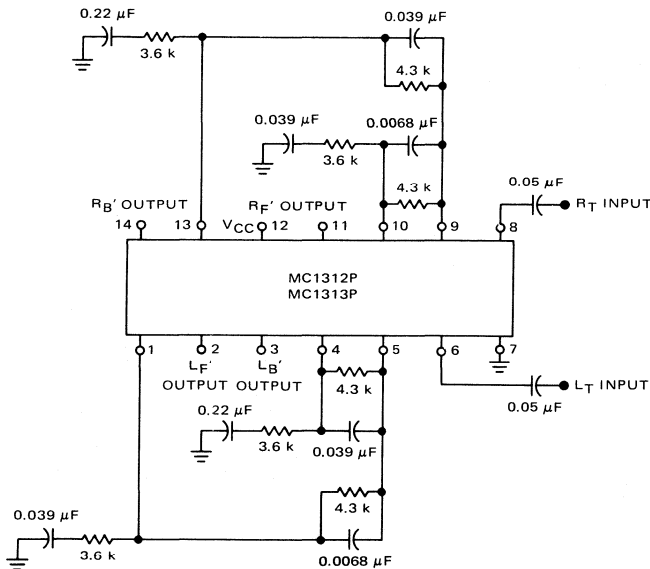
- Both Home Entertainment (MC1312) and Automotive (MC1313) Versions Available
- High Input Impedance
MC1312P – 3.0 Megohms typ, MC1313P – 1.8 Megohms typ
- Low Harmonic Distortion
MC1312P – 0.1% typ, MC1313P – 0.25% typ
- High Signal Handling Capability
MC1312P – 2.0 V(RMS) min, MC1313P – 0.8 V(RMS) min
- MC1313 Provides Excellent Performance at $V_{CC} = +8.0$ Vdc

FOUR-CHANNEL
SQ* DECODER
MONOLITHIC SILICON
INTEGRATED CIRCUIT



This component is sold without patent indemnity and any infringement resulting from use or resale thereof shall be the sole responsibility of purchaser and shall not be the responsibility of manufacturer or distributor even though such use is in accordance with manufacturer's recommendations.

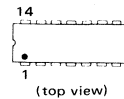
FIGURE 1 – TYPICAL APPLICATION CIRCUIT



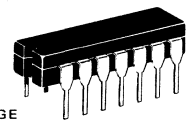
Note: For optimum performance $\pm 5\%$ tolerance components are recommended with the exception of the input capacitors.

DEFINITIONS

| | |
|---------------------|---------------------|
| L_T = Left total | R_T = Right total |
| L_F = Left front | L_B = Left back |
| R_F = Right front | R_B = Right back |



PLASTIC PACKAGE
CASE 646
TO-116



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

*Trademark of Columbia Broadcasting Systems, Inc.
See Packaging Information Section for outline dimensions.

MC1312P, MC1313P (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

| Rating | Value | Unit |
|--|--------------------|------------------------|
| Power Supply Voltage | 25 | Vdc |
| Power Dissipation (Package Limitation) | 625 | mW |
| Derate above T _A = +25°C | 5.0 | mW/°C |
| Operating Temperature Range | MC1312P MC1313P | 0 to +75 -40 to +85 |
| Storage Temperature Range | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V_{CC} for MC1312P = +20 Vdc, V_{in} = 0.5 V(RMS), for MC1313P V_{CC} = +12 Vdc, V_{in} = 0.2 V(RMS), T_A = +25°C unless otherwise noted.) (See Figure 3.)

| Characteristic | Min | Typ | Max | Unit | |
|---|--------------------|------------|-------------|------------|--------|
| Supply Current Drain | MC1312P MC1313P | 11 6.5 | 16 9.0 | 21 12.5 | mA |
| Input Impedance | MC1312P MC1313P | 1.8 1.0 | 3.0 1.8 | — | MΩ |
| Output Impedance | — | 5.0 | — | — | kΩ |
| Channel Balance (L _F /R _F) | -1.0 | 0 | +1.0 | dB | |
| Voltage Gain L _F /L _T or R _F /R _T | -1.0 | 0 | +1.0 | dB | |
| Relative Voltage Gain L _B '/L _F ', R _B '/L _F ', L _B '/R _F ', R _B '/R _F ' L _F ' measurements made with L _T input, R _F ' measurements made with R _T input. | -2.0 | -3.0 | -4.0 | dB | |
| Maximum Input Voltage for 1%THD at Output | MC1312P MC1313P | 2.0 0.8 | — — | — — | V(RMS) |
| Total Harmonic Distortion | MC1312P MC1313P | — — | 0.1 0.25 | — — | % |
| Signal to Noise Ratio (Short-Circuit Input V _O = 0.5 V(RMS) MC1312P with Output Noise Referenced to Output V _O = 0.2 V(RMS) MC1313P Voltage, V _O) (BW = 20 Hz to 20 kHz) | — | — | 80 74 | — — | dB |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

TYPICAL CHARACTERISTICS

FIGURE 2 – CURRENT DRAIN

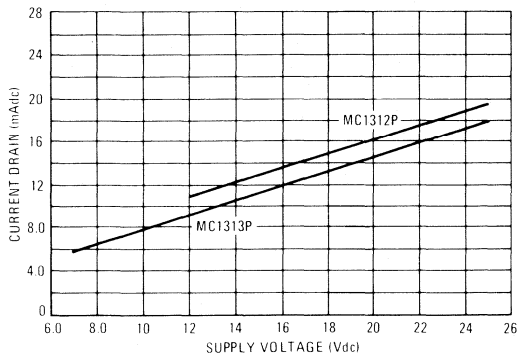
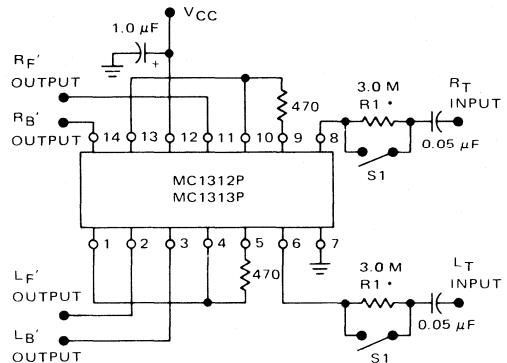


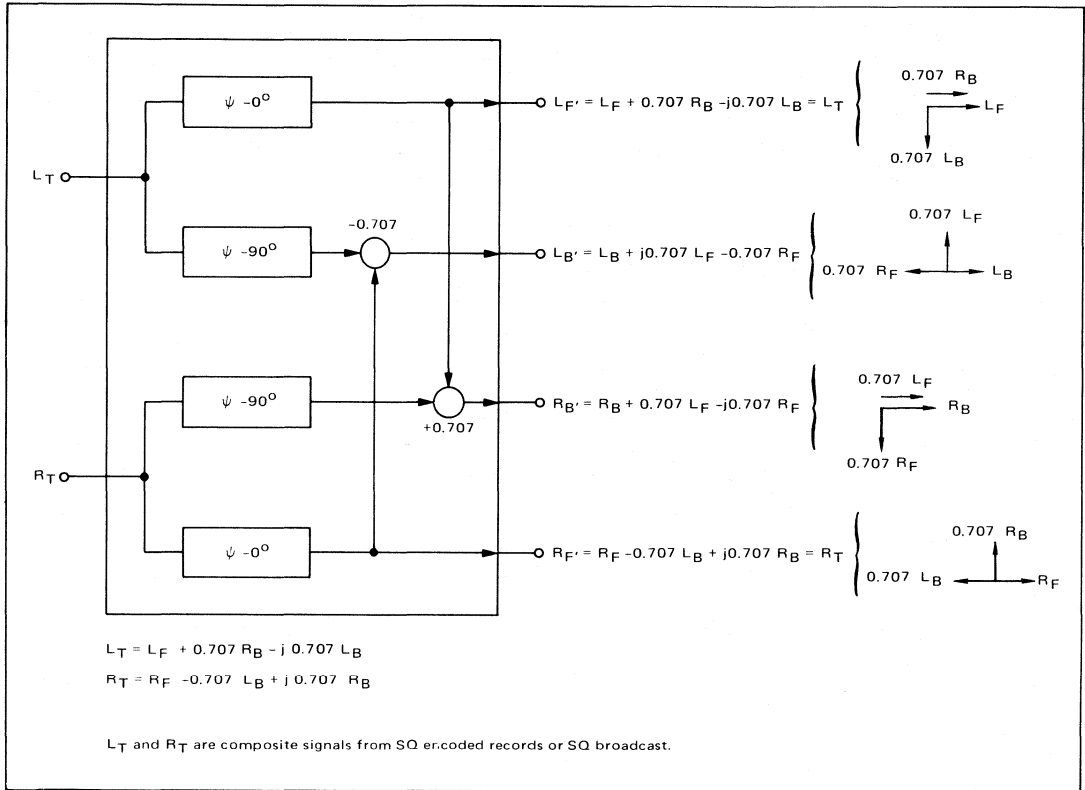
FIGURE 3 – TEST CIRCUIT



* R1 is used for input impedance measurement.
S1 is normally closed.

APPLICATIONS INFORMATION

FIGURE 4 – DECODING PROCESS DIAGRAM



7

The decoding process is shown schematically in Figure 4. The MC1312P/MC1313P circuits that perform this function consists of two preamplifiers which are fed with left total, L_T , and right total, R_T , signals. The preamplifiers each feed two all-pass* networks that are used to generate two L_T signals in quadrature and two R_T signals in quadrature. The four signals are matrixed to yield left-front, left-back, right-front, and right-back signals (L_F' , L_B' , R_F' , R_B').

The all-pass networks are of the Wein bridge form with the resistive arms realized in the integrated circuit and the RC arms formed by external components. The values shown in Figure 1 are for a 100-Hz to 10-kHz bandwidth and a phase ripple of $\pm 8.5^\circ$ on a 90° phase difference.

It is generally desirable to enhance center-front to center-back separation. This is accomplished by connecting a resistor between pins 2 and 11 (front outputs) and a resistor between pins 3 and 14 (back outputs). For a 10% front channel blending† and a 40% back channel blending†, 47 kilohms between pins 2 and 11 and 7.5 kilohms between pins 3 and 14 is required.

$$\begin{aligned} \dagger R_F'' &= 0.9 R_F' + 0.1 L_F' \\ L_F'' &= 0.9 L_F' + 0.1 R_F' \\ R_B'' &= 0.6 R_B' + 0.4 L_B' \\ L_B'' &= 0.6 L_B' + 0.4 R_B' \end{aligned}$$

*An all-pass network produces phase shift without amplitude variations.

DUAL CHROMA DEMODULATOR

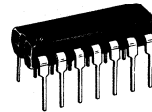
MC1326

DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B MATRIX AND CHROMA DRIVER STAGES

... a monolithic device designed for use in solid-state color television receivers.

- Luminance Input Provided
- Good Chroma Sensitivity – 0.3 Vp-p Input for 5 Vp-p Output
- Low Differential Output DC Offset Voltage – 0.6 V max
- DC Temperature Stability – 3 mV/°C typ
- Negligible Change in Output Voltage Swing with Varying 3.58 MHz Reference Input Signal
- High Ripple Rejection Achieved with MOS Filter Capacitors
- High Blue Output Voltage Swing – 10 Vp-p typ
- Blanking Input Provided

DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B OUTPUT MATRIX MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



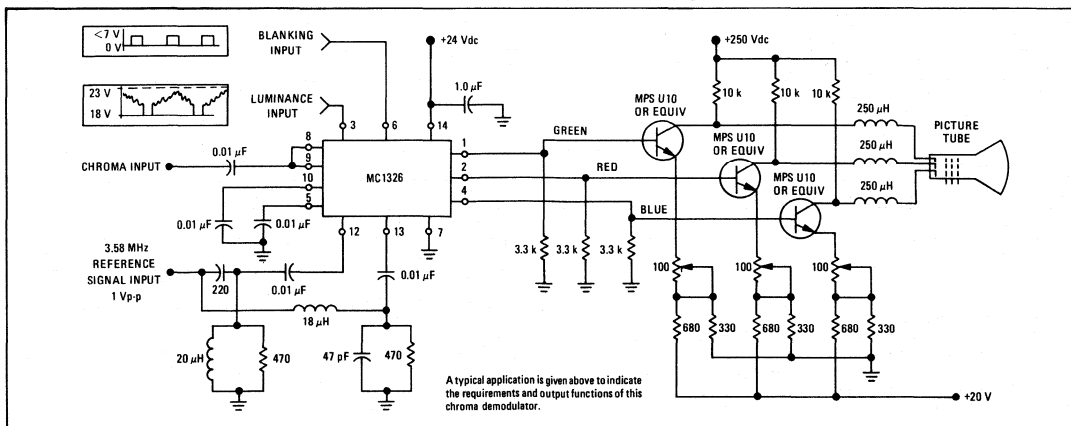
PQ SUFFIX
PLASTIC PACKAGE
CASE 647

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Value | Unit |
|--|-------------|-------------|
| Power Supply Voltage | 30 | Vdc |
| Chroma Signal Input Voltage | 5.0 | Vpk |
| Reference Signal Input Voltage | 5.0 | Vpk |
| Minimum Load Resistance | 3.0 | k ohms |
| Luminance Input Voltage | 12 | Vp-p |
| Blanking Input Voltage | 7.0 | Vp-p |
| Power Dissipation (Package Limitation) Plastic Packages Derate above $T_A = +25^\circ\text{C}$ | 625 5.0 | mW mW/°C |
| Operating Temperature Range (Ambient) | 0 to +75 | °C |
| Storage Temperature Range | -65 to +150 | °C |

Maximum Ratings as defined in MIL-S-19500, Appendix A.

FIGURE 1 – MC1326 TYPICAL APPLICATION



See Packaging Information Section for outline dimensions.

MC1326 (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = 24 \text{ Vdc}$, $R_L = 3.3 \text{ k ohms}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Pin No. | Min | Typ | Max | Unit |
|--|----------------------|------------|-------------|------------|----------------------|
| STATIC CHARACTERISTICS | | | | | |
| Quiescent Output Voltage See Figure 2 | 1, 2, 4 | 13 | 14.4 | 16 | Vdc |
| Quiescent Input Current from Supply (Figure 2) ($R_L = \infty$) ($R_L = 3.3 \text{ k ohms}$) | | — 16.5 | 6.0 19 | — 25.5 | mA |
| Reference Input DC Voltage (Figure 2) | 5,12,13 | — | 6.2 | — | Vdc |
| Chroma Reference Input DC Voltage (Figure 2) | 8,9,10 | — | 3.4 | — | Vdc |
| Differential Output Voltage (Reference Input Voltage = 1.0 Vp-p) See Note 1 and Figure 3 | 1, 2, 4 | — | 0.3 | 0.6 | Vdc |
| Output Voltage Temperature Coefficient (Reference Input Voltage = 1.0 Vp-p, $+25^\circ$ to $+65^\circ\text{C}$) See Note 1 and Figure 3 | 1, 2, 4 | — | 3.0 | — | mV/ $^\circ\text{C}$ |
| DYNAMIC CHARACTERISTICS ($V^+ = 24 \text{ Vdc}$, $R_L = 3.3 \text{ k ohms}$, Reference Input Voltage = 1.0 Vp-p, $T_A = +25^\circ\text{C}$ unless otherwise noted) | | | | | |
| Blue Output Voltage Swing See Note 2 and Figure 4 | 4 | 8.0 | 10 | — | Vp-p |
| Chroma Input Voltage (B Output = 5.0 Vp-p) See Note 3 and Figure 4 | 8 | — | 0.3 | 0.7 | Vp-p |
| Luminance Input Resistance | 3 | 100 | — | — | k Ω |
| Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz) | 1, 2, 4 | — — | 0.95 0.5 | — — | — |
| Blanking Input Resistance 1.0 Vdc 0 Vdc | 6 | — — | 1.1 75 | — — | k Ω |
| Detected Output Voltage (Adjust B Output to 5.0 Vp-p, Luminance Voltage = 23 V) See Note 4 | 4 | | | | Vp-p |
| | G Output R Output | 1 2 | 0.75 3.5 | 1.0 3.8 | 1.25 4.2 |
| Relative Output Phase (B Output = 5.0 Vp-p, Luminance Voltage = 23 V) B to R Output B to G Output | 4, 2 4, 1 | 101 248 | 106 256 | 111 264 | Degrees |
| | | | | | |
| Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage) | 1, 2, 4 | — | 250 | 500 | mVp-p |
| B-Y Phase Shift (B-Y Reference Input to B-Y Output) | 4, 13 | — | 3 | — | Degrees |
| Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B Output = 5.0 Vp-p) | 1, 2, 4 | — | 0.7 | 1.5 | Vp-p |
| Reference Input Resistance (Chroma Input = 0) | 12, 13 | — | 2.0 | — | k Ω |
| Reference Input Capacitance (Chroma Input = 0) | 12, 13 | — | 6.0 | — | pF |
| Chroma Input Resistance | 8, 9, 10 | — | 2.0 | — | k Ω |
| Chroma Input Capacitance | 8, 9, 10 | — | 2.0 | — | pF |

NOTES:

1. With Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage = 1.0 Vp-p, all output voltages will be within specified limits and will not differ from each other by greater than 0.6 Vdc.
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 0.6 Vp-p.
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5 Vp-p. The Chroma Input Voltage at this point should be equal to or less than 0.7 Vp-p.
4. With normal Reference Input Signal Voltage, adjust the Chroma Input Signal until the Blue Output Voltage = 5 Vp-p. At this point, the Red and Green voltages will fall within the specified limits.

TEST CIRCUITS

($V^+ = 24 \text{ Vdc}$, $R_L = 3.3 \text{ Kilohms}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 2 – DC TEST CIRCUIT WITHOUT REFERENCE INPUT SIGNAL VOLTAGE (B-Y AND R-Y)
(For Testing Quiescent Current, DC Output Voltage, Difference Voltage)

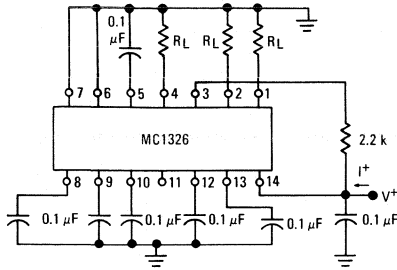


FIGURE 3 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

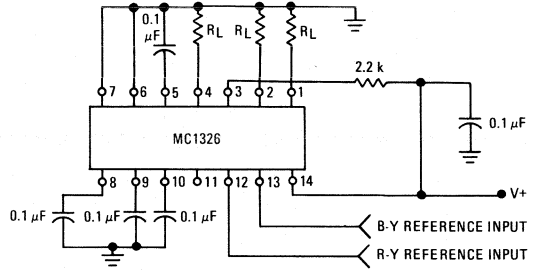


FIGURE 4 – DYNAMIC TEST CIRCUIT

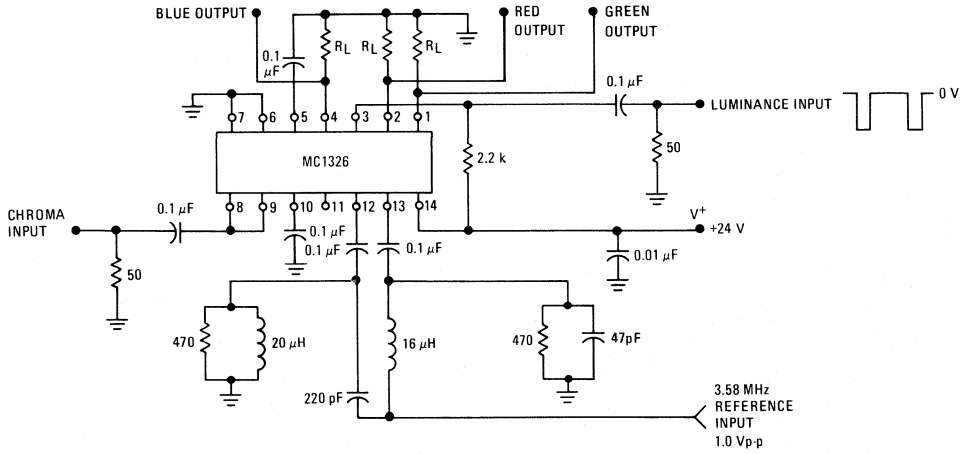
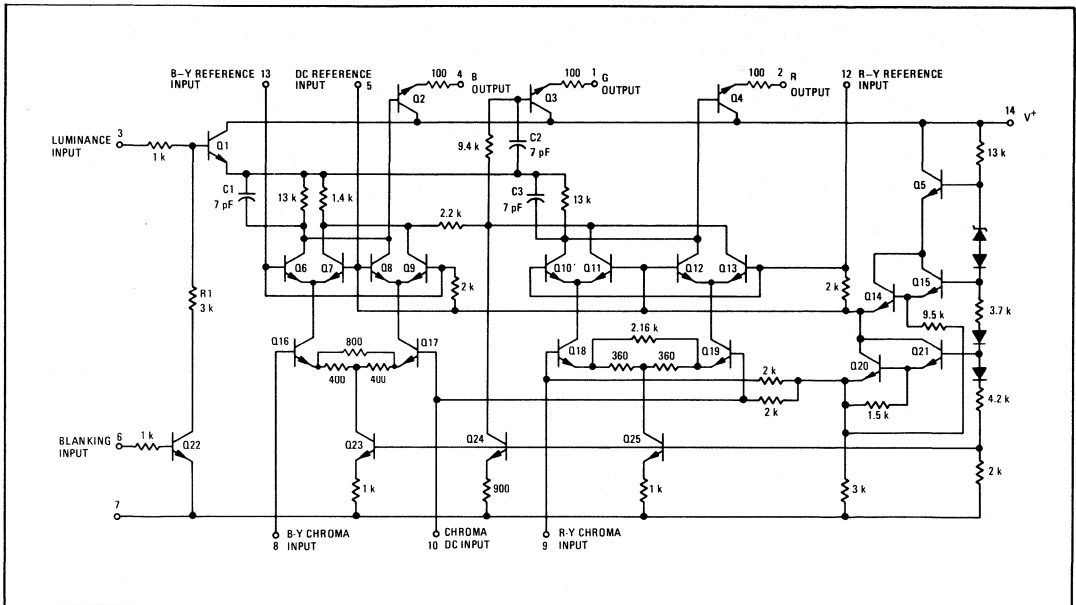


FIGURE 5 — CIRCUIT SCHEMATIC



CIRCUIT OPERATION

A double sideband suppressed carrier chroma signal flows between the bases of the two differential pairs, Q16 and Q17, Q18 and Q19. A reference signal of approximately 1 Vp-p amplitude having the same frequency as the suppressed chroma carrier with an appropriate phase relationship is supplied between the bases of the upper differential pairs Q6 and Q7, Q8 and Q9, Q10 and Q11, Q12 and Q13. The upper pairs are switched between full conduction and zero conduction at the carrier frequency rate. The collectors of the upper pairs are cross-coupled so that "doubly balanced" or "full-wave" synchronous detected chroma signals are obtained. Both positive and negative phases of the detected signal are available at opposite collector pairs.

While the detector section is almost identical to other available units, several excellent additional features are incorporated. Transistor Q1 is used as an emitter follower to which the collector load resistors of the detectors are returned. The collector impedances of the upper pair transistors are high compared with the collector load resistors, and any signal at the emitter of Q1 appears virtually unattenuated at the collectors of the upper pairs, and hence at the three detector output terminals. This feature may be used to mix the correct amount of the luminance portion of the color TV signal with the color difference signals produced by the detectors to give R-G-B outputs directly.

Capacitors C1, C2, and C3 compensate for most of the high frequency roll-off in the luminance signal. This is due to the collector capacitances of the detector transistors and the input capacitances of the emitter followers, Q2, Q3, Q4. Capacitors C1, C2, and C3 provide filtering of carrier harmonics from the detected color difference signals. This increases the available swing before clipping for the color difference signal, and reduces the high frequency components which must pass through the emitter followers (Q2, Q3, Q4) into the video output stages. Since high capacitance (>100 pF) is characteristic of the input impedance of a video output stage, the transistor emitter followers must operate at a

high quiescent current (>5 mA) in order to pass large high frequency components without distortion. The filtering reduces the quiescent current required in the emitter followers and thus reduces dissipation in the integrated circuit.

If it is not required to mix the luminance signal via Q1, this transistor can be used for brightness control. If the base of Q1 is connected to a suitable variable dc voltage, this will vary the dc output levels of the three detected outputs accordingly and thereby vary the picture brightness level.

Blanking of the picture during line and frame flyback may be achieved by applying a positive-going blanking signal to the base of Q22. With an extra external resistor in series with the Q1 base of approximately 5 k ohms, when Q22 is turned on by the blanking pulse, the base of Q1 will be pulled negative by the current in R1, thus forcing all three detected outputs to go negative by the same amount. In a conventional solid-state receiver with a single video output stage driving the picture tube cathode, a negative-going signal at the base of the video output stage will blank the picture tube. When using the blanking input be certain the blanking pulse does not switch off the luminance input stage Q1 completely; this would turn off the collector supply for the demodulators and put the entire chroma demodulator out of lock at each blanking pulse.

Matrix for MC1326

$$\frac{R-Y \text{ gain}}{B-Y \text{ gain}} = 0.77$$

$$-G-Y = 0.11 (B-Y) + 0.28 (R-Y)$$

For indicated requirements and output functions of the MC1326 chroma demodulator please refer to the typical application shown on the first page of this specification.

TYPICAL CHARACTERISTICS
($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

(Figures 6 through Figure 10 Reference Test Circuit of Figure 2)

FIGURE 6 – DC OUTPUT VOLTAGE

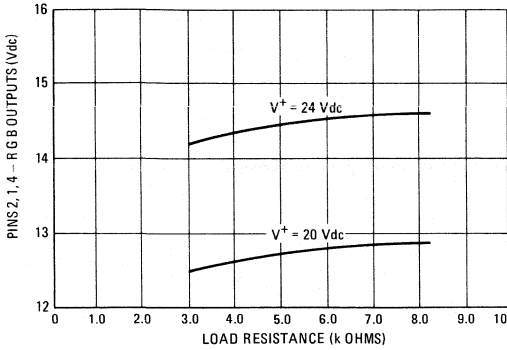


FIGURE 7 – POWER DISSIPATION

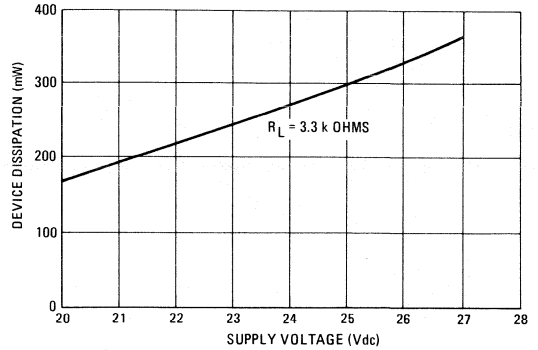


FIGURE 8 – DC OUTPUT VOLTAGE

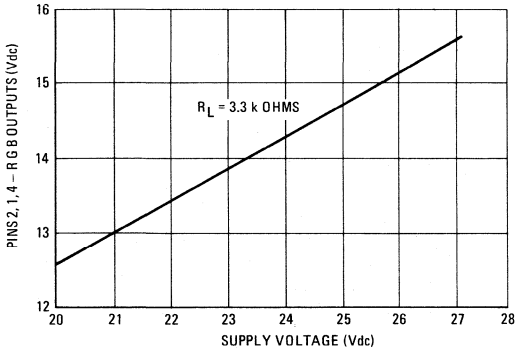


FIGURE 9 – POWER DISSIPATION

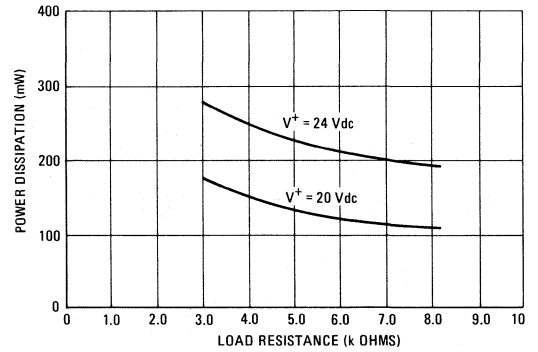


FIGURE 10 – DC OUTPUT VOLTAGE

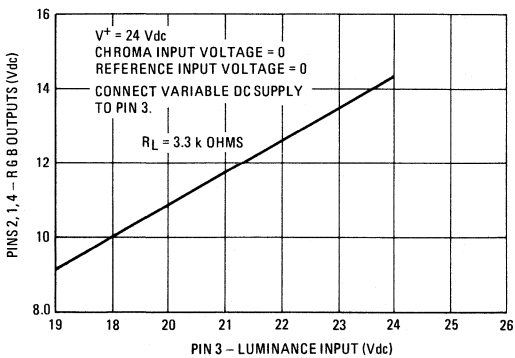
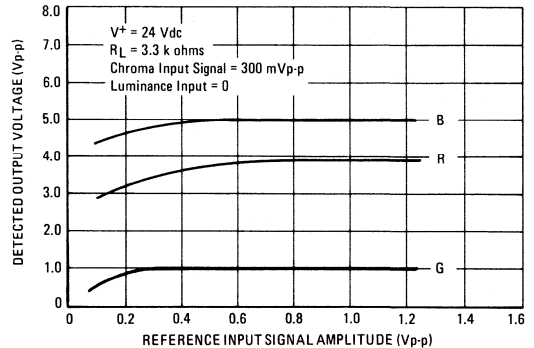


FIGURE 11 – DETECTED OUTPUT VOLTAGE
(Reference Test Circuit of Figure 4)



TYPICAL CHARACTERISTICS (continued)
 (T_A = +25°C unless otherwise noted)

(Figures 12 through Figure 17 Reference Test Circuit of Figure 4)

FIGURE 12 – OUTPUT VOLTAGE

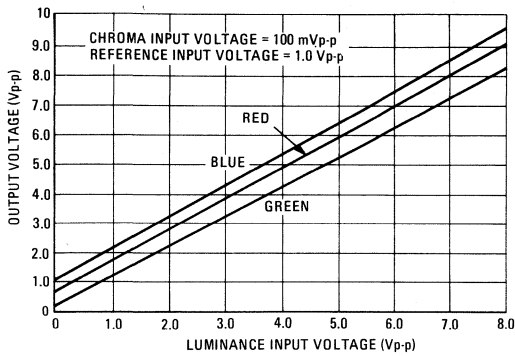


FIGURE 13 – GREEN OUTPUT

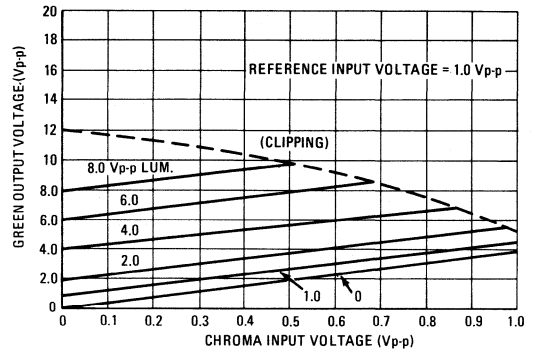


FIGURE 14 – RED OUTPUT

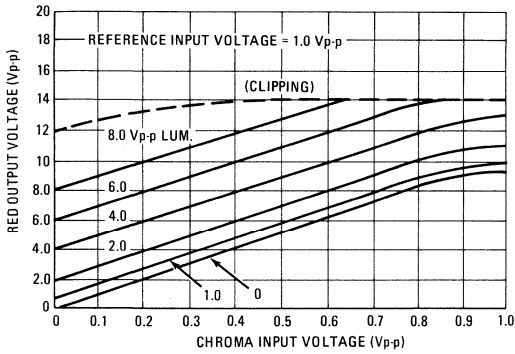


FIGURE 15 – BLUE OUTPUT

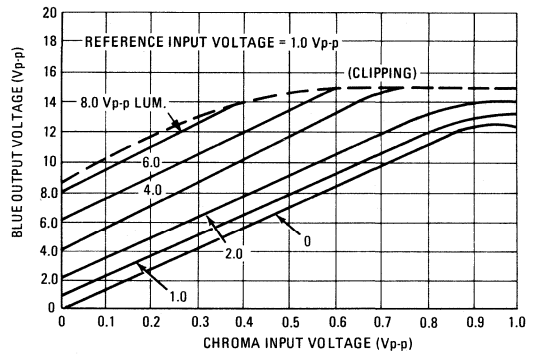


FIGURE 16 – LUMINANCE BANDWIDTH

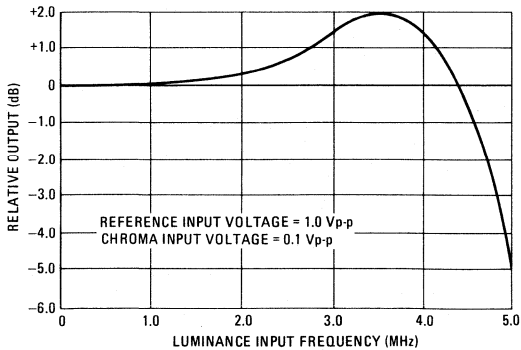
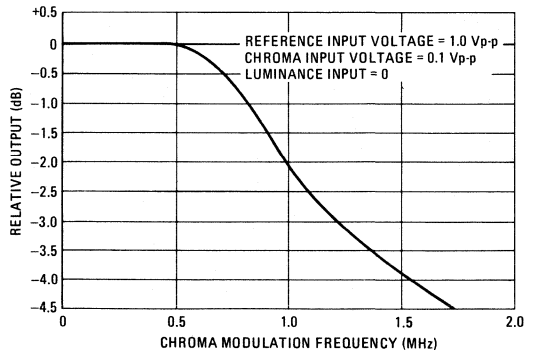


FIGURE 17 – CHROMA BANDWIDTH



7

MC1327

CHROMA DEMODULATOR

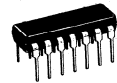
DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH RGB MATRIX, PAL SWITCH, AND CHROMA DRIVER STAGES

... a monolithic device designed for use in solid-state color television receivers.

- Good Chroma Sensitivity – 0.28 Vp-p Input Typical for 5.0 Vp-p Output
- Low Differential Output DC Offset Voltage – 0.6 V Maximum
- Differential DC Temperature Stability – 0.7 mV/°C
- High Blue Output Voltage Swing – 10 Vp-p Typical
- Blanking Input Provided
- Luminance Bandwidth Greater than 5.0 MHz

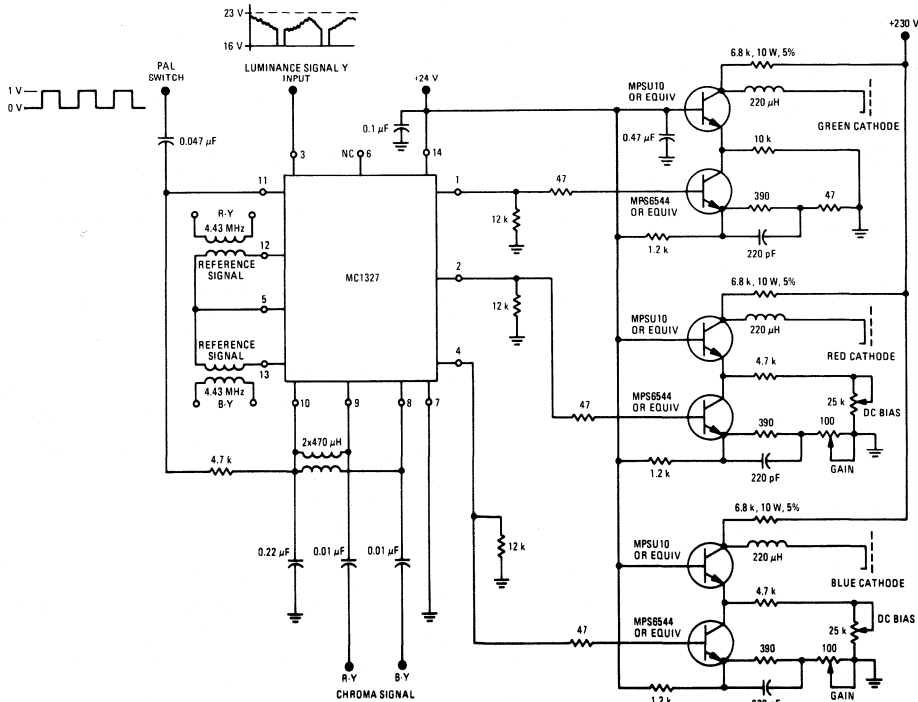
DUAL DOUBLY BALANCED CHROMA DEMODULATOR with RGB OUTPUT MATRIX AND PAL SWITCH MONOLITHIC SILICON INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



See Packaging Information Section for outline dimensions.

MC1327 (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Value | Unit |
|---|-------------|------------------|
| Power Supply Voltage | 30 | Vdc |
| Chroma Signal Input Voltage | 5.0 | V _{pk} |
| Reference Signal Input Voltage | 5.0 | V _{pk} |
| Minimum Load Resistance | 3.0 | k ohms |
| Luminance Input Voltage | 12 | V _{p-p} |
| Blanking Input Voltage | 7.0 | V _{p-p} |
| Power Dissipation (Package Limitation) Plastic Packages Derate above T _A = +25°C | 625 5.0 | mW mW/°C |
| Operating Temperature Range (Ambient) | -20 to +75 | °C |
| Storage Temperature Range | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3.3 k ohms, T_A = +25°C unless otherwise noted)

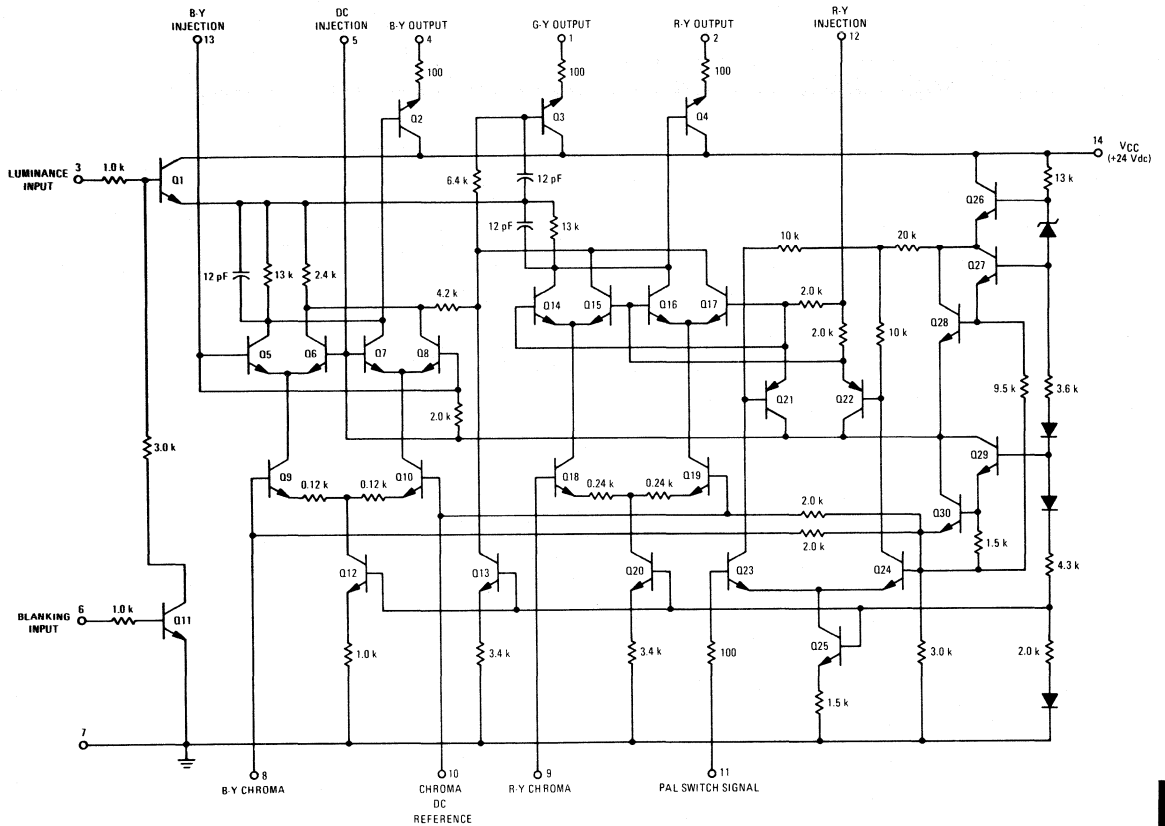
| Characteristic | Pin No. | Min | Typ | Max | Unit |
|---|---------|---------|-----------|---------|-------|
| STATIC CHARACTERISTICS | | | | | |
| Quiescent Output Voltage (See Figure 2) | 1,2,4 | 13.2 | 14.5 | 15.8 | Vdc |
| Quiescent Input Current from Supply (Figure 2) (R _L = ∞) (R _L = 3.3 k ohms) | | – 16 | 7.5 19 | – 26 | mA |
| Reference Input DC Voltage (Figure 2) | 5,12,13 | – | 6.2 | – | Vdc |
| Chroma Reference Input DC Voltage (Figure 2) | 8,9,10 | – | 3.4 | – | Vdc |
| Differential Output Voltage (See Note 1 and Figure 2) | 1,2,4 | – | 0.3 | 0.6 | Vdc |
| Differential Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C) | 1,2,4 | – | 0.7 | – | mV/°C |
| Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C) | 1,2,4 | – | +0.5 | ±5.0 | mV/°C |

DYNAMIC CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3.3 k ohms, Reference Input Voltage = 1.0 V_{p-p}, T_A = +25°C unless otherwise noted)

| | | | | | |
|--|----------------------|--------|--------------|------------|-------------------|
| Blue Output Voltage Swing (See Note 2 and Figure 3) | 4 | 8.0 | 10 | – | V _{p-p} |
| Chroma Input Voltage (B Output = 5.0 V _{p-p}) (See Note 3 and Figure 3) | 8 | – | 280 | 550 | mV _{p-p} |
| Luminance Input Resistance | 3 | 100 | – | – | kΩ |
| Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz, reference at 100 kHz) | 1,2,4 | – – | 0.95 –1.8 | – – | – dB |
| Differential Luminance Gain, RGB Outputs (@ 5.0 MHz) | | – | 0.3 | – | dB |
| Blanking Input Resistance (1.0 Vdc) (0 Vdc) | 6 | – – | 1.1 75 | – – | kΩ |
| Detected Output Voltage (Adjust B Output to 5.0 V _{p-p} , Luminance Voltage = 23 V) (See Note 4) | 4 | | | | V _{p-p} |
| | G Output R Output | 1 2 | 1.4 2.5 | 1.8 2.9 | 2.2 3.3 |
| PAL Switch Operating Voltage Range (7.8 kHz Square Wave) | 11 | 0.3 | – | 3.0 | V _{p-p} |
| R-Y Output dc Offset with PAL Switch Operation | | – | – | 100 | mVdc |
| Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage) | 1,2,4 | – | 200 | 300 | mV _{p-p} |
| Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B Output = 5.0 V _{p-p}) | 1,2,4 | – | 0.6 | 1.0 | V _{p-p} |
| Reference Input Resistance (Chroma Input = 0) | 12,13 | – | 2.0 | – | kΩ |
| Reference Input Capacitance (Chroma Input = 0) | 12,13 | – | 6.0 | – | pF |
| Chroma Input Resistance | 8,9,10 | – | 2.0 | – | kΩ |
| Chroma Input Capacitance | 8,9,10 | – | 2.0 | – | pF |

- NOTES: 1. Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage = 1.0 V_{p-p}.
 2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 1.2 V_{p-p}.
 3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5.0 V_{p-p}.
 4. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5.0 V_{p-p}. At this point, the Red and Green voltages will fall within the specified limits. *Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

MC1327 CHROMA DEMODULATOR (PAL)



TEST CIRCUITS

($V_{CC} = 24 \text{ Vdc}$, $R_L = 3.3 \text{ kilohms}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 2 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

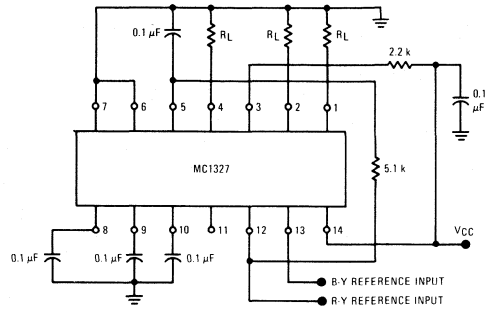
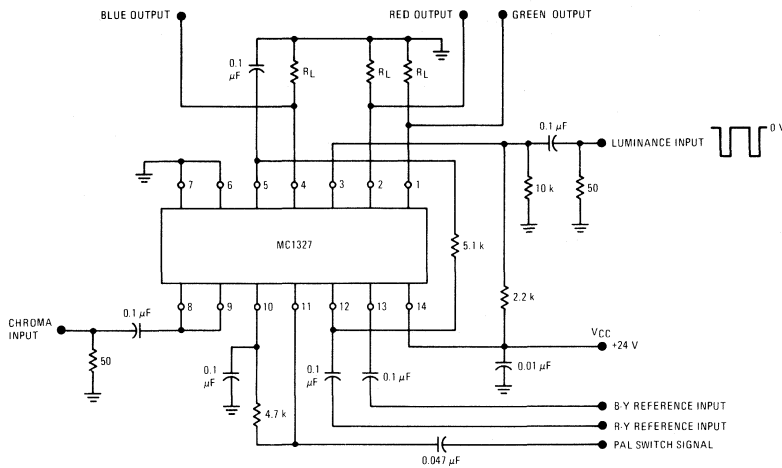


FIGURE 3 – DYNAMIC TEST CIRCUIT



MC1328

DUAL CHROMA DEMODULATOR

MONOLITHIC DUAL DOUBLY BALANCED CHROMA DEMODULATOR

- Good Chroma Sensitivity (0.3 Vp-p Input Produces 5.0 Vp-p Output)
- Good dc Temperature Stability (3 mV/°C typ)
- Low Output dc Offset Voltages (0.6 V max)
- Pin Compatible with ULN-2114, ULN-2114A
- Negligible Change in Output Voltage Swing With Varying 3.58 MHz Reference Signal
- High Ripple Rejection Due To Built-In MOS Filter Capacitors
- High Output Voltage Swing (10 Vp-p Typ) – B-Y

DUAL DOUBLY BALANCED CHROMA DEMODULATOR

Monolithic Silicon Integrated Circuit



G SUFFIX
METAL PACKAGE
CASE 603-02
(TO-100)

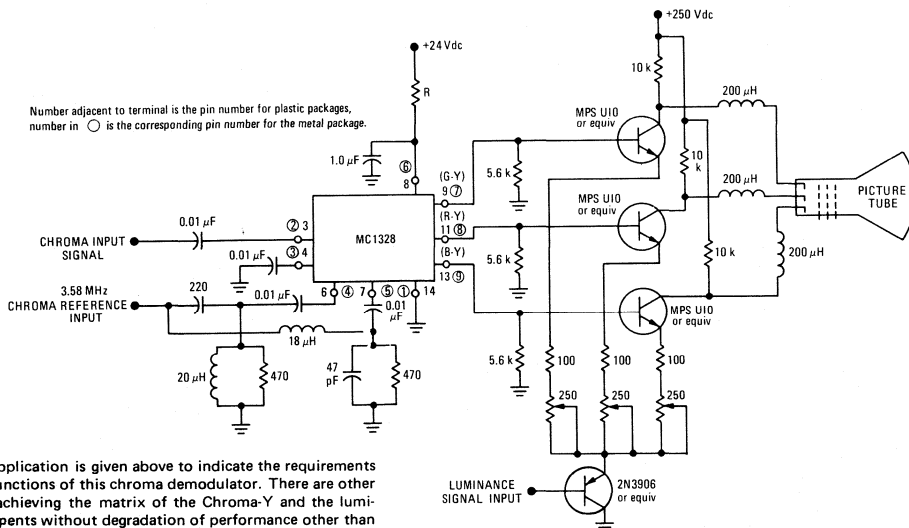


P SUFFIX
PLASTIC PACKAGE
CASE 605
(TO-116)



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – MC1328 TYPICAL APPLICATION



See Packaging Information Section for outline dimensions.

MC1328 (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

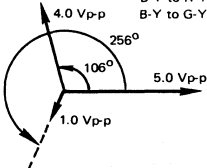
| Rating | Value | Unit |
|--|-------------|--------|
| Power Supply Voltage | 30 | Vdc |
| Power Dissipation (Package Limitation) | | |
| Plastic Packages | 625 | mW |
| Derate above T _A = +25°C | 5.0 | mW/°C |
| Metal Package | 680 | mW |
| Derate above T _A = +25°C | 4.5 | mW/°C |
| Chroma Signal Input Voltage | 5.0 | Vpk |
| Reference Signal Input Voltage | 5.0 | Vpk |
| Minimum Load Resistance | 3.0 | k ohms |
| Operating Temperature Range (Ambient) | 0 to +75 | °C |
| Storage Temperature Range | -65 to +150 | °C |

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V⁺ = 24 Vdc, R_L = 3.3 k ohms, Reference Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

| Characteristic | Pin No. Suffix G Pkg | Pin No. Suffix P, PQ Pkgs | Min | Typ | Max | Unit |
|---|----------------------|---------------------------|-----|------|-----|-------|
| Quiescent Output Voltage See Figure 2 | 7,8,9 | 9,11,13 | 13 | 14.3 | 16 | Vdc |
| Quiescent Input Current (See Figure 2) (R _L = ∞, Chroma and Reference Input Voltages = 0) (R _L = 3.3 k ohms, Chroma and Reference Input Voltages = 0) | 6 | 8 | — | 6.0 | — | mA |
| Reference Input DC Voltage | 4,5 | 6,7 | — | 6.2 | — | Vdc |
| Chroma Input DC Voltage | 2,3 | 3,4 | — | 3.4 | — | Vdc |
| Differential Output Voltage See Note 1 and Figure 3 | 7,8,9 | 9,11,13 | — | 0.3 | 0.6 | Vdc |
| Output Temperature Coefficient (No Output Differential Voltage > 0.6 Vdc, +25°C to +65°C) See Note 1 and Figure 3 | 7,8,9 | 9,11,13 | — | 3.0 | — | mV/°C |

DYNAMIC CHARACTERISTICS (V⁺ = 24 Vdc, R_L = 3.3 k ohms, Referenced Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

| | | | | | | |
|---|------------|---------------|-------------|------------|-------------|---------|
| Detected Output Voltage (B-Y) See Note 2 | 9 | 13 | 8.0 | 9.0 | — | Vp-p |
| Chroma Input Voltage (B-Y Output = 5.0 Vp-p) See Note 3 | 2 | 3 | — | 0.3 | 0.7 | Vp-p |
| Detected Output Voltage (Adjust B-Y Output to 5.0 Vp-p) See Note 4 | 7 8 | 9 11 | 0.75 3.5 | 1.0 3.8 | 1.25 4.2 | Vp-p |
| Relative Output Phase (B-Y Output = 5.0 Vp-p) B-Y to R-Y B-Y to G-Y | 9-8 9-7 | 13-11 13-9 | 101 248 | 106 256 | 111 264 | Degrees |
|  | | | | | | |
| Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage) | 7,8,9 | 9,11,13 | — | 250 | 500 | mVp-p |
| B-Y Phase Shift (B-Y Reference Input to B-Y Output) | 5-9 | 7-13 | — | 3 | — | Degrees |
| Residual Carrier and Harmonics (with Input Signal Voltage, normal Reference Signal Voltage and B-Y = 5.0 Vp-p) | 7,8,9 | 9,11,13 | — | — | 1.5 | Vp-p |
| Reference Input Resistance (Chroma Input = 0) | 4,5 | 6,7 | — | 2.0 | — | k ohms |
| Reference Input Capacitance (Chroma Input = 0) | 4,5 | 6,7 | — | 6.0 | — | pF |
| Chroma Input Resistance | 2,3 | 3,4 | — | 2.0 | — | k ohms |
| Chroma Input Capacitance | 2,3 | 3,4 | — | 2.0 | — | pF |

NOTES:

- With Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage (1.0 Vp-p), all output voltages will be within specified limits and will not differ from each other by greater than 0.6 Vdc.
- With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 0.6 Vp-p.
- With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the B-Y Output Voltage = 5 Vp-p. The Chroma Input Voltage at this point should be equal to or less than 0.7 Vp-p.
- With normal Reference Input Signal Voltage, adjust the Chroma Input Signal until the B-Y Output Voltage = 5 Vp-p. At this point, the R-Y and G-Y voltages will fall within the specified limits.

TEST CIRCUITS

($V^+ = 24$ Vdc, $R_L = 3.3$ k Ω , $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 2 – TEST CIRCUIT WITH NO REFERENCE INPUT SIGNAL

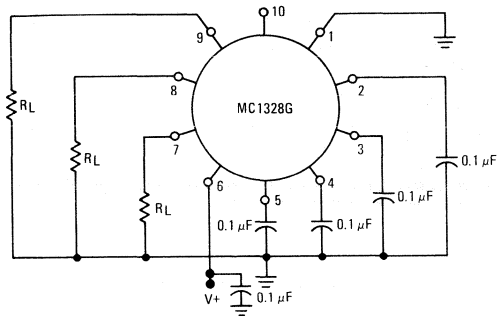
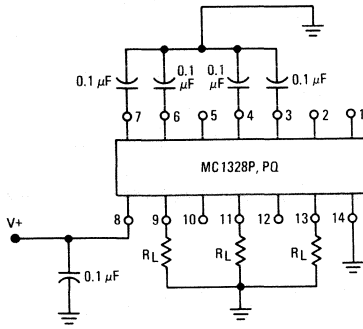
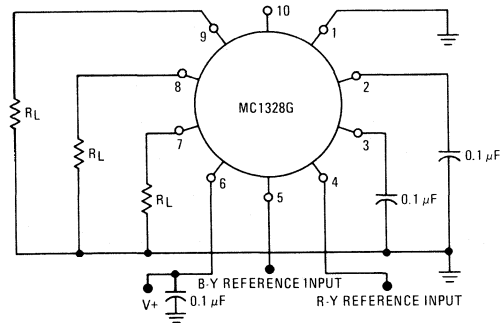
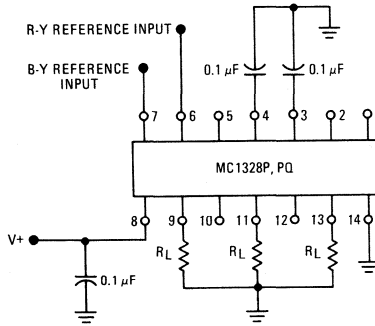


FIGURE 3 – TEST CIRCUIT WITH REFERENCE INPUT SIGNAL
(Quiescent Current, DC Output Voltage, Difference Voltage)



TYPICAL CHARACTERISTICS

FIGURE 4 – DETECTED OUTPUT

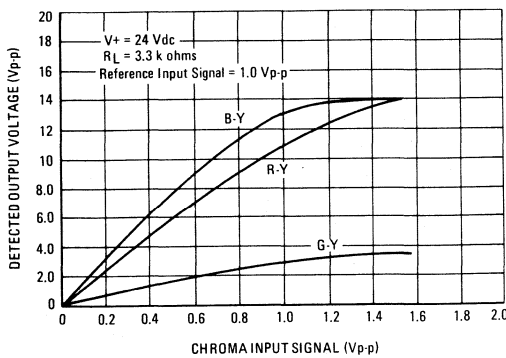
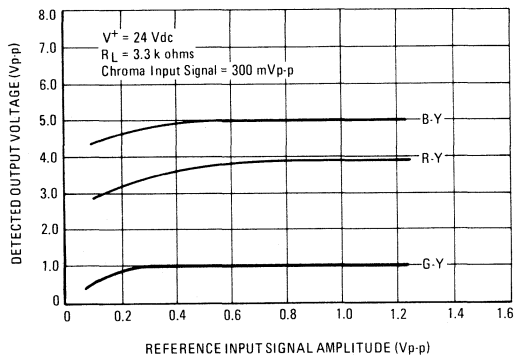


FIGURE 5 – DETECTED OUTPUT



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – DETECTED OUTPUT VOLTAGE

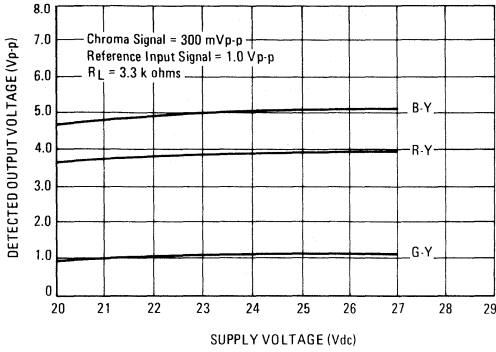


FIGURE 7 – DC OUTPUT VOLTAGE

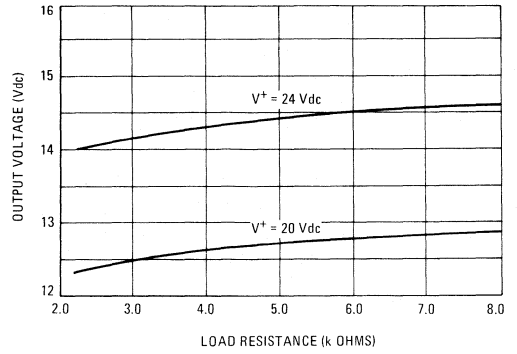


FIGURE 8 – DC OUTPUT VOLTAGE

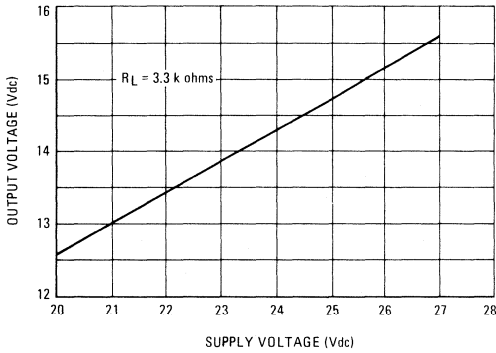


FIGURE 9 – POWER DISSIPATION

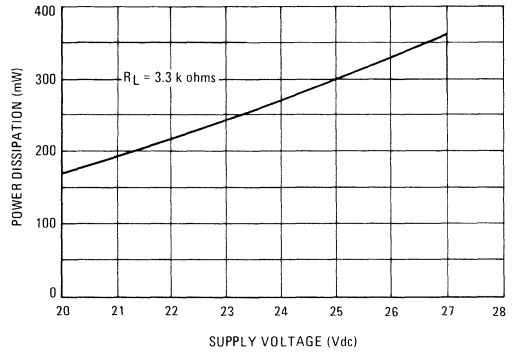


FIGURE 10 – POWER DISSIPATION

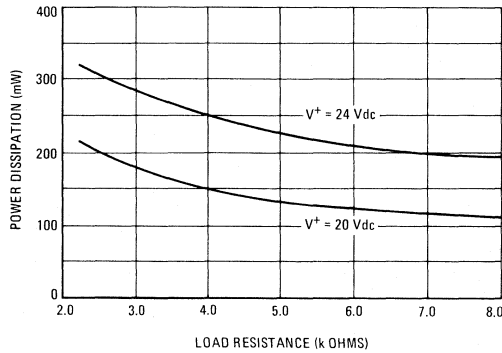
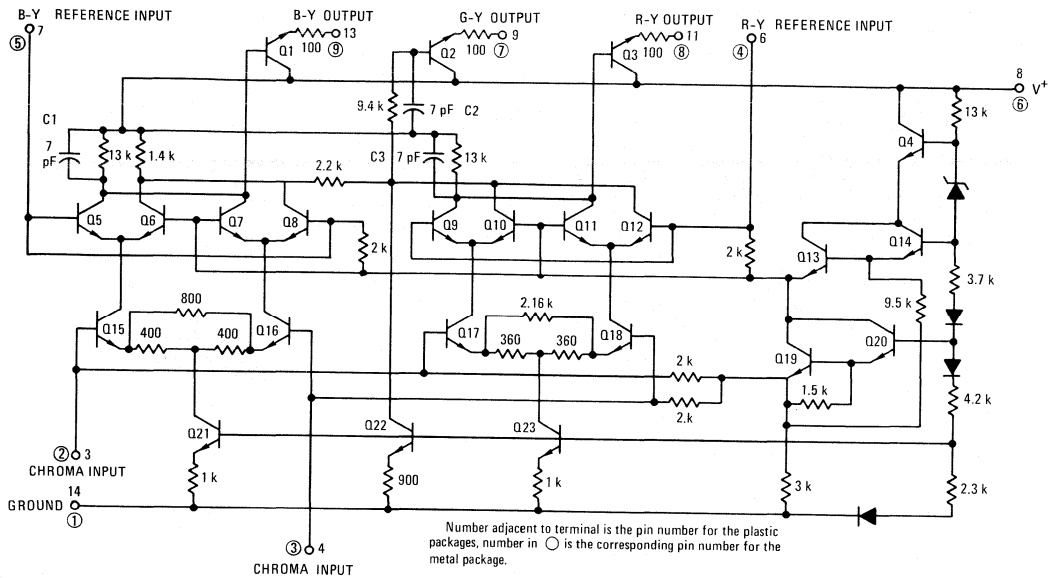


FIGURE 11 – CIRCUIT SCHEMATIC



CIRCUIT OPERATION

A double sideband suppressed carrier chroma signal flows between the bases of the two differential pairs, Q15 and Q16, Q17 and Q18. A reference signal of approximately 1 Vp-p amplitude having the same frequency as the suppressed chroma carrier with an appropriate phase relationship is supplied between the bases of the upper differential pairs Q5 and Q6, Q7 and Q8, Q9 and Q10, Q11 and Q12. The upper pairs are switched between full conduction and zero conduction at the carrier frequency rate. The collectors of the upper pairs are cross-coupled so that "doubly balanced" or "full-wave" synchronous detected chroma signals are obtained. Both positive and negative phases of the detected signal are available at opposite collector pairs.

Capacitors C1, C2 and C3 provide filtering of carrier harmonics from the detected color difference signals. This increases the available swing before clipping for the color difference signal, and reduces the high frequency components which must pass through the emitter followers (Q1, Q2, Q3) into the video output stages. Since high capacitance (>100 pF) is characteristic of the input impedance of a video output stage, the transistor emitter followers must operate at a high quiescent current (>5 mA) in order to pass large high frequency components without distortion. The filtering reduces the quiescent current required in the emitter followers and thus reduces dissipation in the integrated circuit.



MC1330P

VIDEO DETECTOR

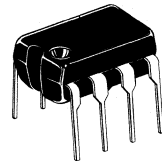
MONOLITHIC LOW-LEVEL VIDEO DETECTOR

... an integrated circuit featuring very linear video characteristics, wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and the AFC buffer.

- Conversion Gain – 34 dB typ
- Video Frequency Response @ 6.0 MHz < 1.0 dB
- Input of 36 mV Produces 3.0 Vp-p Output
- High Video Output – 7.7 Vp-p
- Fully Balanced Detector
- High Rejection of IF Carrier
- Low Radiation of Spurious Frequencies

LOW-LEVEL VIDEO DETECTOR

MONOLITHIC SILICON
INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Value | Unit |
|---|-------------|-------------|
| Power Supply Voltage | +24 | Vdc |
| Supply Current | 26 | mAdc |
| Input Voltage | 1.0 | V(rms) |
| Power Dissipation (Package Limitation) $T_A = +25^\circ\text{C}$ Derate above $T_A = +25^\circ\text{C}$ | 625 5.0 | mW mW/°C |
| Operating Temperature Range (Ambient) | 0 to +75 | °C |
| Storage Temperature Range | -65 to +150 | °C |

Maximum Ratings as defined in MIL-S-19500, Appendix A.

FIGURE 1 – DETECTED COLOR BARS

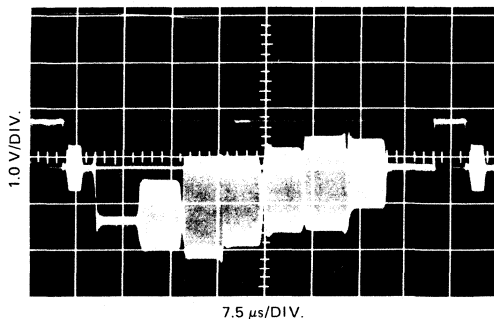
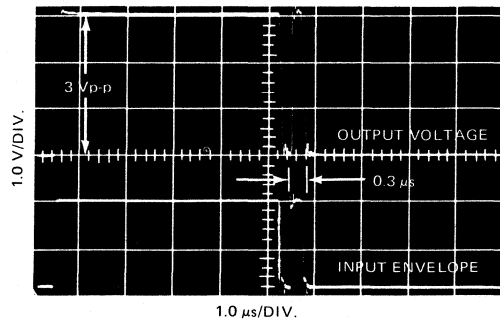


FIGURE 2 – PULSE RESPONSE



See Packaging Information Section for outline dimensions.

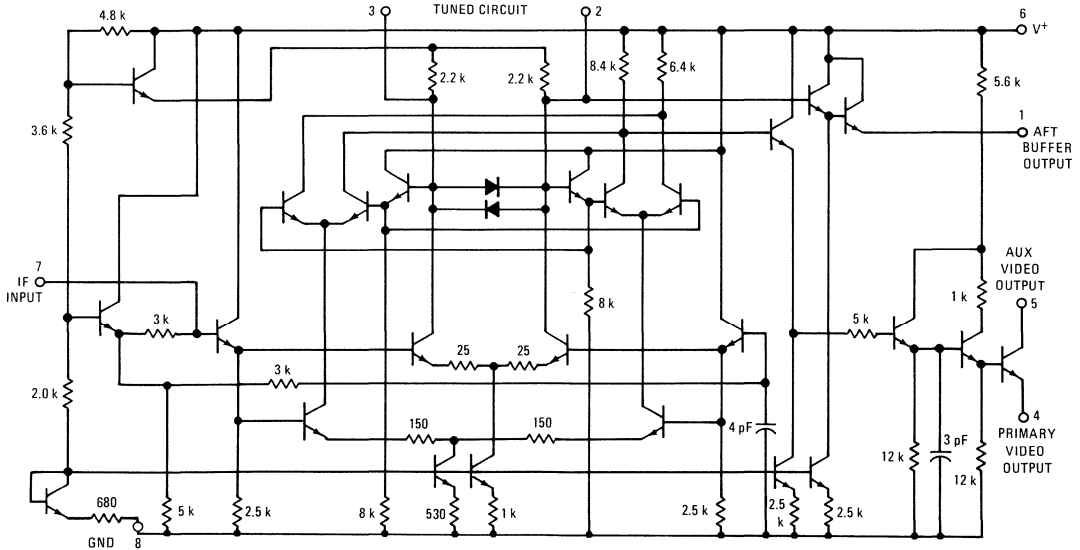
MC1330P (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = 20$ Vdc, $Q = 30$, $f_C = 45$ MHz, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Pin | Min | Typ | Max | Unit |
|---|-----|-----|------------|-----|---------------|
| Supply Voltage Range | 6 | 12 | 20 | 24 | Vdc |
| Supply Current | 5,6 | — | 15 | — | mA |
| Zero Signal dc Output Voltage | 4 | 6.8 | 7.7 | 8.3 | Vdc |
| Maximum Signal dc Output Voltage | 4 | — | 0 | — | Vdc |
| Input Signal Voltage for 3.0 Vp-p Video Output (90% Modulation) | 7 | — | 36 | — | mV(rms) |
| Maximum Output Voltage Swing | 4 | — | 7.7 | — | Vp-p |
| Carrier Rejection at Output | 4 | 42 | 60 | — | dB |
| Carrier Output Voltage (at 3.0 Vp-p output) $f_{out} = f_C$ $f_{out} = 2 f_C$ | | — | 1.0 3.0 | — | mV(rms) |
| 3.0 dB Bandwidth of IF Carrier | 7 | — | 80 | — | MHz |
| 3.0 dB Bandwidth of Video Output | 4 | — | 12.3 | — | MHz |
| Input Resistance | 7 | — | 3.5 | — | kilohms |
| Input Capacitance | | — | 3.0 | — | pF |
| Output Resistance | 4 | — | 180 | — | ohms |
| Internal Resistance } (across tuned circuit) Internal Capacitance } | 2,3 | — | 4.4 1.0 | — | kilohms pF |
| AFT Buffer Output at Carrier Frequency ① | 1 | — | 350 | — | mVp-p |
| AFT Buffer dc Level | 1 | — | 6.5 | — | Vdc |

① Measured with 10 times probe.

FIGURE 3 — CIRCUIT SCHEMATIC



MC1330P (continued)

TYPICAL CHARACTERISTICS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

FIGURE 4 – TEST CIRCUIT

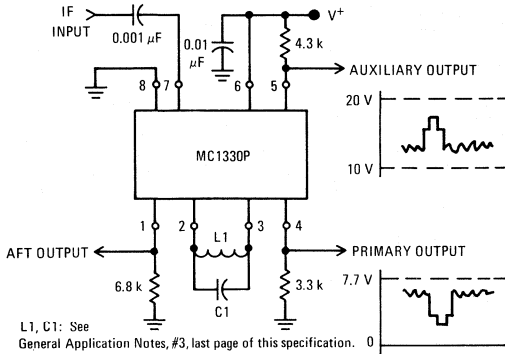


FIGURE 5 – OUTPUT VOLTAGE

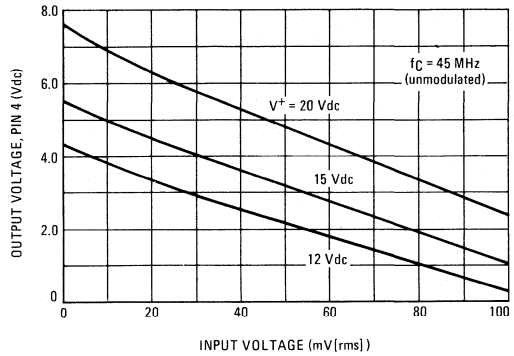


FIGURE 6 – OUTPUT VOLTAGE

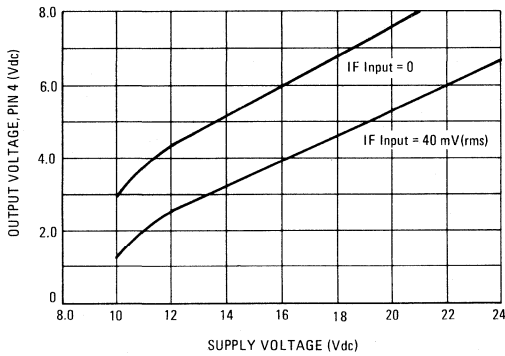


FIGURE 7 – DETECTOR LINEARITY

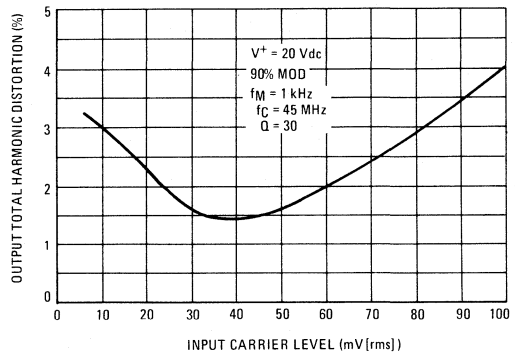


FIGURE 8 – VIDEO FREQUENCY RESPONSE

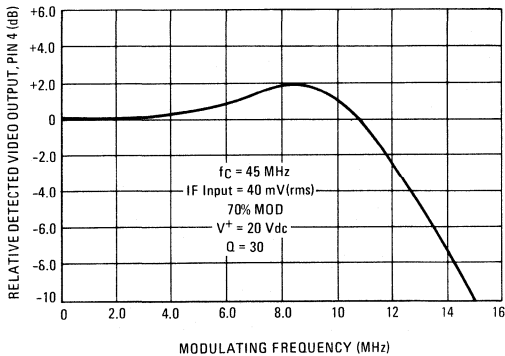
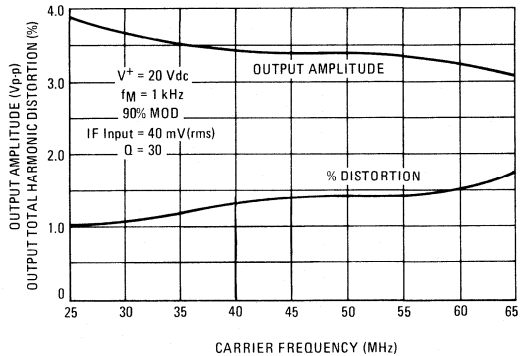
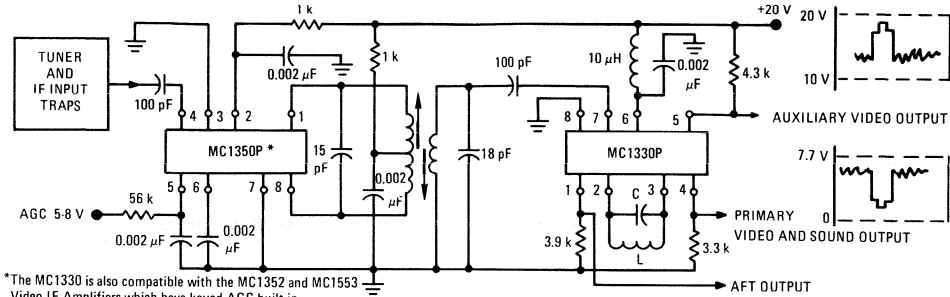


FIGURE 9 – CARRIER FREQUENCY PERFORMANCE



APPLICATIONS INFORMATION

FIGURE 10 – COLOR IF AMPLIFIER TYPICAL APPLICATION

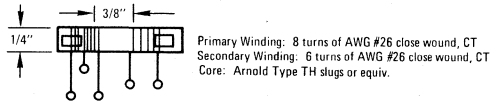


*The MC1330 is also compatible with the MC1352 and MC1553 Video IF Amplifiers which have keyed AGC built-in.

TV-IF Amplifier Information

A very compact high performance IF amplifier constructed as shown in Figure 11 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 84 dB voltage gain and can accommodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1350P input ($Z_{in} \approx 7.0$ kilohms). The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3 volt peak-to-peak output can be varied from 0 to 7.0 V with excellent linearity and freedom from spurious output products.

FIGURE 11 – TRANSFORMER



Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate the low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input), next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3 dB greater than the sweep amplitude.

MC1330P General Information

The MC1330P offers the designer a new approach to an old problem. Now linear detection can be performed at much lower power signal levels than possible with a detector diode. Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some

specific features and information on systems design with this device are given below:

1. The device provides excellent linearity of output versus input, as shown in Figure 6. This graph also shows that video peak-to-peak amplitude (ac) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)
2. The dc output level does change linearly with supply voltage. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.
3. The choice of Q for the tuned circuit of pins 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products but the more critical the tuning accuracy required. Values of Q from 20 to 50 are recommended. (Note the internal resistance.)
4. A video output with positive-going sync is available at pin 5 if required. This signal has a higher output impedance than pin 4 so it must be handled with greater care. If not used, pin 5 may be connected directly to the supply voltage (pin 6).
5. An AFT output (pin 1) provides 350 mV of clipped carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.

MC1339P

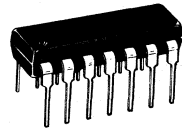
STEREO PREAMPLIFIER

MONOLITHIC DUAL STEREO PREAMPLIFIER

... designed for low noise preamplification of stereo audio signals.

- Low Audio Noise
- High Channel Separation
- Single Power Supply
- High Input Impedance
- Built-In Power Supply Filter
- Emitter Follower Output

DUAL LOW-NOISE STEREO PREAMPLIFIER MONOLITHIC SILICON EPITAXIAL PASSIVATED INTEGRATED CIRCUIT

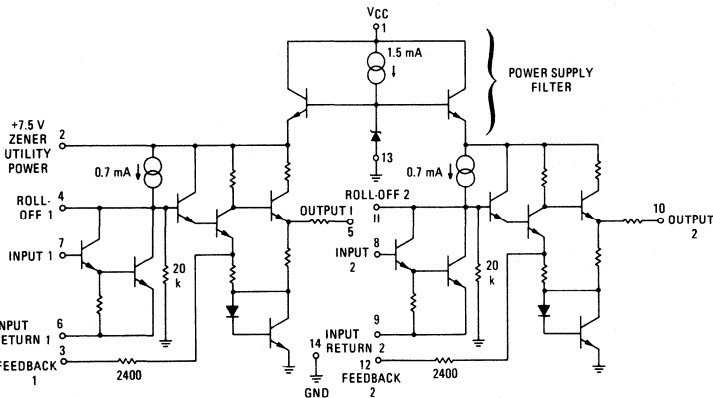


PLASTIC PACKAGE
CASE 646
TO-116

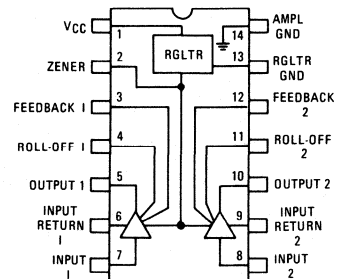
MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Value | Unit |
|---|-------------|----------------------------|
| Power Supply Voltage | +16 | Vdc |
| Power Dissipation (Package Limitation) (Derate above $T_A = +25^\circ\text{C}$) | 625 5.0 | mW mW/ $^\circ\text{C}$ |
| Operating Temperature Range | -40 to +85 | $^\circ\text{C}$ |
| Storage Temperature Range | -65 to +150 | $^\circ\text{C}$ |

CIRCUIT SCHEMATIC



CONNECTION DIAGRAM



MC1339P (continued)

ELECTRICAL CHARACTERISTICS (Each Pre-amplifier) ($V_{CC} = +12$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Min | Typ | Max | Unit |
|--|-----------------|------|-----|--------------------|
| Power Supply Current | — | 17.5 | 22 | mA |
| Voltage Gain | 63 | 66 | 71 | dB |
| Gain Balance | — | 0.3 | 2.0 | dB |
| Channel Separation ($f = 1.0$ kHz) See Figure 1, S1 in position 1. | 45 | 70 | — | dB |
| Input Resistance | 100 | 250 | — | kilohms |
| Signal Output Voltage | | | | V(RMS) |
| | No load | 1.5 | — | |
| | 3.0-kilohm load | 1.0 | — | |
| Output Resistance | — | 100 | — | ohms |
| Power Supply Rejection ($f = 1.0$ kHz) See Figure 2 | — | 33 | — | dB |
| Total Harmonic Distortion without Feedback (0.5 V(RMS) into a 3.0-kilohm load, 1.0 kHz) | — | 1.2 | — | % |
| Input Bias dc Current | — | 0.8 | — | μA |
| Gain to Feedback Terminals (pins 3 and 12) | — | 45 | — | dB |
| Impedance at Feedback Terminals | — | 2400 | — | ohms |
| Equivalent Input Noise Voltage (100 Hz to 10 kHz) See Figure 1, S1 in position 2. | — | 0.7 | 3.0 | $\mu\text{V(RMS)}$ |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

TEST CIRCUITS

FIGURE 1 – CHANNEL SEPARATION AND AUDIO NOISE

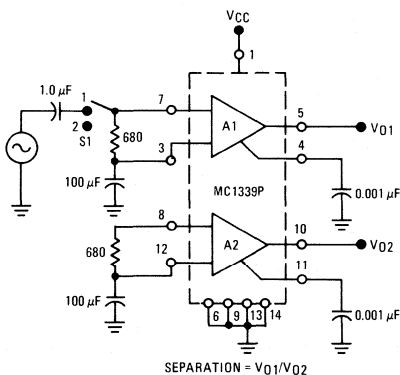
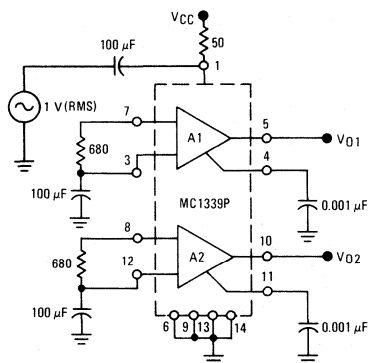


FIGURE 2 – POWER SUPPLY REJECTION



APPLICATIONS INFORMATION

The circuit diagrams shown in this section are examples of applications for the MC1339P. Included are circuits for a broadband preamplifier with tape playback and record amplifiers, and a phono preamplifier.

Broadband Amplifiers

The MC1339P is useful as a broadband amplifier in applications requiring a low-signal level low-noise amplifier. The circuit in Figure 3 fills these requirements with a voltage gain of 40 dB and an input impedance of 10 kilohms.

FIGURE 3 – BROADBAND AMPLIFIER

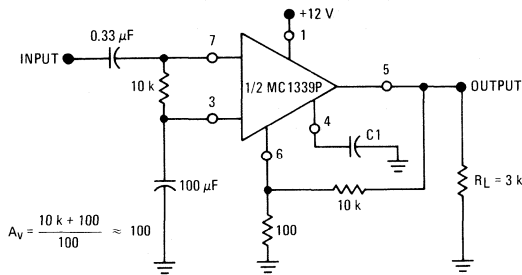
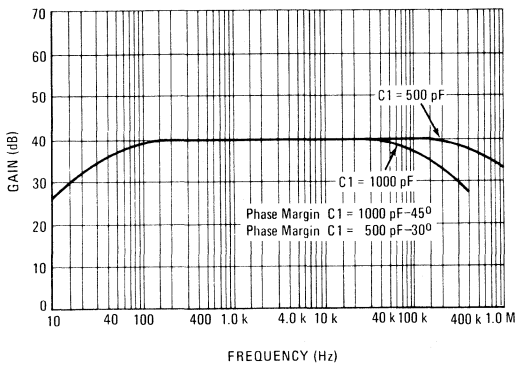


Figure 4 shows the response of the broadband amplifier with two different values of compensation capacitors, C1. Other capacitor values can be used; however, as the phase margin is reduced a greater possibility of oscillation exists.

FIGURE 4 – BROADBAND AMPLIFIER RESPONSE

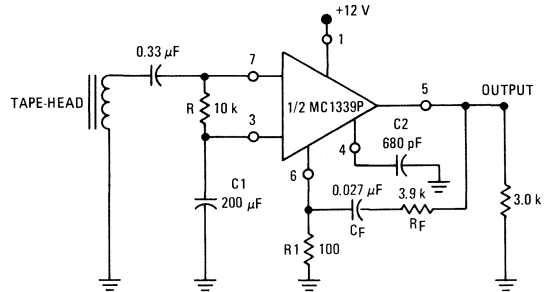


Tape Playback Preamplifier

A low-noise, high-gain preamplifier to properly process the low-level output of the magnetic tape-heads is shown in Figure 5 illustrating a tape-head preamplifier using the MC1339P.

To faithfully reproduce recorded music from magnetic tape, special frequency compensation is required to provide the NAB standard tape playback equalization characteristics, see the response curves shown in Figure 6. The circuit shown in Figure 5 is designed to provide an output of 100 millivolts with an input signal of 2.2 millivolts at a frequency of 1.0 kHz. (Reference gain is 33 dB).

FIGURE 5 – TAPE PLAYBACK PREAMPLIFIER



The lower -3.0 dB corner frequency (f1) is determined by the value for capacitor C1 in accordance with equation 1.

$$C1 = \frac{A3}{2\pi z3f1} \quad (1)$$

where z3 is the impedance at pin 3 (2.4 kilohms) and A3 is the amplifier gain at pin 3 (178).

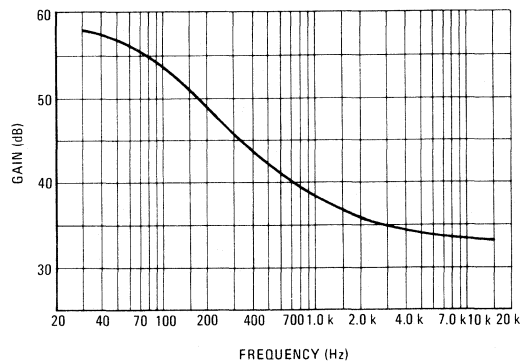
The minimum high-frequency gain (5 dB below reference gain of 33 dB) of the amplifier is determined by the ratio of $\frac{R1 + RF}{R1}$ while the value of capacitor CF provides the bass boost corner frequency in accordance with equation 2.

$$CF = \frac{1}{2\pi RFf2} \quad (2)$$

Based on measurements made on the amplifier (See Figure 5), the value of C2 is chosen for a phase margin greater than thirty degrees.

The nearest 10% tolerance component values were used in the circuit of Figure 5.

FIGURE 6 – FREQUENCY RESPONSE FOR TAPE PLAYBACK PREAMPLIFIER (TAPE SPEED 1 7/8 OR 3 3/4 IN/S)



Tape Record Preamplifier

The frequency response of a tape recording preamplifier must be the mirror image of the NAB playback equalization characteristic, so that the composite record and playback response is flat. Figure 7 shows the record characteristic superimposed on the NAB playback response and Figure 8 illustrates the output characteristic of

APPLICATIONS INFORMATION (continued)

a typical laminated core tape head. Figure 9 shows the necessary amplifier response characteristic to make a composite signal of Figures 8 and 9 that will meet the proper NAB recording characteristic of Figure 7.

FIGURE 7 – NAB TAPE EQUALIZATION CHARACTERISTIC CURVES

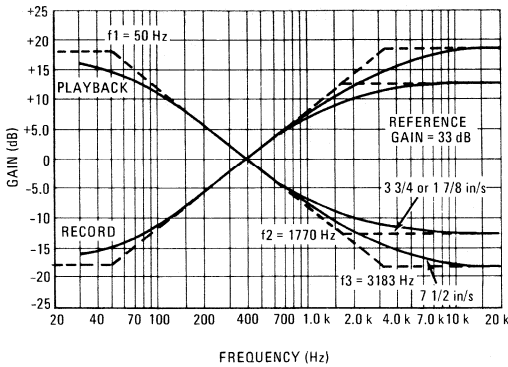


FIGURE 8 – TYPICAL TAPE HEAD OUTPUT CHARACTERISTICS (constant flux)

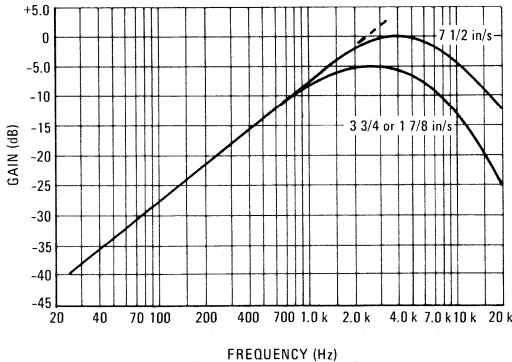


FIGURE 9 – TAPE RECORD AMPLIFIER RESPONSE

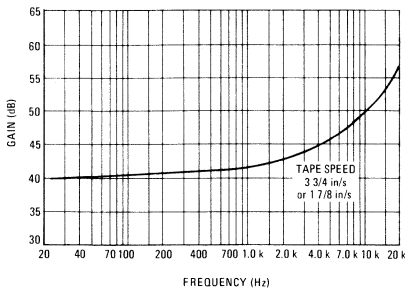
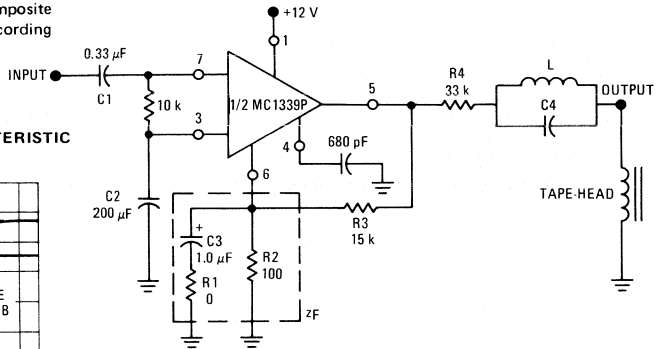


FIGURE 10 – TAPE RECORD PREAMPLIFIER



The circuit shown in Figure 10 will give the preamplifier response as presented in Figure 9.

The gain is established by the equation

$$GAIN = \frac{R3 + z_f}{z_f} \text{ where } z_f = \frac{R2 (R1 + \frac{1}{2\pi f C3})}{R2 + (R1 + \frac{1}{2\pi f C3})} \quad (3)$$

The high corner frequency, f2, is determined by equation 4.

$$C3 = \frac{1}{2\pi f2 R2} \quad (4)$$

At high frequencies the feedback impedance z_f is R1 in parallel with R2 and at low frequencies is R2. Again, capacitor C1 is chosen by equation 1 to give the desired low frequency breakpoint, f1. As an example, consider a recording head requiring 30 μA is used with a microphone with a 10-mV output. The 30-μA current source is simulated by a 1.0 V(RMS) output driving a 33-kilohm resistor, R4, at the reference frequency of 1.0 kHz. The gain requirement is therefore 100 or 40 dB. The low-frequency gain is calculated by letting R2 = 100 ohms and calculating the value of R3 for frequencies below f2.

$$A_v = \frac{R2 + R3}{R2} = 125 \quad R3 = 124 (R2) \approx 12 \text{ k}\Omega. \quad (5)$$

A 15-kilohm resistor is used to achieve the gain necessary since the open-loop gain of the amplifier is not infinite.

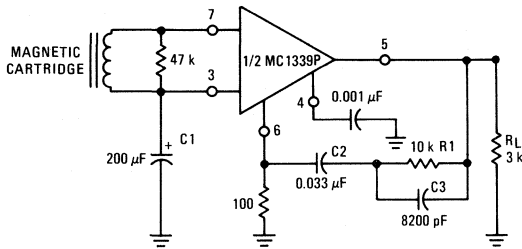
The typical response for a quarter-track (3 3/4 in/s) tape-head is 3.0 dB down at 1770 Hz. Therefore, the high-corner frequency (f2) of the record amplifier should be at the same frequency. Using equation 4 the value of C3 is calculated to be 1.0 μF. Resistor R1 is not needed to roll-off the high-frequency gain at frequencies above 20 kHz since the limited open-loop gain of the MC1339P accomplishes the same thing. The parallel LC circuit at the amplifier output is used to trap the bias oscillator signal and is tuned to that frequency.

Phonographic Preamplifier

Crystal and ceramic phono-cartridges seldom require a preamplifier due to high-output signal levels (100 mV to 1.0 V). However, magnetic cartridges have output levels of from 2.0 to 12 mV and require a preamplifier such as the MC1339P. Special equalization of the preamplifier is necessary to make the response match the RIAA recording characteristic which is used universally. The amplifier shown in Figure 11 does provide the proper response

APPLICATIONS INFORMATION (continued)

FIGURE 11 – PHONOGRAPH PREAMPLIFIER



$$f_2 = \frac{1}{2\pi R_1 C_2} \quad (7)$$

and f_3 is calculated from $f_3 = \frac{1}{2\pi R_1 C_3}$

Printed Circuit Board Layout

Most of the circuits in the applications section can be built on this printed circuit board layout. Printed circuit board design is not particularly critical with the MC1339P. However, usual layout practices such as keeping the input and output lines separated and providing maximum ground plane area should be used. The layout shown is for Figure 5 but it can easily be modified without any problem for the other application circuits given.

FIGURE 12 – FREQUENCY RESPONSE OF PHONO-PREAMPLIFIER (compensated for RIAA Equalization)

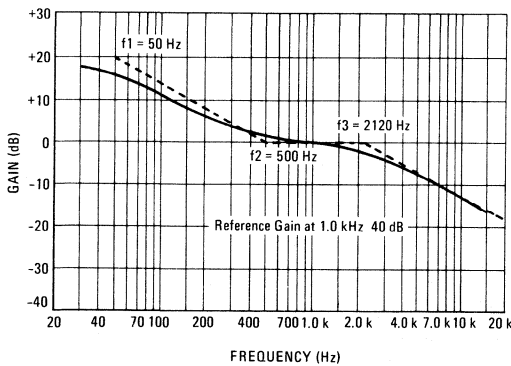
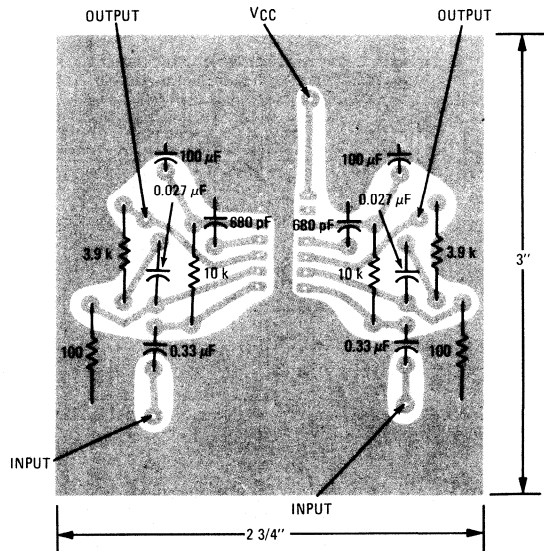


FIGURE 13 – PRINTED CIRCUIT BOARD (copper side shown)



for RIAA equalization. Figure 12 illustrates the RIAA response of the amplifier in Figure 11. The dashed line shows the ideal response with the corner frequencies indicated. The lower corner frequency (f_1) is determined by the input capacitance C_1 and the equation

$$f_1 = \frac{A_f}{2\pi C_1 z_3} \quad (6)$$

where A_f is the feedback gain of 45 dB and z_3 equals the terminal resistance at pin 3. The corner frequency f_2 is determined by

MC1345P

TV SIGNAL PROCESSOR

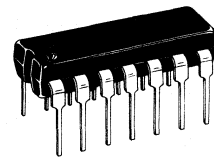
TV SIGNAL PROCESSOR

... a monolithic TV circuit with sync separator, advanced noise inversion, AGC comparator, and versatile RF AGC delay amplifier for use in color or monochrome TV receivers.

- Video Internally Delayed for Total Noise Inversion
- Low Impedance, Noise Cancelled Sync Output
- Refined AGC Gate
- Small IF AGC Output Change During RF AGC Interval
- Positive and Negative Going RF AGC Outputs
- Noise Threshold May Be Externally Adjusted
- Time Constants for Sync Separator Externally Chosen
- Stabilized for $\pm 10\%$ Supply Variations

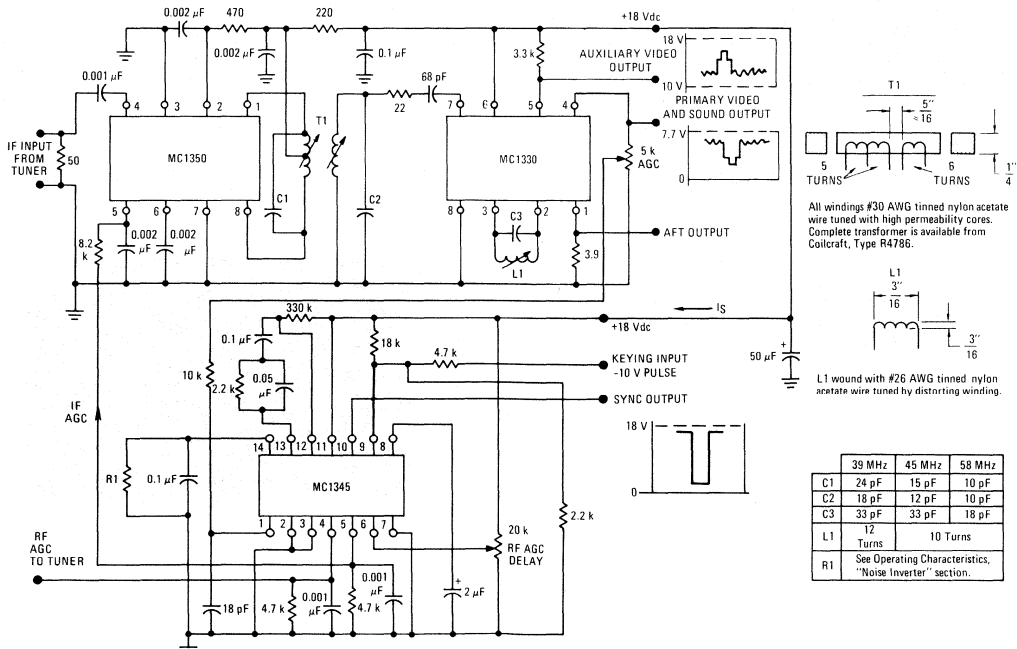
TV SIGNAL PROCESSOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 605
TO-116

FIGURE 1 - TYPICAL MC1345 APPLICATION WITH VIDEO IF AMPLIFIER



See Packaging Information Section for outline dimensions.

MC1345P (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Value | Unit |
|--|-------------|------------------|
| Power Supply Voltage (Pin 11) | +22 | Vdc |
| Video Input Voltage (Pin 1) | +10 | Vdc |
| Negative RF AGC Supply Voltage (Pin 3) | -10 | Vdc |
| Gating Voltage (Pin 9) | 15 | V _{p-p} |
| Sync Separator Drive Voltage (Pin 12) | 7.0 | V _{p-p} |
| Power Dissipation (Package Limitation) | | |
| Plastic Package | 625 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | 5.0 | mW/°C |
| Operating Temperature Range (Ambient) | 0 to +70 | °C |
| Storage Temperature Range | -55 to +150 | °C |

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS ($V^+ = +18\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Min | Typ | Max | Unit |
|---|------|------|------|------------------|
| Sync Tip dc Level of Input Signal | 3.6 | 3.9 | 4.2 | Vdc |
| Temperature Coefficient of Sync Tip (Input) | 0 | -1.3 | -2.5 | mV/°C |
| Sync Output Amplitude | — | 16 | — | V _{p-p} |
| Sync Output Impedance | — | — | 100 | Ohms |
| Sync Tip to Noise Threshold Separation (Input) | 0.45 | 0.7 | 0.95 | Vdc |
| IF AGC Voltage Change During RF Interval | — | 0.10 | 0.5 | Vdc |
| Peak AGC Charge Current | — | 15 | — | mA _{dc} |
| Peak AGC Discharge Current | — | 0.9 | — | mA _{dc} |
| IF AGC Voltage Range (See Figures 2 and 3) | 9.0 | — | — | Vdc |
| Positive RF AGC Voltage Range | — | 10 | — | Vdc |
| Positive RF AGC Minimum Voltage | 0.5 | 1.5 | 2.0 | Vdc |
| Negative RF AGC Voltage Range | — | 10 | — | Vdc |
| Negative RF AGC Maximum Voltage | 9.5 | 10.5 | 11.5 | Vdc |
| Total Supply Current, I_S (Circuit of Figure 1) | — | 26 | — | mA _{dc} |

FIGURE 2 – TEST CIRCUIT FOR AGC AMPLIFIER MEASUREMENTS

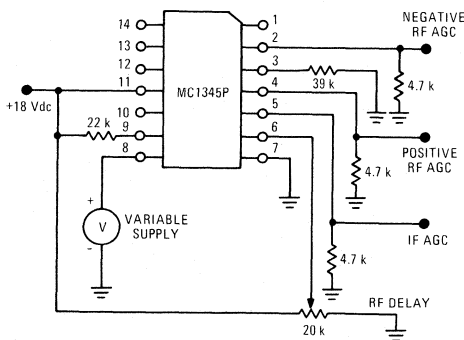
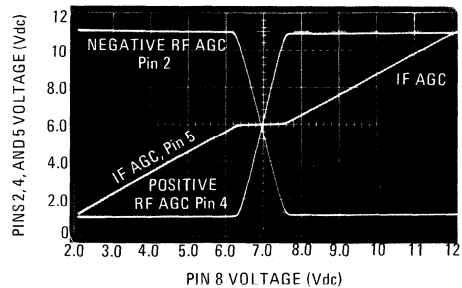
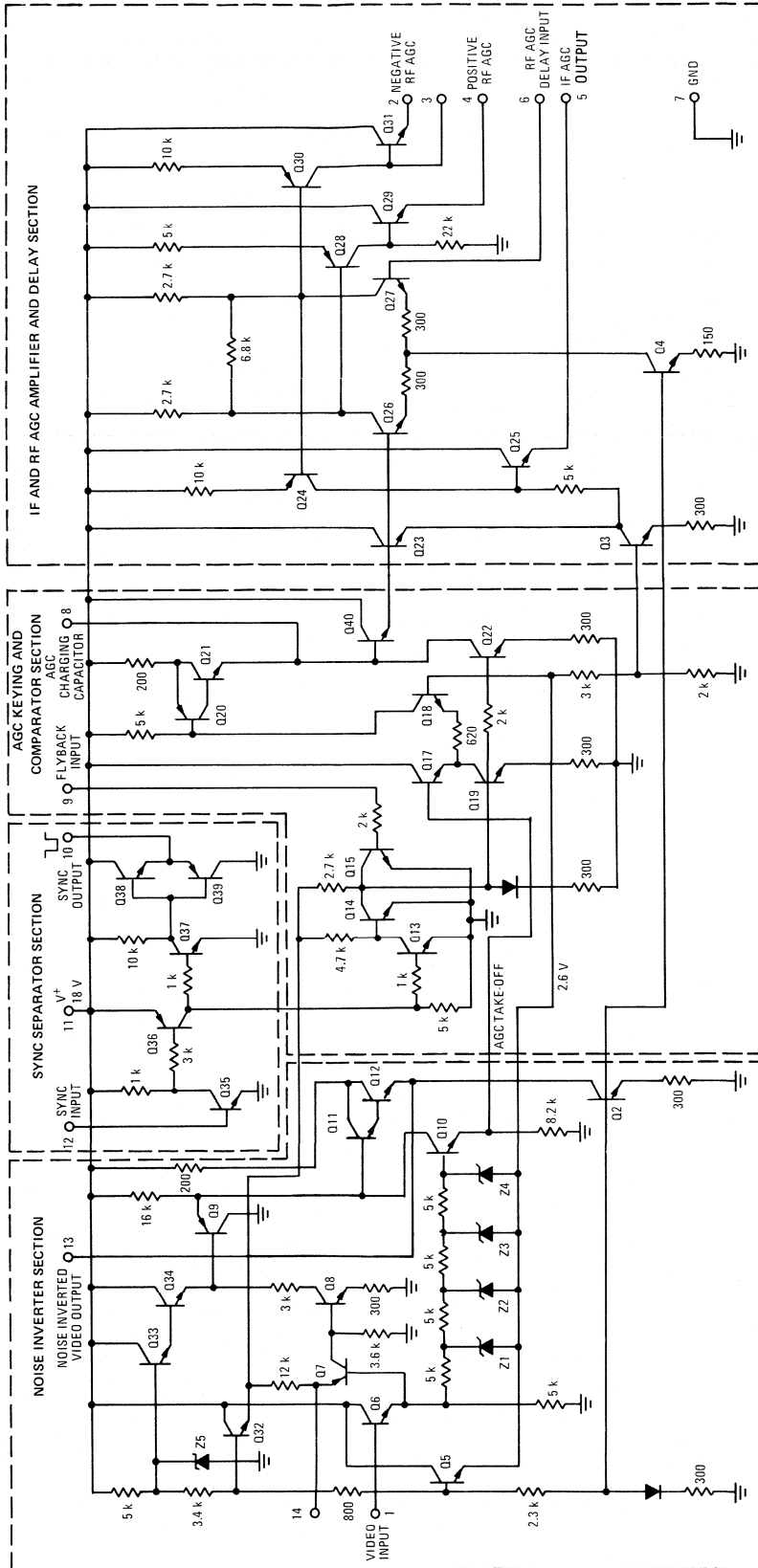


FIGURE 3 – AGC AMPLIFIER RESPONSE



7

FIGURE 4 - CIRCUIT SCHEMATIC



OPERATING CHARACTERISTICS

NOISE INVERTER

A composite video signal of from 1 to 3 volts peak-to-peak amplitude with negative-going sync, superimposed on a positive dc offset voltage, is required at the input, pin 1. The amplitude of the dc offset voltage will determine the allowable magnitude of the video input, since the sync tip will always be clamped at 3.9 V. See Figure 5.

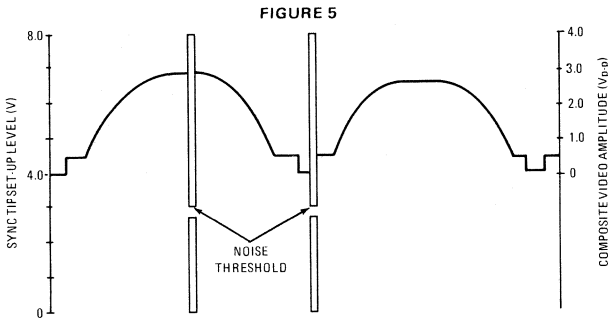
The noise threshold is set by Q7's emitter voltage determined by Q32 and the bias-chain Zener diode. The resulting dc level (or noise threshold) may be lowered by adding an external resistor, R1 (Figure 1), connected from pin 14 to ground. With this arrangement, the lowered threshold would be given by:

$$V = \frac{R1 V_n}{R1 + 12,000 \Omega}$$

where V_n = noise threshold without R1 connected.

The noise threshold can also be raised to the same degree by connecting R1 from pin 14 to the supply voltage level. However, in this case, care should be exercised to insure that the resulting voltage appearing at pin 14 does not exceed the sync threshold (approximately 3.9 V).

Noise inversion is achieved as follows: first the composite input signal is impedance-buffered by the Q6 emitter-follower. Then,



or tropospheric sources is common. To prevent this type of interference from spuriously triggering the inverter, some RC filtering is required between the video detector and the video input at pin 1. For this filter, RC values of 10 kΩ and 18 pF are typical.

SYNC SEPARATOR

The noise-inverted video output at pin 13 is passed through an external RC filter network, to the sync separator input at pin 12, cutting off Q35, Q36, and Q37, except during the positive sync tips. Time constants for the filter are a matter of the designer's preference, and are chosen as for discrete-circuit sync separators.

Operation of the sync separator is as follows. Q35 conducts only during the positive-going sync pulse. Q36 amplifies and inverts the sync pulse, driving Q37 into saturation during the sync pulse interval. The output of Q37 drives the complementary pair, Q38/Q39, which yield a low output impedance negative-going sync pulse of greater than 15 V peak-to-peak amplitude. It should be noted that the first sync pulse occurring after noise inversion ends, will be slightly longer in duration than other sync pulses. Typical resistance and capacitance values for the RC sync input network are given in Figure 6A.

FIGURE 6A – NORMAL SYNC SEPARATION NETWORK

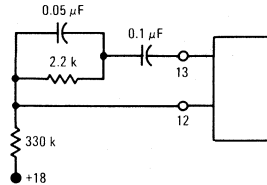
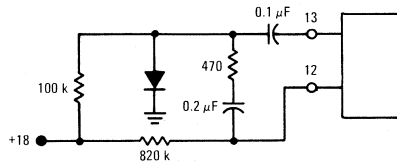


FIGURE 6B – ALTERNATE DIODE SYNC SEPARATION NETWORK



An alternate input network is shown in Figure 6B, it uses a diode to separate the sync pulses. In this case the pulses will be clamped to +0.7 V above ground. As a result, Q35 and the transistors following it serve as over-driven amplifiers.

KEYER AND COMPARATOR

The AGC system is internally connected to the video input at Q10's emitter. The sync signal at Q36 is internally connected to the AGC sync keyer which consists of Q13 and Q14. An externally-derived negative-going flyback pulse (≈ 12 V peak-to-peak) is applied to Q15 for flyback keying the AGC. Since the detected video output level is sampled only when the sync pulse and the flyback pulse are coincident, true keyed AGC action occurs.

An AGC comparator is formed by Q17 and Q18. The base of Q18 is connected to a fixed reference of 2.6 V. The base of Q17 is connected to the emitter of Q10, where the video signal has negative-going sync pulses. The emitters of both devices are supplied

the buffered signal is fed to Q10's base through an RC delay line (Z1 - Z4). Finally the signal appears, inverted and delayed by approximately 300 ns, at the base of Q11.

If an interference pulse occurs, with an amplitude enough above the sync tip level to reach the noise threshold, the pulse will drive the emitter of Q6 below its pre-set level. Q7 will conduct, and charge from the external capacitor connected to pin 14 will pass through Q7, turning on both Q8 and Q9. When Q9 is on, Q11's base is grounded, blanking the output of Q10's collector.

The video signal with the interfering noise cancelled, emerges at pin 13. Polarity is inverted, so the sync pulses are positive-going.

Blanking commences before the interference pulse itself emerges from the delay line, and the blanking action persists for a short time interval after the end of the noise pulse, due to energy stored in Q9's junction.

For very long noise pulses, the rate of discharge of the external capacitor sets the end of the blanking interval. In such a case, blanking could extend over several horizontal line-sweep periods, depending on the capacitor value used. The external capacitor is typically 0.1 µF, and this value allows continuous cancellation for approximately 4 line-sweep intervals.

Under weak signal conditions, high frequency noise from thermal

from a gated current source, Q19. This current source conducts only when Q14 and Q15 are simultaneously switched off. To do this, a positive sync pulse is required on the base of Q13, coincident with a negative flyback pulse on the base of Q15 (pin 9).

If the video signal at the emitter of Q10 increases in amplitude, the sync pulse becomes more negative. Thus, when Q19 is gated on, Q18 conducts and turns on both Q20 and Q21, which charge the external AGC filter capacitor connected at pin 8. A typical value for this capacitor is 2.0 μ F.

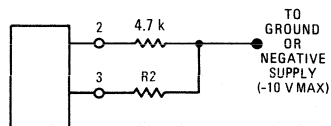
If the video signal decreases, Q18 will not conduct. However, Q22 will conduct and permit a current of 0.9 mA to flow out of the capacitor at pin 8. In effect, this "charge dumping" through Q22 promotes faster AGC action than could be attained with a conventional "charge only" system. Coupling between the charging capacitor and the AGC amplifier is through an emitter follower, Q40.

The MC1345 will operate without flyback pulses if pin 9 is grounded. However, the AGC noise immunity and aircraft flutter rejection will be impaired.

THE AGC AMPLIFIER

AGC for the IF is supplied by the emitter of Q25. The RF AGC is generated in the following way: Given a weak signal condition, Q26 is barely conducting, while Q27 passes the bulk of the current flowing from the current source, Q4. Assume that the base of Q27 is biased "on" by the RF AGC delay control connected to pin 6. The IF AGC will increase if the AGC input voltage from Q40 increases. When this latter voltage increases to a predetermined level (set by the delay control), Q26 turns on. Then, when Q26 turns on, Q27 turns off, which also turns Q24 off. As Q24 turns off, it will cancel any further increases at the base of Q25, which would come from Q23 through the 5.0 k Ω resistor. The result is that the IF AGC level is held constant during the RF AGC excursion.

FIGURE 7 — ALTERNATE RF AGC OUTPUT FOR FET OR TUBE TUNER



As Q26 is now conducting, Q28 and Q29 will also be turned on supplying the forward RF AGC voltage to pin 4. Then, when the RF AGC voltage excursion is complete, Q24 will have reached cutoff and will be unable to oppose the voltage rise at the base of Q25, thus allowing the IF AGC voltage to begin increasing.

The negative RF AGC action is similar, except that Q30 and Q31 are turned off as Q28 and Q29 are turned on. The RF AGC delay, or turn-off of Q27, can be adjusted by the delay control so that it occurs at any selected point in the IF AGC range (see Figure 3).

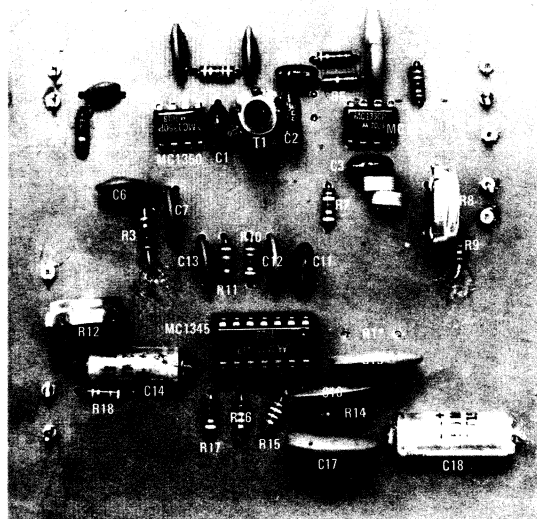
The negative AGC swing may be level-shifted by connecting the pin 2 and pin 3 resistors to a negative supply instead of to ground. The value of the pin 3 resistor, R2, for a given voltage swing, can be determined as:

$$R2 = 4000 \Delta V$$

(See Figure 7 for component connections for negative AGC.)

All external component values given are only suggested values; the final choices will depend on the designer's preferences.

FIGURE 8 — PRINTED CIRCUIT BOARD COMPONENT LAYOUT OF IF AND JUNGLE CIRCUIT OF FIGURE 1

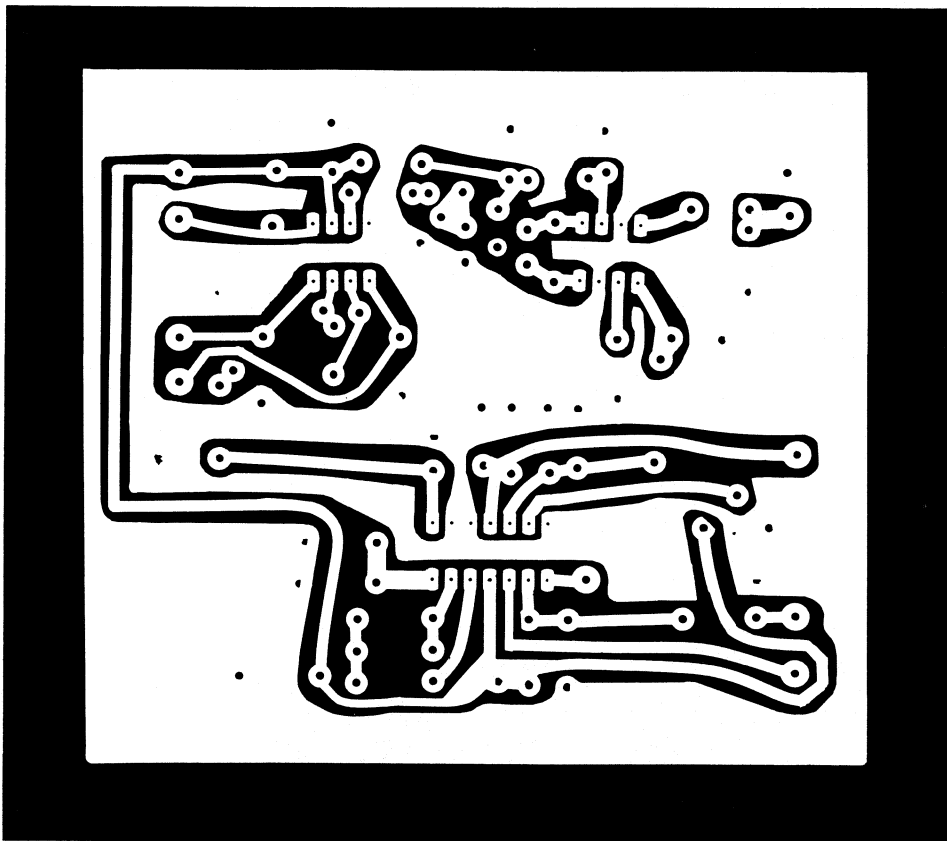


- C1 See chart of Figure 1
- C2 See chart of Figure 1
- C3 See chart of Figure 1
- C4 0.001 μ F
- C5 0.002 μ F
- C6 0.002 μ F
- C7 0.002 μ F
- C8 0.002 μ F
- C9 0.1 μ F
- C10 68 pF
- C11 18 pF
- C12 0.001 μ F
- C13 0.001 μ F
- C14 2 μ F/10 V
- C15 0.1 μ F
- C16 0.05 μ F
- C17 0.1 μ F
- C18 50 μ F/25 V
- L1 See Figure 1
- T1 See Figure 1

- R1 See Operating Characteristics discussion, Noise Inverter section
- R2 470 ohms
- R3 8200 ohms
- R4 220 ohms
- R5 22 ohms
- R6 3300 ohms
- R7 3900 ohms
- R8 5 kilohm potentiometer
- R9 10 kilohms
- R10 4700 ohms
- R11 4700 ohms
- R12 2 kilohm potentiometer
- R13 50 ohms
- R14 2200 ohms
- R15 330 kilohms
- R16 18 kilohms
- R17 2200 ohms
- R18 4700 ohms

*See Noise Inverter Section (part can be omitted).

FIGURE 9 – PRINTED CIRCUIT BOARD
(Scale = 1:1)



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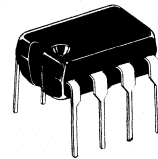
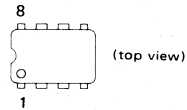
MC1349P

MONOLITHIC IF AMPLIFIER

... an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and television applications over the temperature range 0 to +70°C.

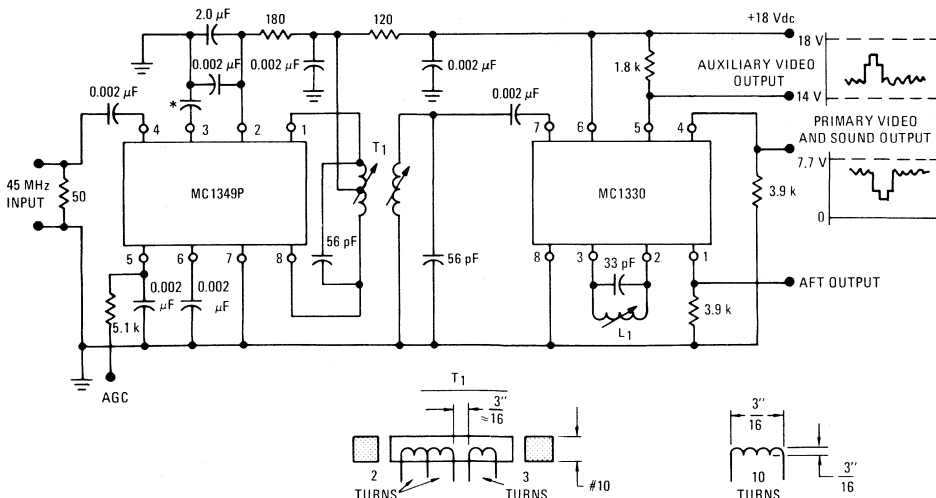
- Power Gain – 60 dB typ at 45 MHz (pin 3 open)
 - 56 dB typ at 58 MHz (pin 3 open)
 - 61 dB typ at 45 MHz (pin 3 bypassed)
 - 59 dB typ at 58 MHz (pin 3 bypassed)
- AGC Range – 80 dB typ, dc to 45 MHz
- High Output Impedance
- Low Reverse Transfer Admittance
- 15-Volt Operation, Single-Polarity Power Supply
- Improved Noise Figure versus AGC

IF AMPLIFIER MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

FIGURE 1 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER
and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT



All windings #22 AWG tinned nylon acetate wire tuned with Coilcraft #61 stugs, size 10-32, or equivalent.

*See Note 1 (page 3), and C4, Parts List (page 4) of this specification.

MC1349P (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

| Rating | Value | Unit |
|---|----------------------------|-------|
| Power Supply Voltage (V _{CC1}) | +18 | Vdc |
| Output Supply Voltage (V _{CC2}) | +18 | Vdc |
| AGC Supply Voltage | ≤ V _{CC1} (pin 2) | Vdc |
| Differential Input Voltage | 5.0 | Vdc |
| Power Dissipation (Package Limitation) | | |
| Plastic Package | 625 | mW |
| Derate above T _A = +25°C | 5.0 | mW/°C |
| Operating Temperature Range | 0 to +70 | °C |
| Storage Temperature Range | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V_{CC1} = +12 Vdc [pin 2], V_{CC2} = +15 Vdc [pins 1 and 8], T_A = +25°C unless otherwise noted.)

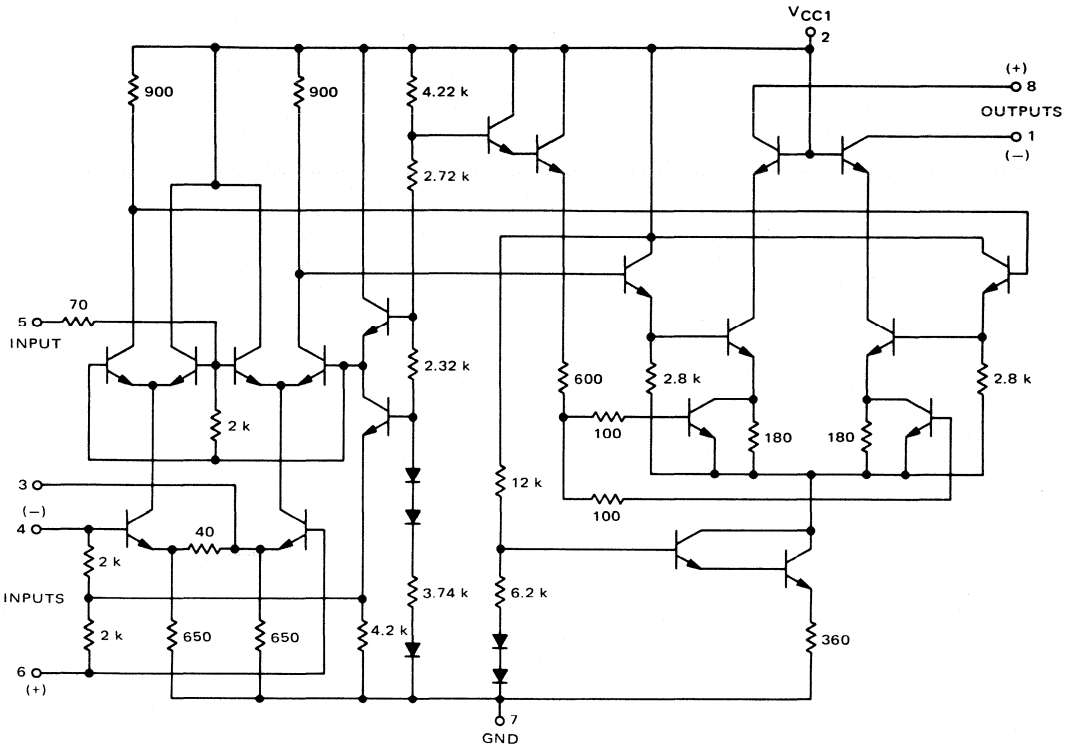
| Characteristic | Min | Typ | Max | Unit |
|--|-----|-----|-----|------|
| AGC Range, 45 MHz (5.0 V to 7.5 V) (Figure 3) | 70 | 80 | — | dB |
| Power Gain (Pin 5 grounded via 5.1 kΩ resistor, input pin 4) | | | | dB |
| f = 45 MHz, BW (3 dB) = 4.5 MHz, Tuned Input, pin 3 open | 52 | 60 | — | |
| Untuned Input, pin 3 bypassed | — | 61 | — | |
| f = 58 MHz, BQ (3 dB) = 4.5 MHz, Tuned Input, pin 3 open | — | 56 | — | |
| Untuned Input, pin 3 bypassed | — | 59 | — | |
| Maximum Differential Output Voltage Swing | — | 6.0 | — | Vp-p |
| Output Stage Current (pins 1 and 8) | — | 9.0 | — | mA |
| Amplifier Current (pin 2) | — | 15 | 20 | mAdc |
| Power Dissipation | — | 315 | 400 | mW |
| Noise Figure | — | 8.5 | — | dB |
| f = 45 MHz, Tuned Input, pin 3 open, Gain Reduction = 15 dB | | | | |

DESIGN PARAMETERS (V_{CC1} = +12 Vdc, [pin 2], V_{CC2} = +15 Vdc, [pins 1 and 8], T_A = +25°C unless otherwise noted.)

| Parameter | Symbol | Frequency | | Unit |
|---|--------|-----------|--------|---------|
| | | 45 MHz | 58 MHz | |
| Single-Ended Input Admittance, input pin 4, AGC min | | | | mmhos |
| Pin 3 open | g11 | 0.74 | 0.95 | |
| Pin 3 open | b11 | 1.9 | 2.4 | |
| Pin 3 bypassed | g11 | 4.1 | 5.4 | |
| Pin 3 bypassed | b11 | 6.5 | 6.9 | |
| Differential Output Admittance, AGC max | | | | μmhos |
| | g22 | 5.5 | 8.3 | |
| | b22 | 270 | 360 | |
| Reverse Transfer Admittance (magnitude) | | 1.5 | 2.0 | μmhos |
| Forward Transfer Admittance | | | | |
| Magnitude, pin 3 open | | 520 | 400 | mmhos |
| Angle (0 dB AGC), pin 3 open | | 100 | 130 | degrees |
| Magnitude, pin 3 bypassed | | 1020 | 800 | mmhos |
| Angle (0 dB AGC), pin 3 bypassed | | 120 | 400 | degrees |
| Single-Ended Input Capacitance, AGC min | | | | pF |
| Pin 3 open | | 6.8 | 6.7 | |
| Pin 3 bypassed | | 2.3 | 20 | |
| Differential Output Capacitance (AGC max) | | 1.0 | 1.0 | pF |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

FIGURE 2 – CIRCUIT SCHEMATIC



GENERAL INFORMATION

The MC1349P is an improved version of the MC1350P. Featuring higher gain, a lower noise figure, and greater AGC range; in addition, an emitter of the input amplifier is available for bypassing. This provides a low input impedance with good gain, useful for untuned input configurations.

Both input and output IF amplifier sections are gain-controlled in the MC1349P, with the input amplifier also serving as an AGC amplifier for the output section. During the initial part of AGC gain reduction, the gain of the input amplifier decreases only a few dB while the output section decreases 15 dB; further AGC acts upon the input section. Although the gain reduction curve was taken with 5.1 kilohms at pin 5, higher series resistance can be used to reduce the voltage and temperature sensitivity of the AGC. Pin 5 currents are shown on the AGC curve, see Figure 10.

In use, it is important to bypass pin 2, both for IF frequencies

and for low frequencies, (as shown in the test circuits). This is due to the dual function of the input amplifier. If replacing MC-1350P take precaution not to ground pin 3, (not used in the MC1350P). Due to the significantly higher gain of the MC1349P, extra care in layout should be exercised.

NOTE 1: The references to bypasses at pin 3 do not give specific values (C4, see Figures 1 and 4). In all cases, measurements were taken with a bypass at a standard value as near as possible to series resonance. The values are dependent on test frequency and circuit layout. Fully bypassing pin 3 reduces the input signal handling capability before distortion from over 100 mV(RMS) to approximately 25 mV(RMS). C4 = 0.002 μF at f = 45 MHz is a typical value for printed circuit applications.

TEST CIRCUITS

FIGURE 3 – TUNED INPUT
(PIN 3 OPEN)

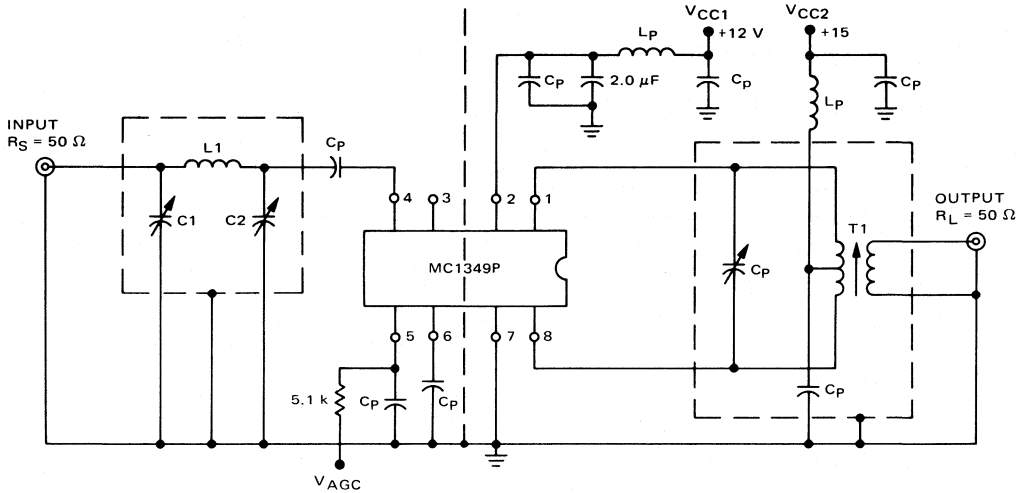
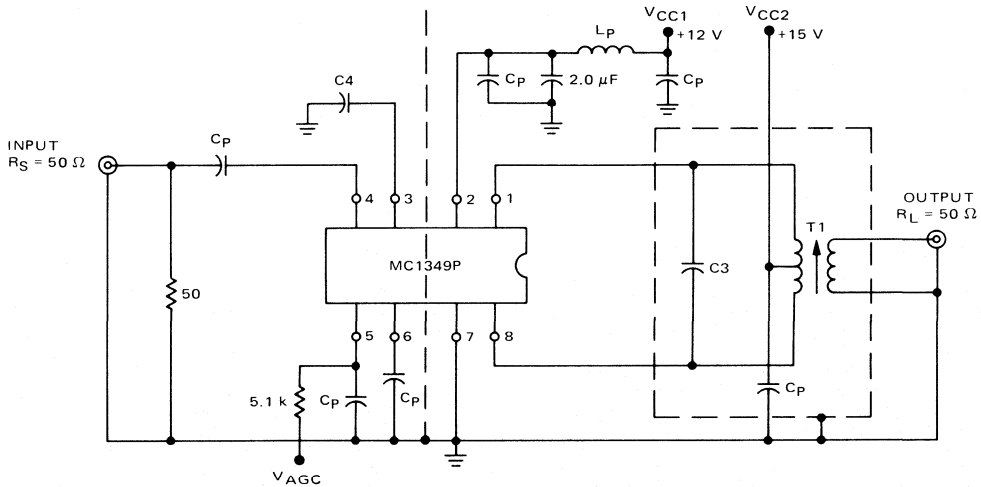


FIGURE 4 – UNTUNED INPUT
(PIN 3 BYPASSED TO GROUND)



PARTS LIST

| COMPONENT | 45 MHz | 58 MHz |
|-----------|-----------|-----------|
| C1 | 8-60 pF | 50-100 pF |
| C2 | 3-35 pF | 3-35 pF |
| C3 | 1-7.0 pF | 1-7.0 pF |
| C4 | 82.470 pF | 82.470 pF |
| Cp | 0.0015 μF | 0.001 μF |
| L1 | 0.84 μH | 0.33 μH |
| Lp | 10 μH | 10 μH |

T1 Primary 14 turns center-tapped
 Secondary 2½ turns (45 MHz tuned input pin #3 open) 1½ turns (all other fixtures) wound over primary
 Wire: #26 AWG tinned nylon acetate wound on 1/4" diameter coil form
 Core: Arnold Type TH, 1/2" long or equivalent.

7

TYPICAL CHARACTERISTICS

FIGURE 5 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 OPEN)

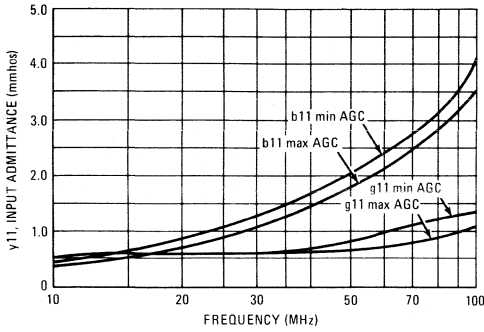


FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 BYPASSED TO GROUND)

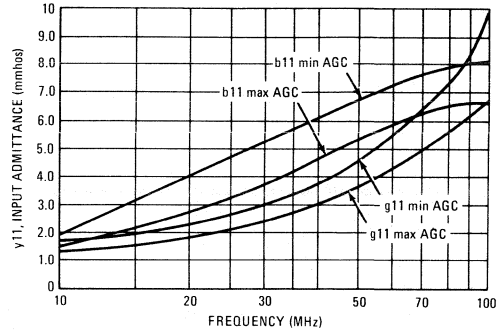


FIGURE 7 – SINGLE-ENDED FORWARD TRANSFER ADMITTANCE

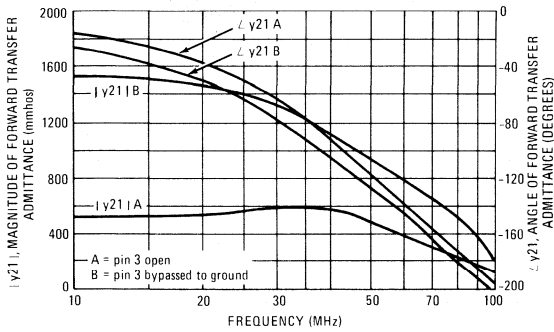


FIGURE 8 – DIFFERENTIAL OUTPUT ADMITTANCE (MAXIMUM AGC)

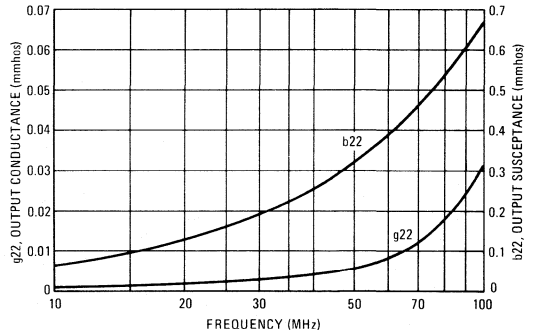


FIGURE 9 – NOISE FIGURE

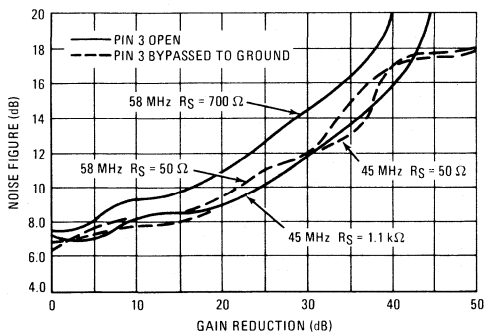
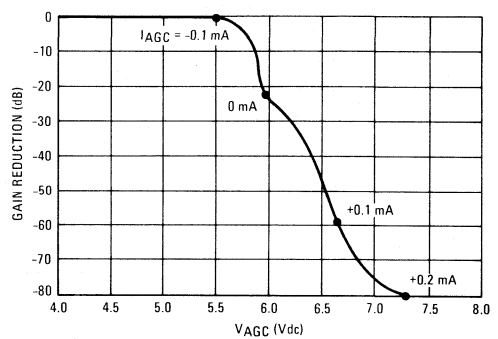


FIGURE 10 – GAIN REDUCTION



MC1350P

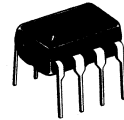
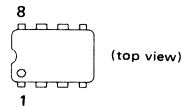
SOUND IF AMPLIFIER

MONOLITHIC IF AMPLIFIER

... an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over the temperature range 0 to +75°C. The MC1352 is similar in design but has a keyed-AGC amplifier as an integral part of the same chip.

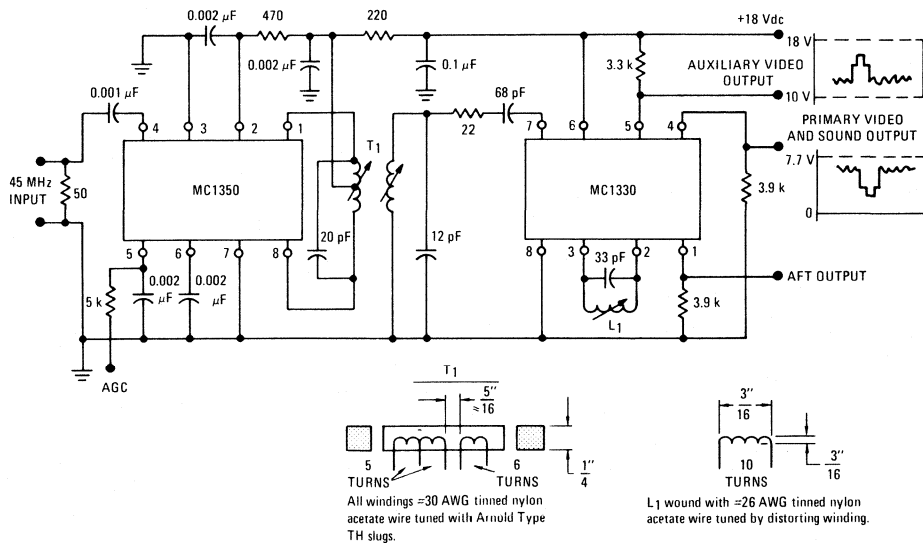
- Power Gain – 50 dB typ at 45 MHz,
– 48 dB typ at 58 MHz
- AGC Range – 60 dB min, dc to 45 MHz
- Nearly Constant Input and Output Admittance Over the Entire AGC Range
- γ_{21} Constant (-3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance – $\ll 1.0 \mu\text{mho}$ typ
- 12-Volt Operation, Single-Polarity Power Supply

IF AMPLIFIER MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

FIGURE 1 – TYPICAL MC1350 VIDEO IF AMPLIFIER
and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT



See Packaging Information Section for outline dimensions.

MC1350P (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|---------------------------------|----------------|-------------|
| Power Supply Voltage | V ⁺ | +18 | Vdc |
| Output Supply Voltage | V ₁ , V ₈ | +18 | Vdc |
| AGC Supply Voltage | V _{AGC} | V ⁺ | Vdc |
| Differential Input Voltage | V _{in} | 5.0 | Vdc |
| Power Dissipation (Package Limitation) Plastic Package Derate above 25°C | P _D | 625 5.0 | mW mW/°C |
| Operating Temperature Range | T _A | 0 to +75 | °C |

ELECTRICAL CHARACTERISTICS (V⁺ = +12 Vdc; T_A = +25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---------------------------------|-------------------|----------------------|------------------|------------------|
| AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1) | | 60 | 68 | — | dB |
| Power Gain (Pin 5 grounded via a 5.1 kΩ resistor) f = 58 MHz, BW = 4.5 MHz } See Figure 5 f = 45 MHz, BW = 4.5 MHz } f = 10.7 MHz, BW = 350 kHz } See Figure 6 f = 455 kHz, BW = 20 kHz } | A _p | — 46 — — | 48 50 58 62 | — — — — | dB |
| Maximum Differential Voltage Swing 0 dB AGC -30 dB AGC | V _o | — — | 20 8.0 | — — | V _{p-p} |
| Output Stage Current (Pins 1 and 8) | I ₁ + I ₈ | — | 5.6 | — | mA |
| Total Supply Current (Pins 1, 2 and 8) | I _S | — | 14 | 17 | mAdc |
| Power Dissipation | P _D | — | 168 | 204 | mW |

DESIGN PARAMETERS, Typical Values (V⁺ = +12 Vdc, T_A = +25°C unless otherwise noted)

| Parameter | Symbol | Frequency | | | | Unit |
|--|---|---------------------|-------------------|-------------------|--------------------|-----------------------------|
| | | 455 kHz | 10.7 MHz | 45 MHz | 58 MHz | |
| Single-Ended Input Admittance | g ₁₁ b ₁₁ | 0.31 0.022 | 0.36 0.50 | 0.39 2.30 | 0.5 2.75 | mmhos |
| Input Admittance Variations with AGC (0 to 60 dB) | Δg ₁₁ Δb ₁₁ | — — | — — | 60 0 | — — | μmhos |
| Differential Output Admittance | g ₂₂ b ₂₂ | 4.0 3.0 | 4.4 110 | 30 390 | 60 510 | μmhos |
| Output Admittance Variations with AGC (0 to 60 dB) | Δg ₂₂ Δb ₂₂ | — — | — — | 4.0 90 | — — | μmhos |
| Reverse Transfer Admittance (Magnitude) | y ₁₂ | << 1.0 | << 1.0 | << 1.0 | << 1.0 | μmho |
| Forward Transfer Admittance Magnitude Angle (0 dB AGC) Angle (-30 dB AGC) | y ₂₁ < y ₂₁ < y ₂₁ | 160 -5.0 -3.0 | 160 -20 -18 | 200 -80 -69 | 180 -105 -90 | mmhos degrees degrees |
| Single-Ended Input Capacitance | C _{in} | 7.2 | 7.2 | 7.4 | 7.6 | pF |
| Differential Output Capacitance | C _o | 1.2 | 1.2 | 1.3 | 1.6 | pF |

FIGURE 2 – TYPICAL GAIN REDUCTION
(Figures 5 and 6)

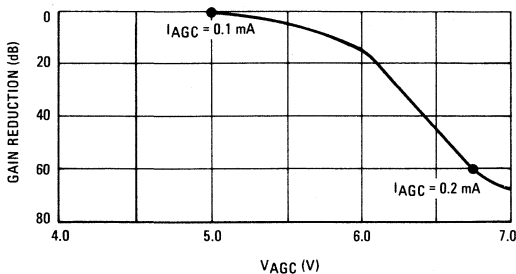
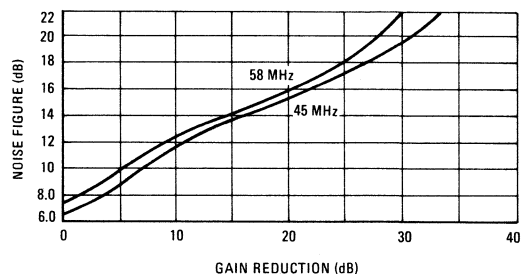


FIGURE 3 – NOISE FIGURE
(Figure 5)



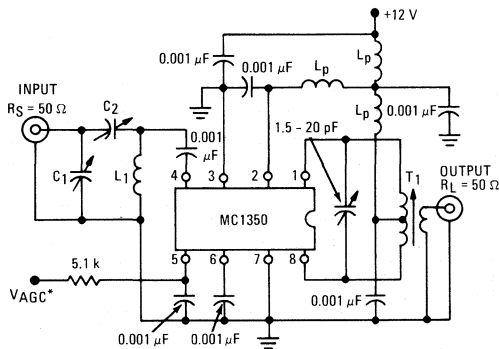
MC1350P (continued)

GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V^{++}) is used, because the base voltage on the output amplifier varies with AGC bias.

FIGURE 5 – POWER GAIN, AGC and NOISE FIGURE TEST CIRCUIT (45 MHz and 58 MHz)



*Connect to ground for maximum power gain test.
All power-supply chokes (L_p), are self-resonate at input frequency. $L_p \geq 20 \text{ k}\Omega$
See Figure 10 for frequency response curve.

- L_1 @ 45 MHz = 7 1/4 Turns on a 1/4" coil form.
- @ 58 MHz = 6 Turns on a 1/4" coil form
- T_1 Primary Winding = 18 Turns on a 1/4" coil form, center-tapped
- Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
- = 1 Turn @ 58 MHz
- Slug = Arnold TH Material 1/2" Long

| | 45 MHz | | 58 MHz | |
|-------|-------------------------|------------------------------|-------------------------|------------------------------|
| L_1 | 0.4 μH | $Q \geq 100$ | 0.3 μH | $Q \geq 100$ |
| T_1 | 1.3 - 3.4 μH | $Q \geq 100 @ 2 \mu\text{H}$ | 1.2 - 3.8 μH | $Q \geq 100 @ 2 \mu\text{H}$ |
| C_1 | 50 - 160 pF | | 8 - 60 pF | |
| C_2 | 8 - 60 pF | | 3 - 35 pF | |

FIGURE 4 – CIRCUIT SCHEMATIC

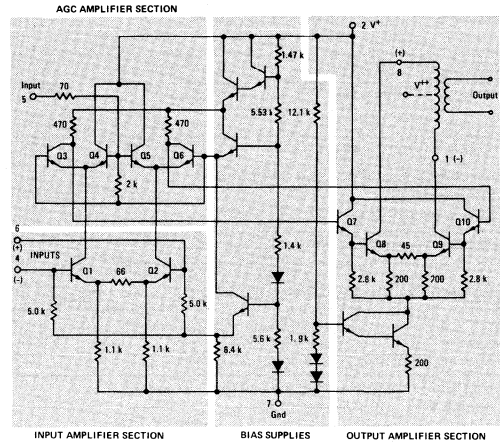
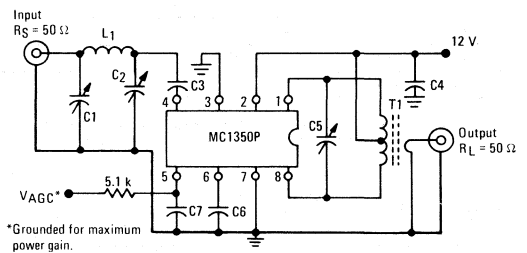


FIGURE 6 – POWER GAIN and AGC TEST CIRCUIT (455 kHz and 10.7 MHz)



- Note 1. Primary: 120 μH (center-tapped)
 $Q_U = 140$ at 455 kHz
Primary: Secondary turns ratio ≈ 13
- Note 2. Primary: 6.0 μH
Primary winding = 24 turns #36 AWG (close-wound on 1/4" dia. form)
Core = Arnold Type TH or equiv.
Secondary winding = 1-1/2 turns #36 AWG, 1/4" dia. (wound over center-tap)

| Component | Frequency | |
|-----------|---------------------|---------------------|
| | 455 kHz | 10.7 MHz |
| C_1 | — | 80 - 450 pF |
| C_2 | — | 5.0 - 80 pF |
| C_3 | 0.05 μF | 0.001 μF |
| C_4 | 0.05 μF | 0.05 μF |
| C_5 | 0.001 μF | 36 pF |
| C_6 | 0.05 μF | 0.05 μF |
| C_7 | 0.05 μF | 0.05 μF |
| L_1 | — | 4.6 μH |
| T_1 | Note 1 | Note 2 |

TYPICAL CHARACTERISTICS

($V^+ = 12\text{ V}$, $T_A = +25^\circ\text{C}$)

FIGURE 7 – SINGLE-ENDED INPUT ADMITTANCE

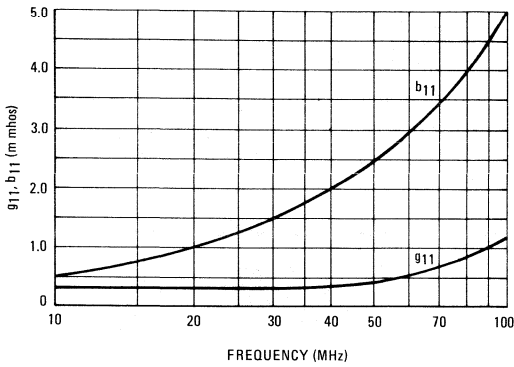


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

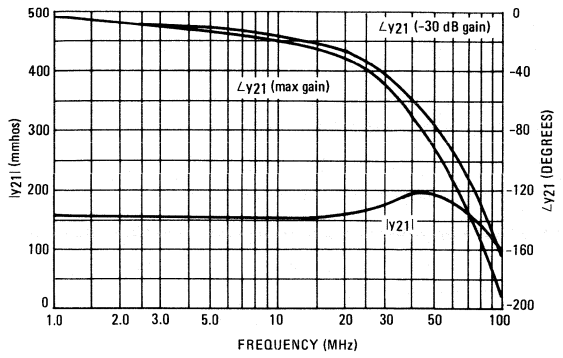


FIGURE 9 – DIFFERENTIAL OUTPUT ADMITTANCE

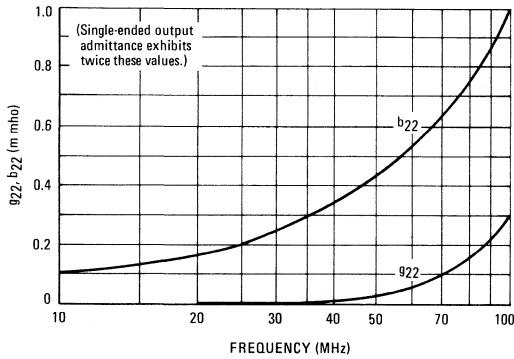


FIGURE 10 – TEST CIRCUIT RESPONSE CURVE (45 and 58 MHz)

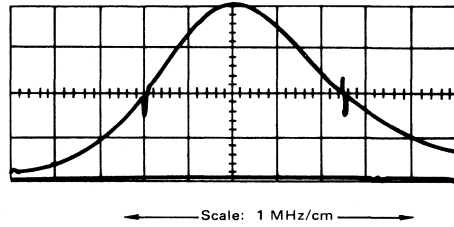
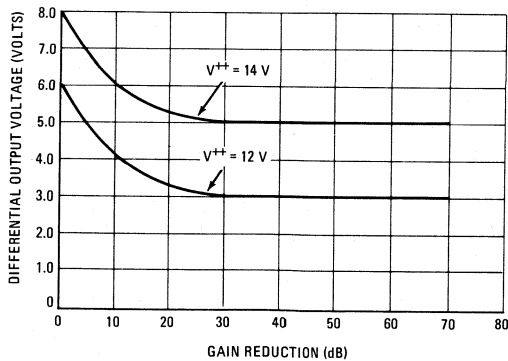


FIGURE 11 – DIFFERENTIAL OUTPUT VOLTAGE



For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control", by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

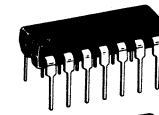
MC1351

WIDE-BAND FM-AMPLIFIER; LIMITER, DETECTOR, AND AUDIO AMPLIFIER INTEGRATED CIRCUIT

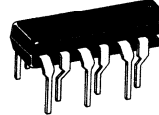
... designed for IF limiting, detection, audio preamplifier and driver for the sound portion of a TV receiver.

- Excellent Limiting with 80 μ V (rms) Input Signal typ
- Large Output-Voltage Swing – to 3.5 V (rms) typ
- High IF Voltage Gain – 65 dB typ
- Zener Power-Supply Regulation Built-In
- Short-Circuit Protection
- A Coincidence Discriminator that Requires Only One RLC Phase Shift Network
- Preamplifier to Drive a Single External-Transistor Class-A Audio-Output Stage

TV SOUND CIRCUIT MONOLITHIC SILICON EPITAXIAL PASSIVATED

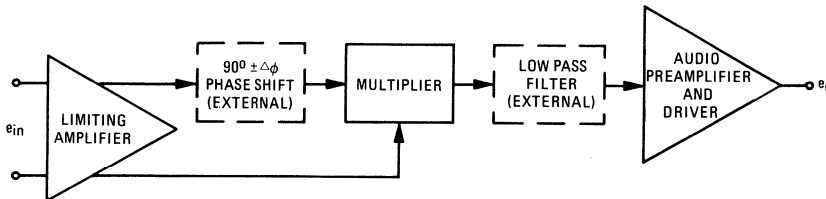


P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116

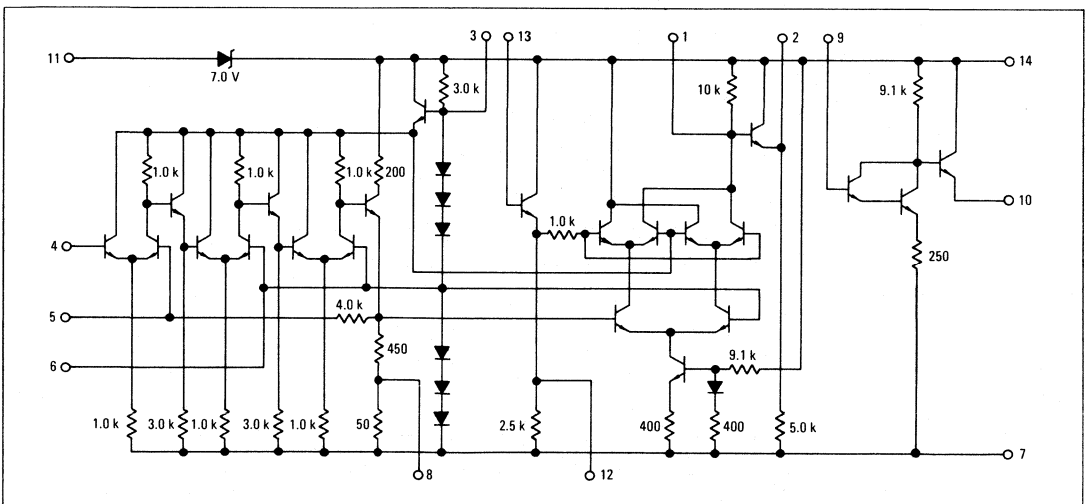


PQ SUFFIX
PLASTIC PACKAGE
CASE 647

BLOCK DIAGRAM



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MC1351 (continued)

MAXIMUM RATINGS ($T_A = +25^\circ$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|--------------------------------------|-------------|-------------|
| Power Supply Voltage | V+ | +16 | Vdc |
| Input Voltage | V _{in} | 0.7 | V(rms) |
| Power Dissipation (Package Limitation) Plastic Packages Derate above +25°C | P _D 1/θ J _A | 625 5.0 | mW mW/°C |
| Operating Temperature Range | T _A | 0 to +75 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

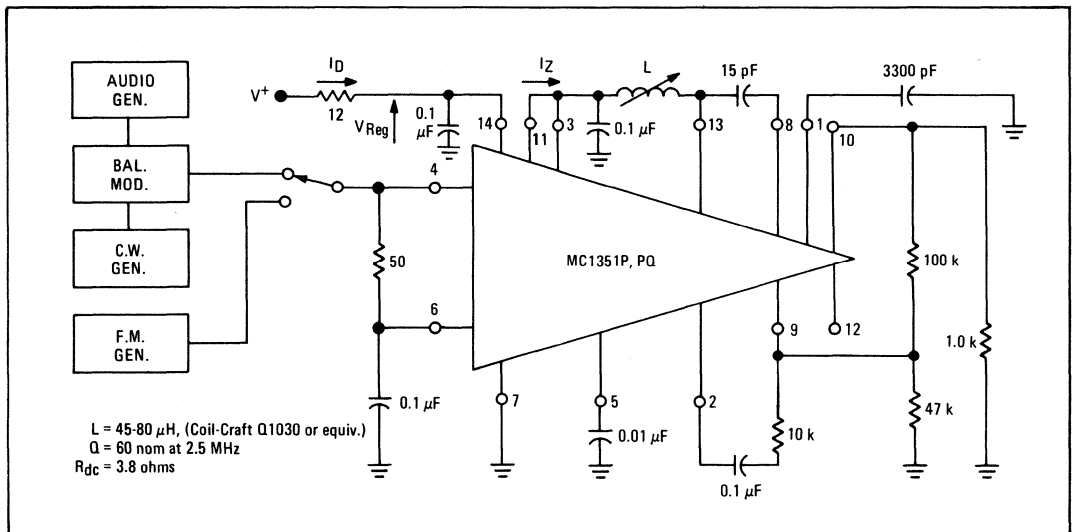
Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS ($V^+ = 12$ Vdc, $T_A = +25^\circ$ C, $f = 4.5$ MHz, Deviation = ± 25 kHz unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---------------------|------|--------------|-----|---------|
| Input Voltage (-3.0 dB Limiting) | V _L | - | 80 | 160 | μV(rms) |
| AM Rejection (V _{in} = 20 mV(rms), AM = 30%) (See Note 1) | AMR | - | 45 | - | dB |
| AMR = 20 log $\frac{V_{OFM}}{V_{OAM}}$ { f = 4.5 MHz, Deviation = ± 25 kHz, Q _L = 24 f = 5.5 MHz, Deviation = ± 50 kHz, Q _L = 30 | | - | 45 | - | |
| Total Harmonic Distortion (Q _L = 24) (See Note 1) (7.5 kHz Deviation) | THD | - | 1.0 | - | % |
| Maximum Undistorted Audio Output Voltage (Pin 10) (See Note 1) (Audio Gain Adjusted Externally) (Q = 24) | V _{o(max)} | - | 3.5 | - | V(rms) |
| Recovered Audio (Pin 2) (See Note 1) (f = 4.5 MHz, Deviation = ± 25 kHz, Q _L = 24) (f = 5.5 MHz, Deviation = ± 50 kHz, Q _L = 30) | V _A | 0.35 | 0.50 0.80 | - | V(rms) |
| Audio Preampifier Open Loop Gain | A _{vp} | - | 25 | - | dB |
| IF Voltage Gain | A _{VIF} | - | 65 | - | dB |
| Parallel Input Resistance | R _{in} | - | 9.0 | - | kΩ |
| Parallel Input Capacitance | C _{in} | - | 6.0 | - | pF |
| Nominal Zener Voltage (I _Z = 5.0 mAdc) | V _{Reg} | - | 11.6 | - | Vdc |
| Power Supply Current (I _Z = 5.0 mAdc) | I _D | - | 31 | - | mAdc |
| Power Dissipation (I _Z = 5.0 mAdc) | P _D | - | 300 | 375 | mW |

Note 1: Q_L is loaded circuit Q.

FIGURE 1 - TEST CIRCUIT ($V^+ = +12$ Vdc, $T_A = +25^\circ$ C)



TYPICAL CHARACTERISTICS

FIGURE 2 – DETECTED AUDIO OUTPUT versus INPUT LEVEL @ $f = 4.5$ MHz, ± 25 kHz DEVIATION

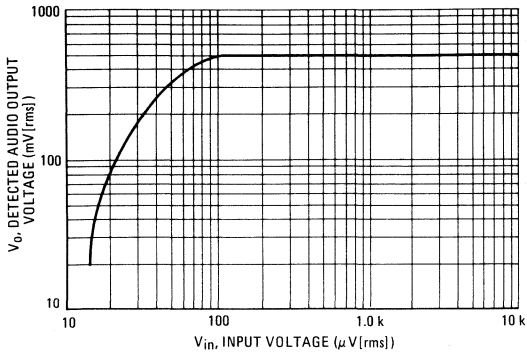


FIGURE 3 – DETECTED AUDIO OUTPUT versus INPUT LEVEL @ $f = 5.5$ MHz, ± 50 kHz DEVIATION

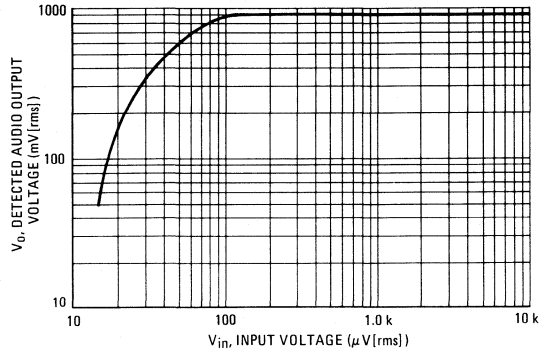


FIGURE 4 – DETECTOR "S" CURVE @ $f = 4.5$ MHz, BW = 200 kHz, Q = 24

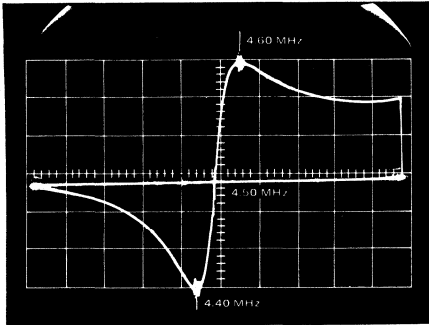


FIGURE 5 – DETECTOR "S" CURVE @ $f = 5.5$ MHz, BW = 220 kHz, Q = 30

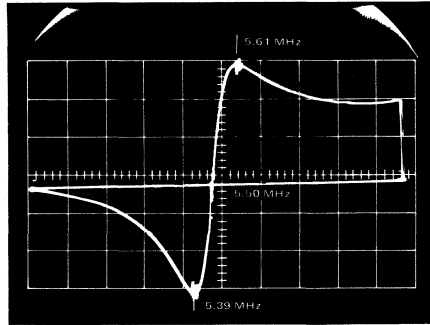


FIGURE 6 – IF VOLTAGE GAIN versus FREQUENCY

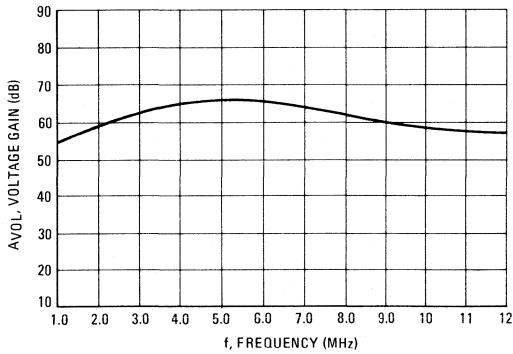
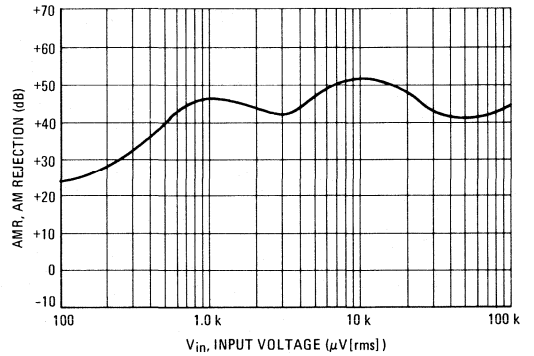
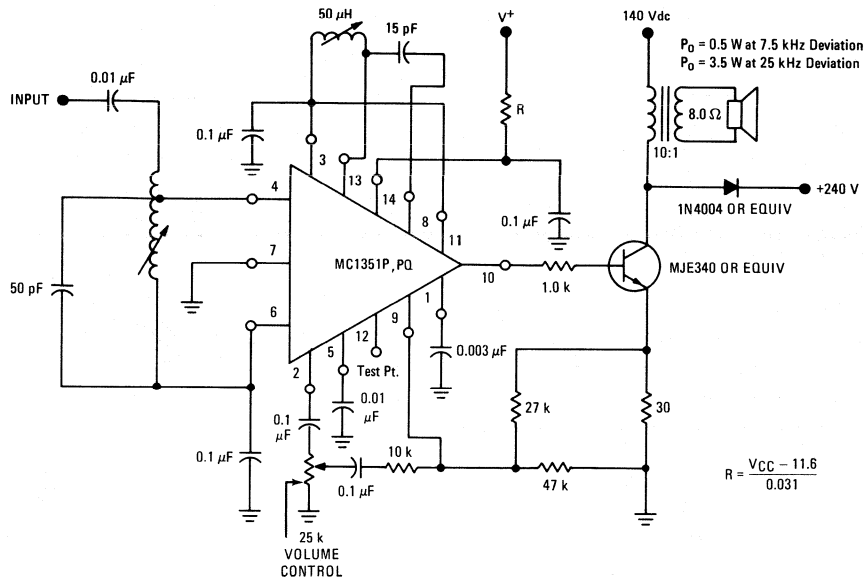


FIGURE 7 – AM REJECTION



7

FIGURE 8 - 4.5 MHz TYPICAL APPLICATION



TV VIDEO IF AMPLIFIER

MC1352 MC1353

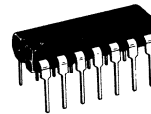
TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

... a monolithic IF amplifier with a complete gated wide-range AGC system for use as the 1st and 2nd IF stages and AGC keyer and amplifier in color or monochrome TV receivers.

- Power Gain at 45 MHz, 52 dB typ
- Extremely Low Reverse-Transfer Admittance – $\ll 1.0 \mu\text{mho typ}$
- Nearly Constant Input and Output Admittance Over AGC Range
- Single-Polarity Power-Supply Operation
- High-Gain Gated AGC System for Either Positive or Negative-Going Video Signals
- Control Signal Available for Delayed AGC of Tuner
- Two Complementary Devices – MC1352 and MC1353 – Offer Opposite Tuner AGC Polarity

TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

MONOLITHIC SILICON INTEGRATED CIRCUIT

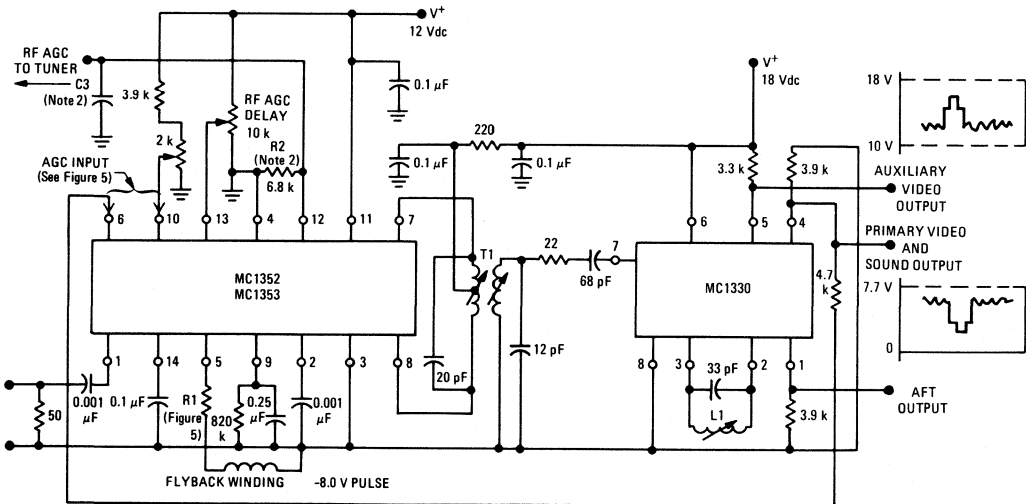


P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116

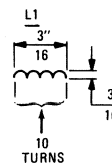
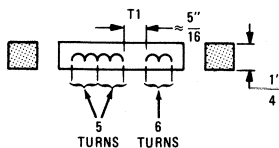
PQ SUFFIX
PLASTIC PACKAGE
CASE 647



FIGURE 1 – TYPICAL VIDEO IF AMPLIFIER APPLICATION



All windings #30 AWG tinned nylon acetate wire tuned with Arnold Type TH slugs.



Wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

MC1352, MC1353(continued)

MAXIMUM RATINGS (Voltages referenced to pin 4, ground; $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Value | Unit |
|--|-------------|----------------------|
| Power Supply (Pin 11) | +18 | Vdc |
| Output Supply (Pins 7 and 8) | +18 | Vdc |
| Signal Input Voltage (Pin 1 or 2, other pin ac grounded) | 10 | V _{p-p} |
| AGC Input Voltage (Pin 6 or 10, other pin ac grounded) | +6.0 | Vdc |
| Gating Voltage, Pin 5 | +10, -20 | Vdc |
| Power Dissipation | 625 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | 5.0 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | 0 to +70 | $^\circ\text{C}$ |
| Storage Temperature Range | -55 to +150 | $^\circ\text{C}$ |

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS ($V_+ = +12$ Vdc, Voltages referenced to pin 4, ground; $T_A = +25^\circ\text{C}$ unless otherwise noted)

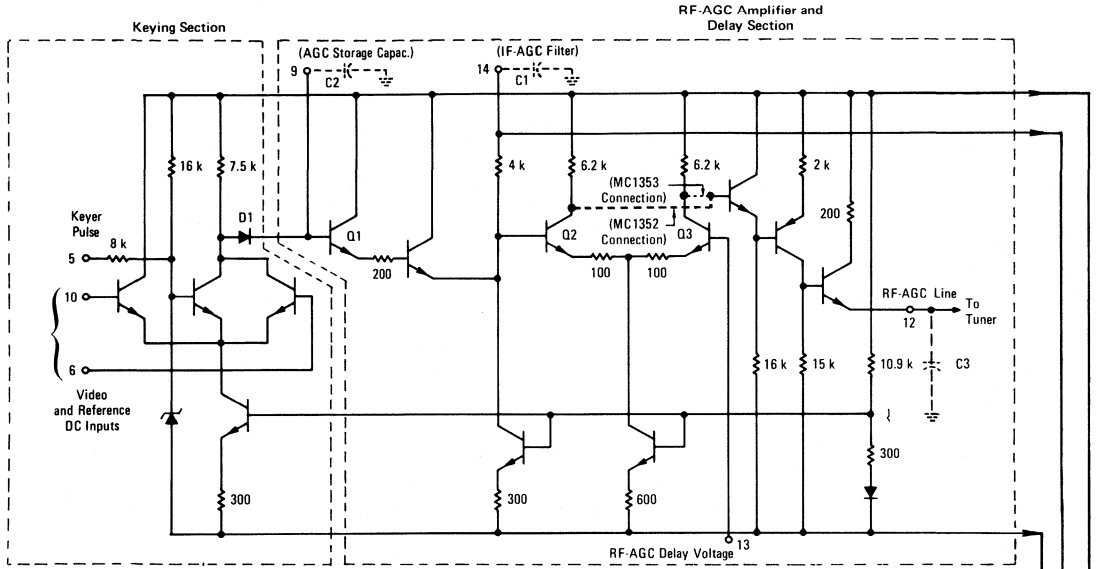
| Characteristic | Min | Typ | Max | Unit |
|---|-----|------|-----|------------------|
| AGC Range | — | 75 | — | dB |
| Power Gain | | | | dB |
| $f = 35$ MHz or 45 MHz | — | 52 | — | |
| $f = 58$ MHz | — | 50 | — | |
| Maximum Differential Output Voltage Swing | | | | V _{p-p} |
| 0 dB AGC | — | 16.8 | — | |
| -30 dB AGC | — | 8.4 | — | |
| Voltage Range for RF-AGC at Pin 12 | | | | Vdc |
| Maximum | — | 7.0 | — | |
| Minimum | — | 0.2 | — | |
| IF Gain Change Over RF-AGC Range | — | 10 | — | dB |
| Output Stage Current ($I_7 + I_8$) | — | 5.7 | — | mAdc |
| Total Supply Current ($I_7 + I_8 + I_{11}$) | — | 27 | 31 | mAdc |
| Total Power Dissipation | — | 325 | 370 | mW |

DESIGN PARAMETERS, TYPICAL VALUES ($V_+ = 12$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

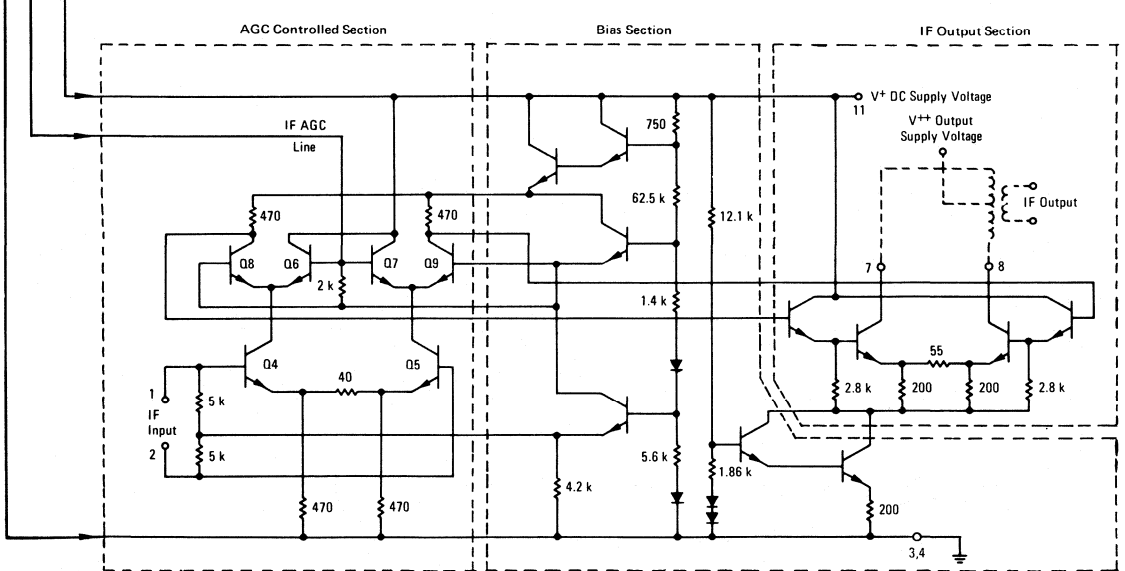
| Parameters | Symbol | f = 35 MHz | f = 45 MHz | f = 58 MHz | Unit |
|--|------------------------------------|--------------|--------------|-------------|------------------|
| Single-Ended Input Admittance | g_{11} b_{11} | 0.55 2.25 | 0.70 2.80 | 1.1 3.75 | mmhos |
| Input Admittance Variations with AGC (0 to 60 dB) | Δg_{11} Δb_{11} | 50 0 | 60 0 | — | μmhos |
| Differential Output Admittance | g_{22} b_{22} | 20 430 | 40 570 | 75 780 | μmhos |
| Output Admittance Variations with AGC (0 to 60 dB) | Δg_{22} Δb_{22} | 3.0 80 | 4.0 100 | — | μmhos |
| Reverse Transfer Admittance | $ v_{12} $ | $\ll 1.0$ | $\ll 1.0$ | $\ll 1.0$ | μmho |
| Forward Transfer Admittance | | | | | |
| Magnitude | $ v_{12} $ | 260 | 240 | 210 | mmhos |
| Angle (0 dB AGC) | $\angle v_{21}$ | -73 | -100 | -135 | degrees |
| Angle (-30 dB AGC) | $\angle v_{21}$ | -52 | -72 | -96 | |
| Single-Ended Input Capacitance | | 9.5 | 10 | 10.5 | pF |
| Differential Output Capacitance | | 2.0 | 2.0 | 2.5 | pF |

FIGURE 2 - CIRCUIT SCHEMATIC

KEYER AND AGC AMPLIFIER

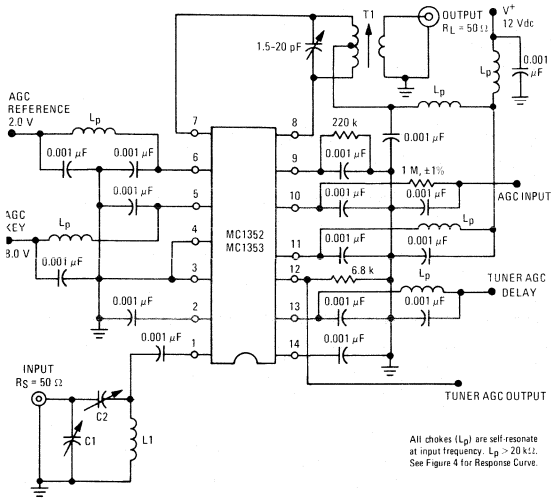


IF AMPLIFIER



MC1352, MC1353 (continued)

FIGURE 3 – POWER GAIN, AGC AND NOISE TEST CIRCUIT



| | 35 and 45 MHz | 58 MHz |
|----|---------------------------|---------------------------|
| L1 | 0.4 μH Q ≥ 100 | 0.3 μH Q ≥ 100 |
| T1 | 1.3-3.4 μH Q ≥ 100 @ 2 μH | 1.2-3.8 μH Q ≥ 100 @ 2 μH |
| C1 | 48-100 pF | 40-80 pF |
| C2 | 8-80 pF | 12-45 pF |

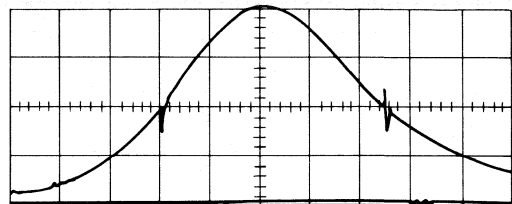
L1 and T1 – #28 AWG Tinned Nylon Acetate Wire.

L1 @ 35 or 45 MHz = 7-1/4 Turns on a 1/4" coil form
 @ 58 MHz = 6 Turns on a 1/4" coil form
 T1 Primary Winding = 18 Turns on a 1/4" coil form
 Secondary Winding = 2 Turns Wound Evenly over Primary
 Winding for 35 or 45 MHz and 1
 Turn for 58 MHz
 Slug = Arnold TH Material 1/2" long

All chokes (Lp) are self-resonate at input frequency. Lp > 20 kΩ. See Figure 4 for Response Curve.

V_C , is maintained across the external capacitor, C2, for a particular video level and dc reference setting. The voltage V_C , is the result of the charge delivered through D1 and the charge drained by Q1. The charge delivered occurs during the time of the gating pulse, and its magnitude is determined by the amplitude of the video signal relative to the dc reference level. The voltage V_C is delivered via the IF-AGC amplifier and applied to the variable gain stage of the IF signal amplifier and is also applied to the RF-AGC amplifier, where it is compared to the fixed RF-AGC delay voltage reference by the differential amplifier, Q2 and Q3. The following stages amplify the output signal of either Q2 for MC1352, or Q3 for MC1353 and shift the dc levels causing the RF-AGC voltage to vary (positive-going for MC1352 or negative-going for MC1353).

FIGURE 4 – TEST CIRCUIT RESPONSE CURVE (45 and 58 MHz)



Scale: 1 MHz/cm

GENERAL OPERATING INFORMATION

Each device, MC1352 and MC1353, consists of an AGC section and an IF signal amplifier (Figure 2) subdivided into different functions as indicated by the illustration.

A gating pulse, a reference level, and a composite video signal are required for proper operation of the AGC section. Either positive or negative-going video may be used; necessary connections and signal levels are shown in Figure 1. The essential difference is that the video is fed into Pin 10 and the AGC reference level is applied to Pin 6 for a video signal with positive-going sync while the input connections are reversed for negative-going sync.

The action of the gating section is such that the proper voltage,

NOTES:

- The 12-V supply must have a low ac impedance to prevent low-frequency instability in the RF-AGC loop. This can be achieved by a 12-V zener diode and a large decoupling capacitor (5 μF).
- Choices of C1, C2 and C3 depend somewhat on the set designers' preference concerning AGC stability versus AGC recovery speed. Typical values are C1 = 0.1 μF, C2 = 0.25 μF, C3 = 10 μF.
- To set a fixed IF-AGC operating point (e.g., for receiver alignment) connect a 22 kΩ resistor from pin 9 to pin 11 to give minimum gain, then bias pin 14 to give the correct operating point using a 200 kΩ variable resistor to ground.
- Although the unit will normally be operating with a very high power gain, the pin configuration has been carefully chosen so that shielding between input and output terminals will not normally be necessary even when a standard socket is used.

The input amplifiers (Q4 and Q5) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac). Terminals 1 and 2 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q6 and Q7 causing those transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q8 and Q9. The output amplifiers are fed from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant.

FIGURE 5 – TYPICAL AGC APPLICATION CHART

| Video Polarity | Pin 6 Voltage | Pin 10 Voltage | Pin 5 R1 (Ω) |
|----------------------|-------------------------------|-------------------------------|--------------|
| Negative-Going Sync. | 5.5 2.0 0 | Adj. 1.0-4.0 Vdc Nom 2.0 V | 0 |
| Positive-Going Sync. | Adj. 1.0-8.0 Vdc Nom 4.5 V | 4.5 0 | 3.9 k |

MC1352, MC1353 (continued)

TYPICAL CHARACTERISTICS

($V^+ = +12$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE

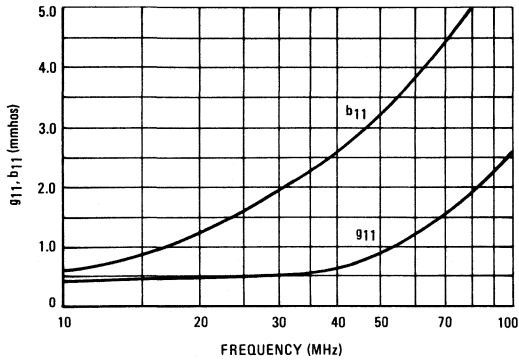


FIGURE 7 – DIFFERENTIAL OUTPUT ADMITTANCE

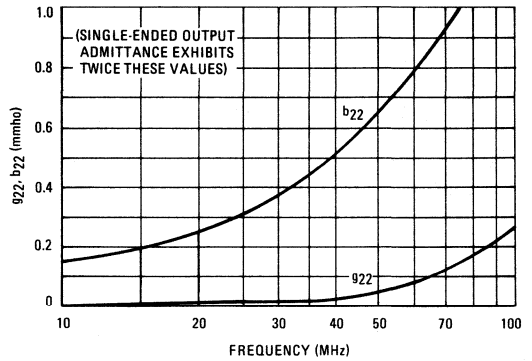


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

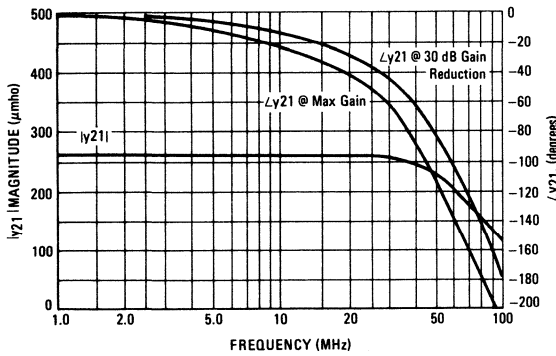


FIGURE 9 – DIFFERENTIAL OUTPUT VOLTAGE

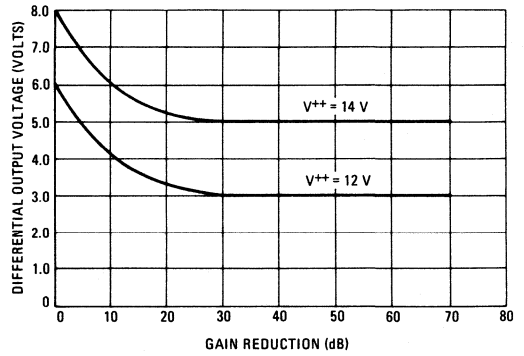


FIGURE 10 – MC1352 AGC CHARACTERISTICS

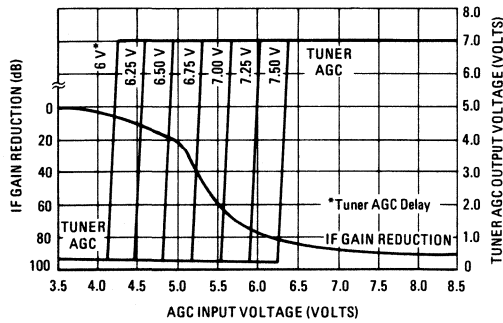
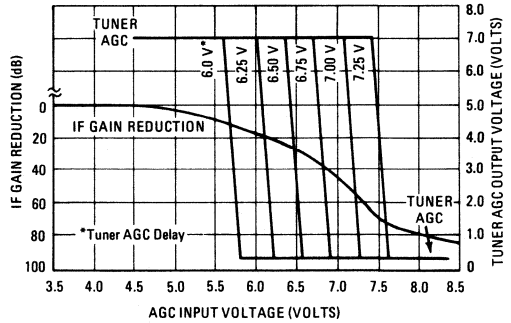
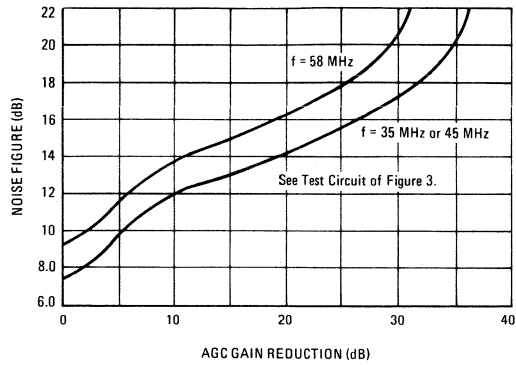


FIGURE 11 – MC1353 AGC CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)
($V^+ = +12\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 12 – TYPICAL NOISE FIGURE



For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control", by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

MC1355

FM IF AMPLIFIER

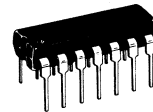
BALANCED MONOLITHIC FOUR-STAGE HIGH-GAIN FM/IF AMPLIFIER

... designed for use with Foster-Seeley discriminator or ratio detector in high quality FM systems.

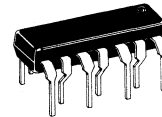
- High AM Rejection (60 dB typ)
- Wide Range of Supply Voltages (8 to 18 Vdc)
- Low Distortion (0.5% typ)

LIMITING FM IF AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



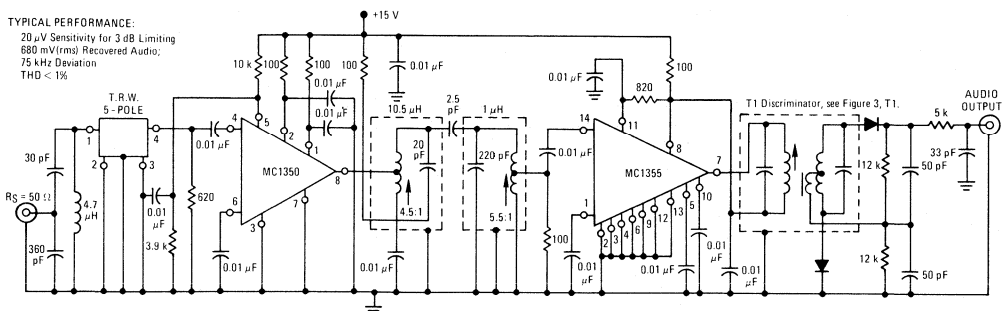
P SUFFIX
PLASTIC PACKAGE
CASE 605
TO-116



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TYPICAL FM-IF APPLICATION

TYPICAL PERFORMANCE:
20 μ V Sensitivity for 3 dB Limiting
680 mV(rms) Recovered Audio;
75 kHz Deviation
THD < 1%



When using the device as a non-saturating limiter the load must be chosen to prevent voltage saturation of the output stage. The load impedance can be calculated from:

$$R_L \leq \frac{2(V^+ - 5.3)}{5.0} \text{ kilohms}$$

See Packaging Information Section for outline dimensions.

MC1355 (continued)

MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

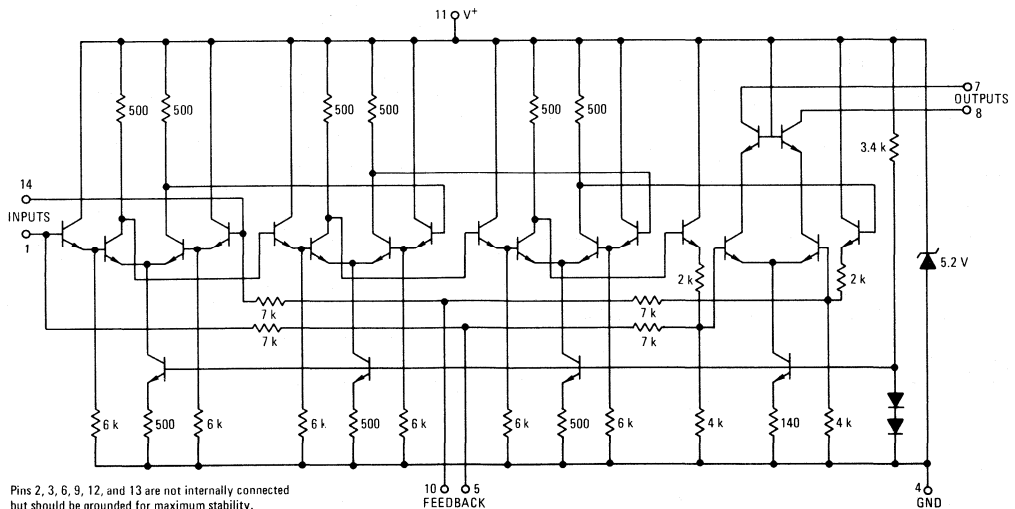
| Rating | Value | Unit |
|--|-------------|------------------------------|
| Output Voltage (pins 7 & 8) | 40 | Vdc |
| Supply Current to pin 11 | 20 | mA |
| Input Signal Voltage (single-ended) | 5.0 | V _{p-p} |
| Input Signal Voltage (differential) | 10 | V _{p-p} |
| Power Dissipation (package limitation) Derate above $T_A = +25^{\circ}\text{C}$ | 625 5.0 | mW mW/ $^{\circ}\text{C}$ |
| Operating Temperature Range (Ambient) | 0 to +75 | $^{\circ}\text{C}$ |
| Storage Temperature Range | -65 to +150 | $^{\circ}\text{C}$ |

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS ($V^+ = 15\text{ Vdc}$, $f = 10.7\text{ MHz}$, $T_A = +25^{\circ}\text{C}$, $R_S = 820\text{ ohms}$ unless otherwise noted)

| Characteristic | Min | Typ | Max | Units |
|---|-----|------------|-----|---------------------|
| Power Supply Voltage Range | 8.0 | 15 | 18 | Vdc |
| Total Circuit Current | — | 16 | — | mAdc |
| Total Output Stage Current | — | 4.2 | — | mA |
| Device Dissipation | — | 125 | — | mW |
| Internal Zener Voltage | — | 5.2 | — | Vdc |
| Input Signal for 3 dB Limiting | — | 175 | 250 | μV (rms) |
| Output Current Swing | 3.5 | 4.2 | 5.0 | mA p-p |
| AM Rejection (10 mv to 1.0 v (rms) input, FM @ 100%, AM @ 80%, Foster Seeley detector) | — | 60 | — | dB |
| Maximum AM Signal before Breakup (FM @ 100%, AM @ 80%) | — | — | 1.4 | V(rms) |
| Admittance Parameters | | | | |
| Y11 | — | 120 + j320 | — | μmhos |
| Y12 | — | j0.6 | — | μmho |
| Y21 | — | 8 + j5.9 | — | mhos |
| Y22 | — | 15 + j230 | — | μmhos |

FIGURE 2 – CIRCUIT SCHEMATIC



MC1355 (continued)

TYPICAL CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT

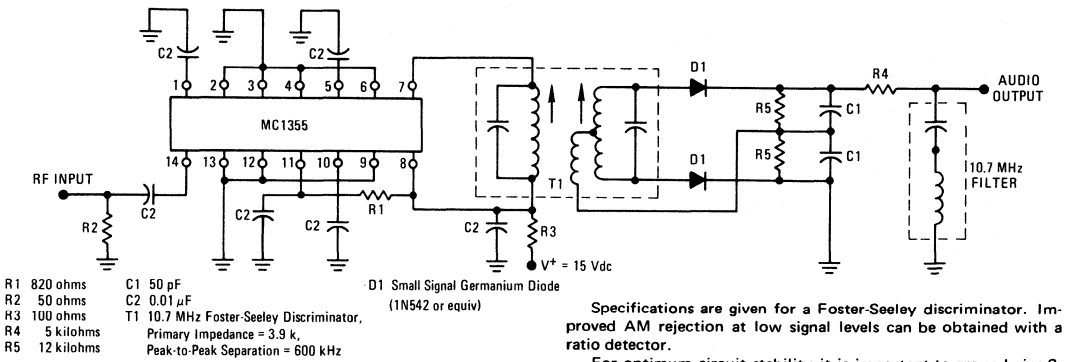


FIGURE 4 – AM REJECTION TEST BLOCK DIAGRAM

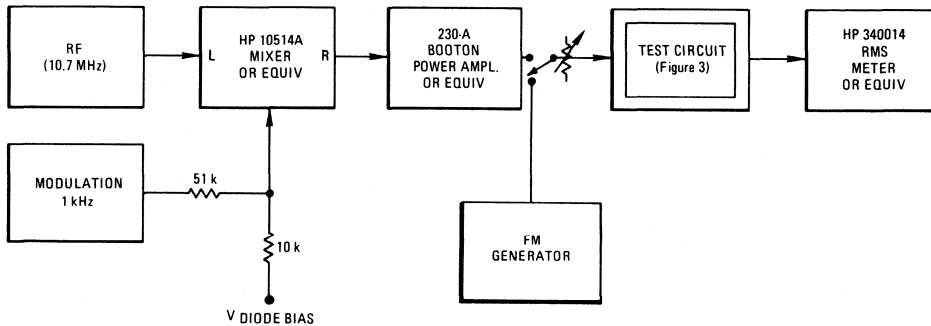


FIGURE 5 – LIMITING

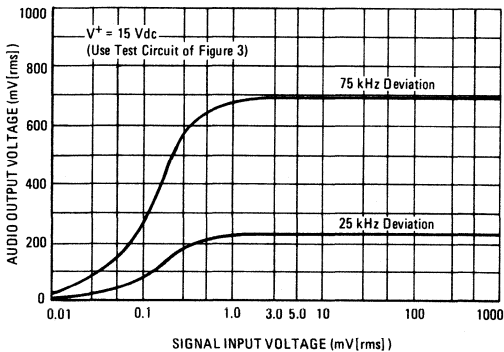
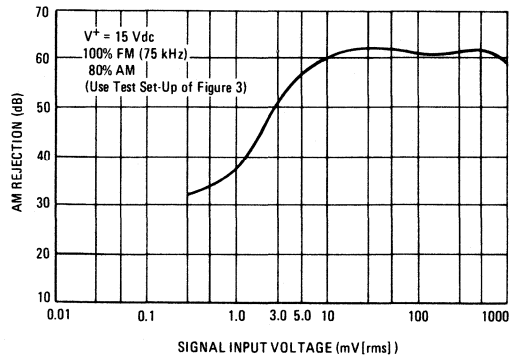


FIGURE 6 – AM REJECTION



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OUTPUT DISTORTION

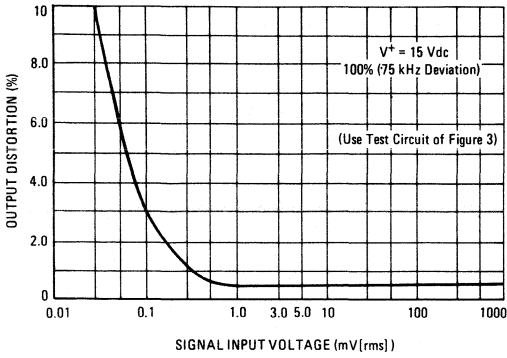


FIGURE 8 – SIGNAL-TO-NOISE RATIO SIGNAL

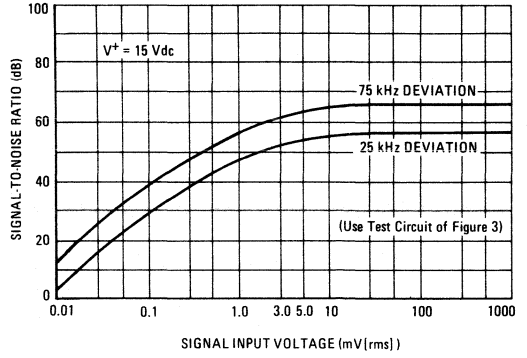
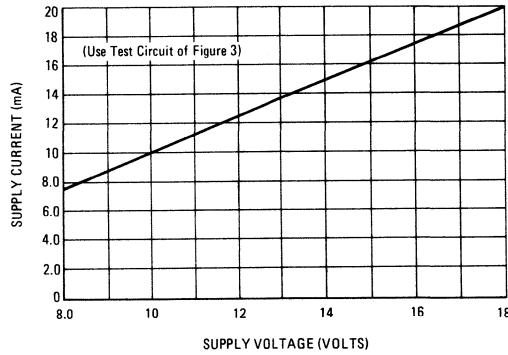


FIGURE 9 – TOTAL SUPPLY CURRENT



MC1357

SOUND IF AMPLIFIER

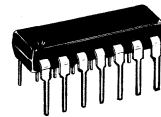
MONOLITHIC TV SOUND IF OR FM IF AMPLIFIER WITH QUADRATURE DETECTOR

- A Direct Replacement for the ULN2111A
- Greatly Simplified FM Demodulator Alignment
- Excellent Performance at $V^+ = 8.0$ Vdc

IF AMPLIFIER AND QUADRATURE DETECTOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

NOVEMBER 1970 — DS 9164 R1

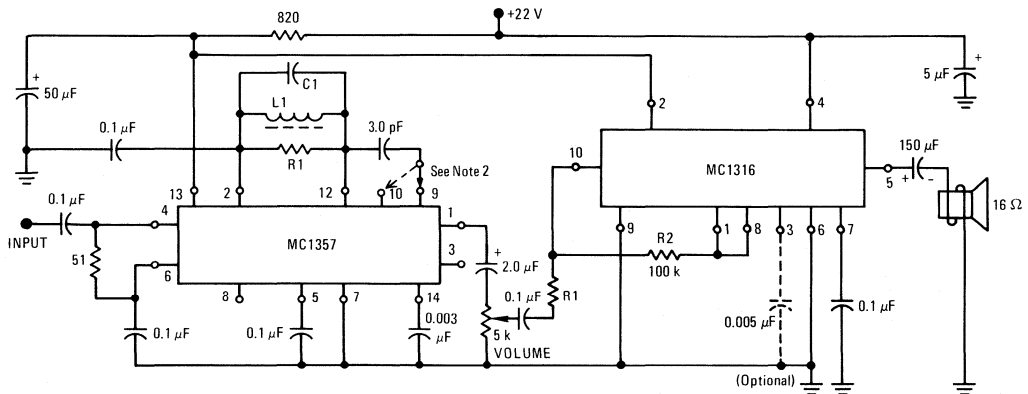


P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 — TV TYPICAL APPLICATION CIRCUIT



Typical Performance:
2 Watts Output
2% Distortion
250 μ V Sensitivity (3 dB Lim.)

C1 = 120 pF
L1 = 14 μ H
R1 = 20 k Ω
Q = 30

See Packaging Information Section for outline dimensions.

MC1357 (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Value | Unit |
|---|-------------|-----------------|
| Power Supply Voltage | 16 | V _{dc} |
| Input Voltage (Pin 4) | 3.5 | V _p |
| Power Dissipation (Package Limitation) | 625 | mW |
| Plastic Packages Derate above T _A = +25°C | 5.0 | mW/°C |
| Operating Temperature Range (Ambient) | 0 to +75 | °C |
| Storage Temperature Range | -65 to +150 | °C |

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V⁺ = 12 Vdc, T_A = +25°C unless otherwise noted)

| Characteristic | Pin | Min | Typ | Max | Units |
|--|-----|---------|------------|----------|-----------------|
| Drain Current V ⁺ = 8 V V ⁺ = 12 V | 13 | 10 — | 12 15 | 19 21 | mA |
| Amplifier Input Reference Voltage | 6 | — | 1.45 | — | V _{dc} |
| Detector Input Reference Voltage | 2 | — | 3.65 | — | V _{dc} |
| Amplifier High Level Output Voltage | 10 | 1.25 | 1.45 | 1.65 | V _{dc} |
| Amplifier Low Level Output Voltage | 9 | — | 0.145 | 0.2 | V _{dc} |
| Detector Output Voltage V ⁺ = 8 V V ⁺ = 12 V | 1 | — — | 3.7 5.4 | — — | V _{dc} |
| Amplifier Input Resistance | 4 | — | 5.0 | — | kΩ |
| Amplifier Input Capacitance | 4 | — | 11 | — | pF |
| Detector Input Resistance | 12 | — | 70 | — | kΩ |
| Detector Input Capacitance | 12 | — | 2.7 | — | pF |
| Amplifier Output Resistance | 10 | — | 60 | — | ohms |
| Detector Output Resistance | 1 | — | 200 | — | ohms |
| De-Emphasis Resistance | 14 | — | 8.8 | — | kΩ |

DYNAMIC CHARACTERISTICS (FM Modulation Freq. = 1.0 kHz, Source Resistance = 50 ohms, T_A = +25°C for all tests.)

(V⁺ = 12 Vdc, f_o = 4.5 MHz, Δf = ± 25 kHz, Peak Separation = 150 kHz)

| Characteristics | Pin | Min | Typ | Max | Units |
|---|-----|-----|------|-----|---------|
| Amplifier Voltage Gain (V _{in} ≤ 50 μV[rms]) | 10 | — | 60 | — | dB |
| AM Rejection* (V _{in} = 10 mV[rms]) | 1 | — | 36 | — | dB |
| Input Limiting Threshold Voltage | 4 | — | 250 | — | μV(rms) |
| Recovered Audio Output Voltage (V _{in} = 10 mV[rms]) | 1 | — | 0.72 | — | V(rms) |
| Output Distortion (V _{in} = 10 mV[rms]) | 1 | — | 3 | — | % |

(V⁺ = 12 Vdc, f_o = 5.5 MHz, Δf = ± 50 kHz, Peak Separation = 260 kHz)

| Characteristics | Pin | Min | Typ | Max | Units |
|---|-----|-----|-----|-----|---------|
| Amplifier Voltage Gain (V _{in} ≤ 50 μV[rms]) | 10 | — | 60 | — | dB |
| AM Rejection* (V _{in} = 10 mV[rms]) | 1 | — | 40 | — | dB |
| Input Limiting Threshold Voltage | 4 | — | 250 | — | μV(rms) |
| Recovered Audio Output Voltage (V _{in} = 10 mV[rms]) | 1 | — | 1.2 | — | V(rms) |
| Output Distortion (V _{in} = 10 mV[rms]) | 1 | — | 5 | — | % |

(V⁺ = 8.0 Vdc, f_o = 10.7 MHz, Δf = ± 75 kHz, Peak Separation = 550 kHz)

| Characteristics | Pin | Min | Typ | Max | Units |
|---|-----|-----|------|-----|---------|
| Amplifier Voltage Gain (V _{in} ≤ 50 μV[rms]) | 10 | — | 53 | — | dB |
| AM Rejection* (V _{in} = 10 mV[rms]) | 1 | — | 37 | — | dB |
| Input Limiting Threshold Voltage | 4 | — | 600 | — | μV(rms) |
| Recovered Audio Output Voltage (V _{in} = 10 mV[rms]) | 1 | — | 0.30 | — | V(rms) |
| Output Distortion (V _{in} = 10 mV[rms]) | 1 | — | 1.4 | — | % |

(V⁺ = 12 Vdc, f_o = 10.7 MHz, Δf = ± 75 kHz, Peak Separation = 550 kHz)

| Characteristics | Pin | Min | Typ | Max | Units |
|---|-----|-----|------|-----|---------|
| Amplifier Voltage Gain (V _{in} ≤ 50 μV[rms]) | 10 | — | 53 | — | dB |
| AM Rejection* (V _{in} = 10 mV[rms]) | 1 | — | 45 | — | dB |
| Input Limiting Threshold Voltage | 4 | — | 600 | — | μV(rms) |
| Recovered Audio Output Voltage (V _{in} = 10 mV[rms]) | 1 | — | 0.48 | — | V(rms) |
| Output Distortion (V _{in} = 10 mV[rms]) | 1 | — | 1.4 | — | % |

* 100% FM, 30% AM Modulation

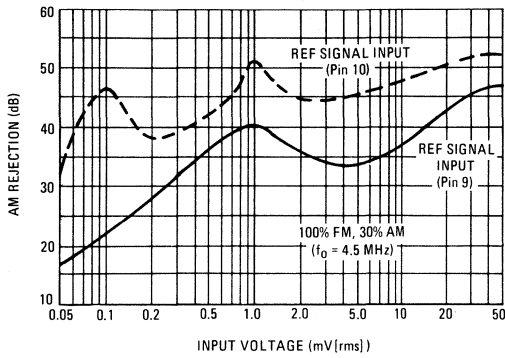
TYPICAL CHARACTERISTICS

($V_+ = 12\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

(Use Test Circuit of Figure 13)

($f_0 = 4.5\text{ MHz}$)

FIGURE 2 – AM REJECTION



($f_0 = 5.5\text{ MHz}$)

FIGURE 3 – AM REJECTION

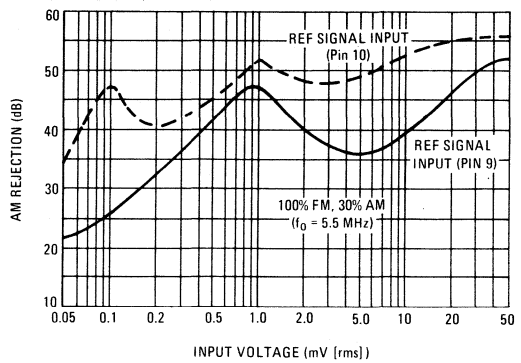


FIGURE 4 – DETECTED AUDIO OUTPUT

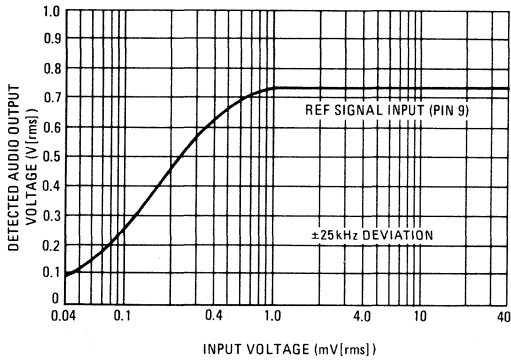


FIGURE 5 – DETECTED AUDIO OUTPUT

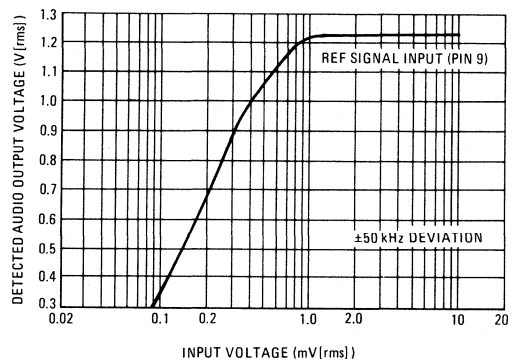


FIGURE 6 – DETECTOR TRANSFER CHARACTERISTIC

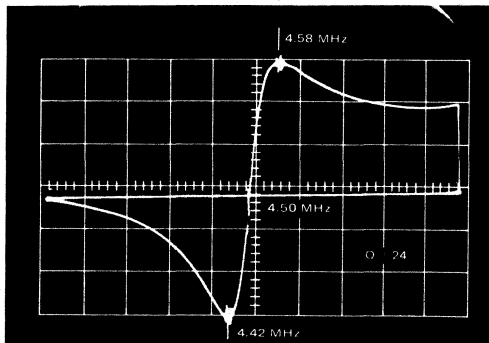
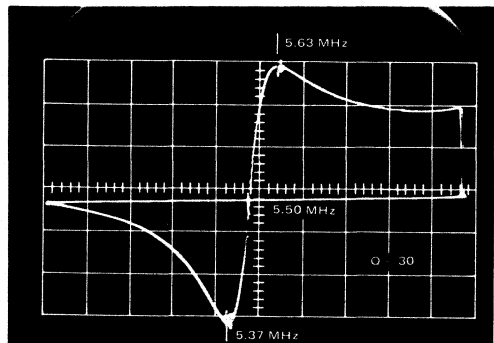


FIGURE 7 – DETECTOR TRANSFER CHARACTERISTIC



TYPICAL CHARACTERISTICS (continued)
 ($f_o = 10.7 \text{ MHz}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)
 (Use Test Circuit of Figure 13)

FIGURE 8 – AM REJECTION

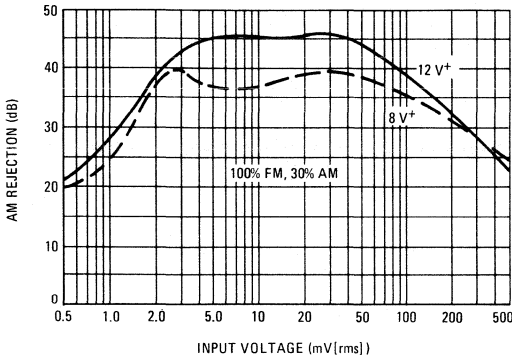


FIGURE 9 – AFC VOLTAGE DRIFT
 (1.0 mV INPUT CARRIER @ 10.7 MHz)

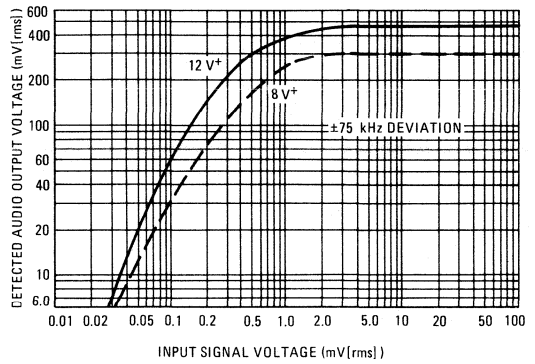


FIGURE 10 – LIMITING

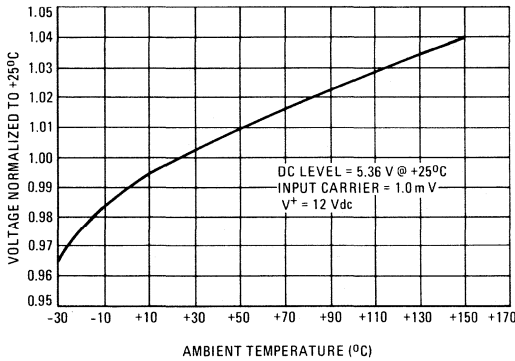


FIGURE 11 – SIGNAL-TO-NOISE RATIO

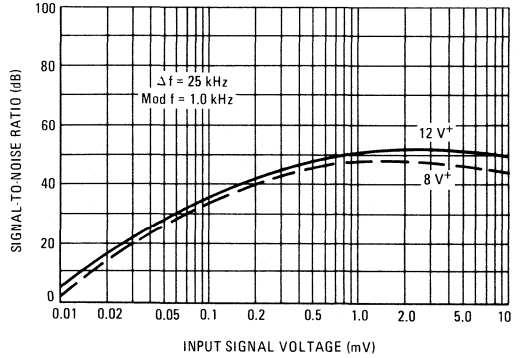


FIGURE 12 – DETECTOR TRANSFER CHARACTERISTIC

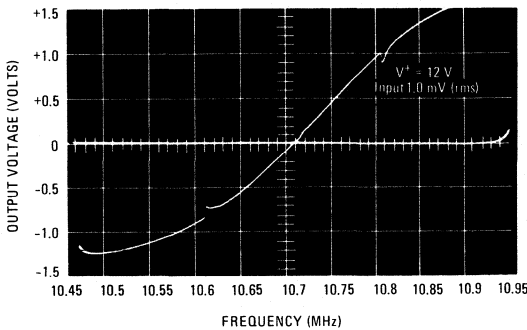
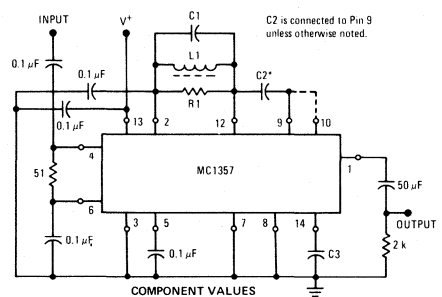


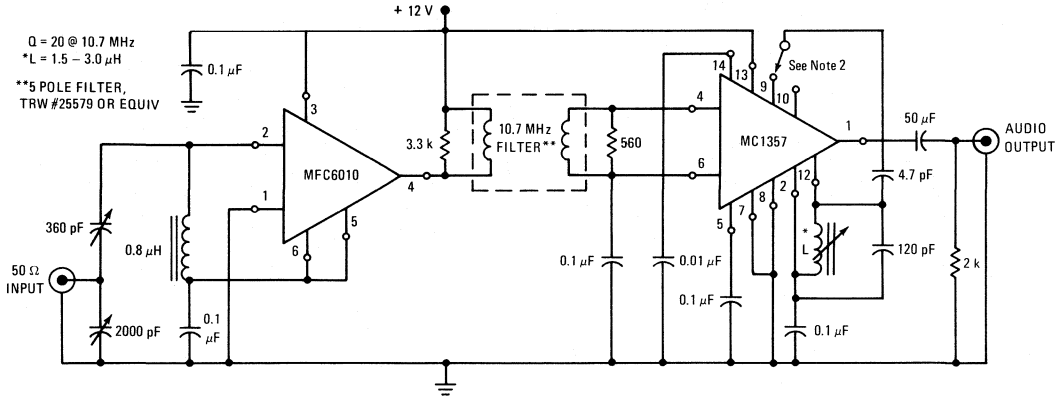
FIGURE 13 – TEST CIRCUIT



COMPONENT VALUES

| f | L1 | C1 | R1 | Q(R1, L1) | C2 | C3 |
|------|-----|-----|-----|-----------|-----|-------|
| MHz | μH | pF | kΩ | | pF | μF |
| 4.5 | 14 | 120 | 20 | 30 | 3.0 | 0.003 |
| 5.5 | 8.0 | 100 | 20 | 30 | 3.0 | 0.003 |
| 10.7 | 2.0 | 120 | 3.9 | 20 | 4.7 | 0.01 |

FIGURE 14 – FM RADIO TYPICAL APPLICATION CIRCUIT



Note 1:
 Information shown in Figures 15, 16, and 17 was obtained using the circuit of Figure 14.

Note 2:
 Optional input to the quadrature coil may be from either pin 9 or pin 10 in the applications shown. Pin 9 has commonly been used on this type of part to avoid overload with various tuning techniques. For this reason, pin 9 is used in tests on the preceding pages (except as noted). However, a significant improvement of limiting sensitivity can be obtained using pin 10, see Figure 17, and no overload problems have been incurred with this tuned circuit configuration.

FIGURE 15 – OUTPUT DISTORTION

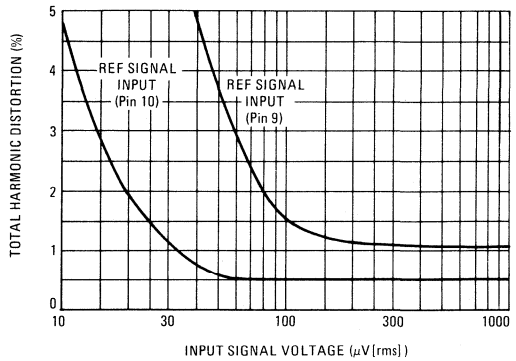


FIGURE 16 – SIGNAL-TO-NOISE RATIO

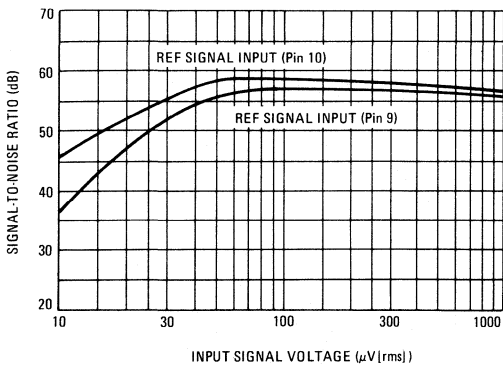


FIGURE 17 – RECOVERED AUDIO OUTPUT

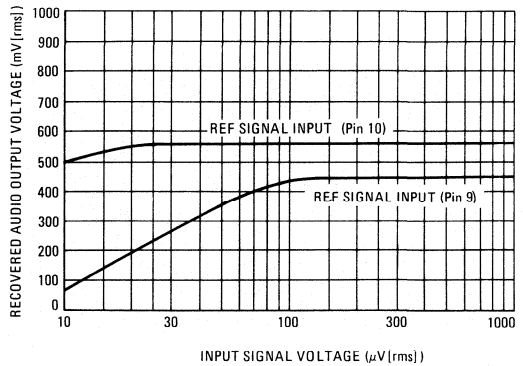
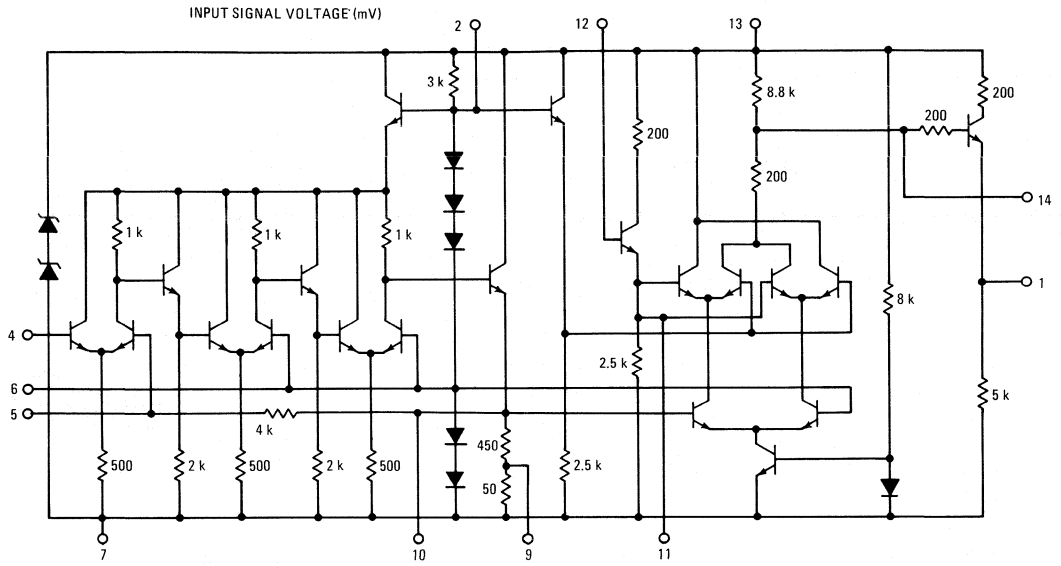


FIGURE 18 – CIRCUIT SCHEMATIC



MC1358

SOUND IF AMPLIFIER

TV SOUND IF AMPLIFIER

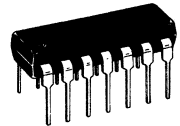
... a versatile monolithic device incorporating IF limiting, detection, electronic attenuation, audio amplifier, and audio driver capabilities.

- Direct Replacement for the CA3065
- Differential Peak Detector Requiring a Single Tuned Circuit
- Electronic Attenuator Replaces Conventional ac Volume Control – Range > 60 dB
- Excellent AM Rejection @ 4.5 and 5.5 MHz
- High Stability
- Low Harmonic Distortion
- Audio Drive Capability – 6.0 mA_{p-p}
- Minimum Undesirable Output Signal @ Maximum Attenuation

**IF AMPLIFIER, LIMITER,
FM DETECTOR, AUDIO DRIVER,
ELECTRONIC ATTENUATOR**

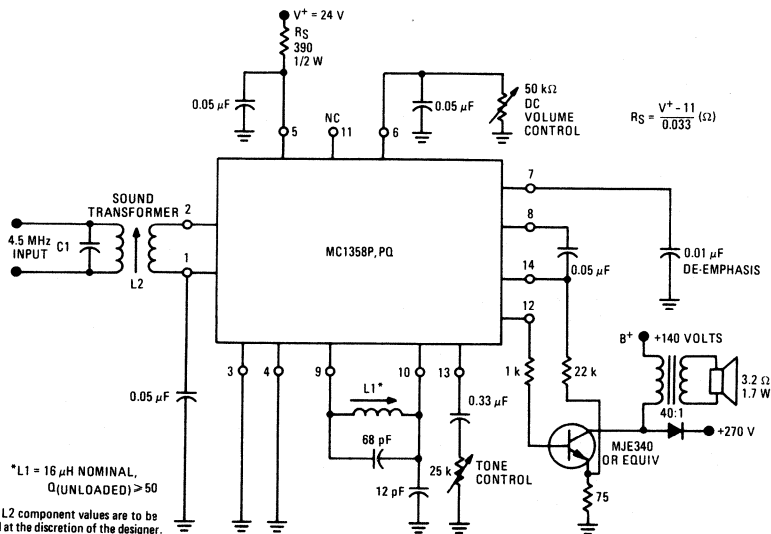
**MONOLITHIC SILICON
INTEGRATED CIRCUIT**

**P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116**



**PQ SUFFIX
PLASTIC PACKAGE
CASE 647**

FIGURE 1 – TYPICAL TV APPLICATION CIRCUIT



7

MC1358 (continued)

MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

| Rating | Value | Unit |
|--|-------------|------------------------|
| Input Signal Voltage (Pins 1 and 2) | ± 3.0 | Vdc |
| Power Supply Current | 50 | mA |
| Power Dissipation (Package Limitation) | | |
| Plastic Packages | 625 | mW |
| Derate above $T_A = +25^{\circ}\text{C}$ | 5.0 | mW/ $^{\circ}\text{C}$ |
| Operating Temperature Range (Ambient) | -20 to +75 | $^{\circ}\text{C}$ |
| Storage Temperature Range | -65 to +150 | $^{\circ}\text{C}$ |

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS ($V^+ = 24\text{ Vdc}$, $T_A = +25^{\circ}\text{C}$ unless otherwise noted)

| Characteristic | Pin | Min | Typ | Max | Unit |
|--|-----|------|-----|------|------|
| Regulated Voltage | 5 | 10.3 | 11 | 12.2 | Vdc |
| DC Supply Current ($V^+ = 9\text{ Vdc}$, $R_S = 0$) | 5 | 10 | 16 | 24 | mA |
| Quiescent Output Voltage | 12 | — | 5.1 | — | Vdc |

DYNAMIC CHARACTERISTICS ($V^+ = 24\text{ Vdc}$, $T_A = +25^{\circ}\text{C}$ unless otherwise noted)

| Characteristic | Min | Typ | Max | Unit |
|----------------|-----|-----|-----|------|
|----------------|-----|-----|-----|------|

IF AMPLIFIER AND DETECTOR

$f_o = 4.5\text{ MHz}$, $\Delta f = \pm 25\text{ kHz}$

| | | | | |
|--|-----|------|-----|---------------------|
| AM Rejection* ($V_{in} = 10\text{ mV [rms]}$) | 40 | 51 | — | dB |
| Input Limiting Threshold Voltage | — | 200 | 400 | $\mu\text{V (rms)}$ |
| Recovered Audio Output Voltage ($V_{in} = 10\text{ mV [rms]}$) | 0.5 | 0.70 | — | V (rms) |
| Output Distortion ($V_{in} = 10\text{ mV [rms]}$) | — | 0.4 | 2.0 | % |

$f_o = 5.5\text{ MHz}$, $\Delta f = \pm 50\text{ kHz}$

| | | | | |
|---|-----|------|-----|---------------------|
| AM Rejection* ($V_{in} = 10\text{ mV [rms]}$) | 40 | 53 | — | dB |
| Input Limiting Threshold Voltage | — | 200 | 400 | $\mu\text{V (rms)}$ |
| Recovered Audio Output Voltage ($V_{in} = 10\text{ mV [rms]}$) | 0.5 | 0.91 | — | V (rms) |
| Output Distortion ($V_{in} = 10\text{ mV [rms]}$) | — | 0.9 | — | % |
| Input Impedance Components ($f = 4.5\text{ MHz}$, measurement between pins 1 and 2) | | | | |
| Parallel Input Resistance | — | 17 | — | $\text{k}\Omega$ |
| Parallel Input Capacitance | — | 4.0 | — | pF |
| Output Impedance Components ($f = 4.5\text{ MHz}$, measurement between pin 9 and GND) | | | | |
| Parallel Output Resistance | — | 3.25 | — | $\text{k}\Omega$ |
| Parallel Output Capacitance | — | 3.6 | — | pF |
| Output Resistance, Detector | | | | |
| Pin 7 | — | 7.5 | — | $\text{k}\Omega$ |
| Pin 8 | — | 250 | — | Ω |

ATTENUATOR

| | | | | |
|--|----|------|-----|----|
| Volume Reduction Range (See Figure 8) (dc Volume Control = ∞) | 60 | — | — | dB |
| Maximum Undesirable Signal (See Note 1) (dc Volume Control = ∞) | — | 0.07 | 1.0 | mV |

AUDIO AMPLIFIER

| | | | | |
|---|------|-----|---|------------------|
| Voltage Gain ($V_{in} = 0.1\text{ V (rms)}$, $f = 400\text{ Hz}$) | 17.5 | 20 | — | dB |
| Total Harmonic Distortion ($V_o = 2.0\text{ V (rms)}$, $f = 400\text{ Hz}$) | — | 2.0 | — | % |
| Output Voltage (THD = 5%, $f = 400\text{ Hz}$) | 2.0 | 3.0 | — | V (rms) |
| Input Resistance ($f = 400\text{ Hz}$) | — | 70 | — | $\text{k}\Omega$ |
| Output Resistance ($f = 400\text{ Hz}$) | — | 270 | — | Ω |

* 100% FM, 30% AM Modulation.

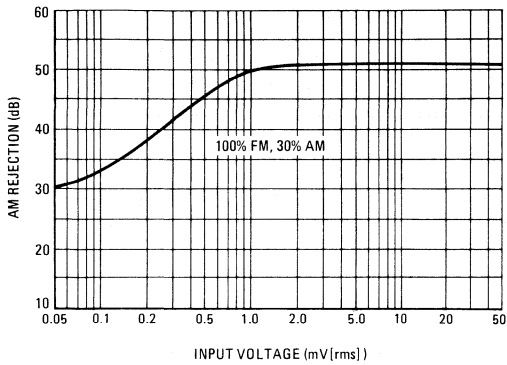
Note 1. Undesirable signal is measured at pin 8 when volume control is set for minimum output.

TYPICAL CHARACTERISTICS

($V^+ = 24\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

($f_o = 4.5\text{ MHz}$)

FIGURE 2 – AM REJECTION



($f_o = 5.5\text{ MHz}$)

FIGURE 3 – AM REJECTION

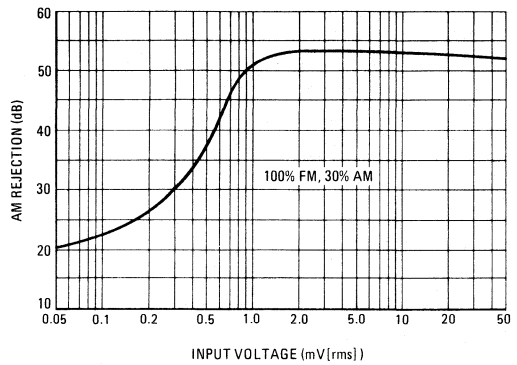


FIGURE 4 – DETECTED AUDIO OUTPUT

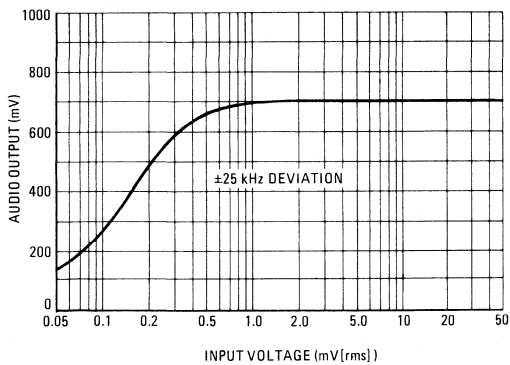


FIGURE 5 – DETECTED AUDIO OUTPUT

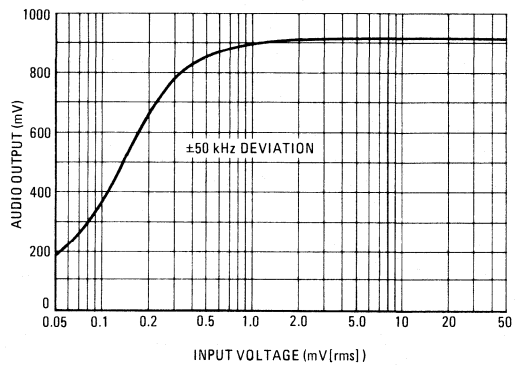


FIGURE 6 – IF AMPLIFIER AND DETECTOR THD

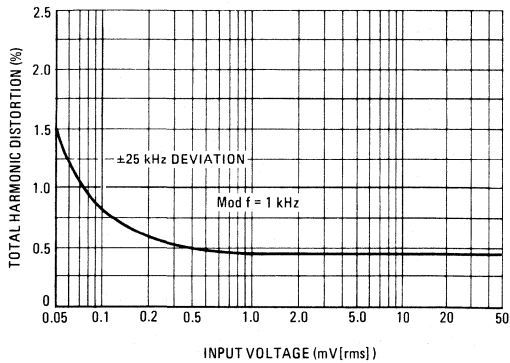
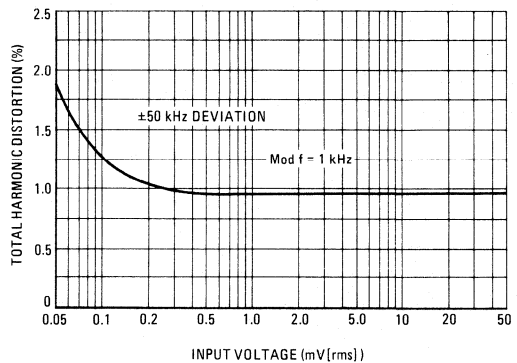


FIGURE 7 – IF AMPLIFIER AND DETECTOR THD



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – GAIN REDUCTION OF ATTENUATOR

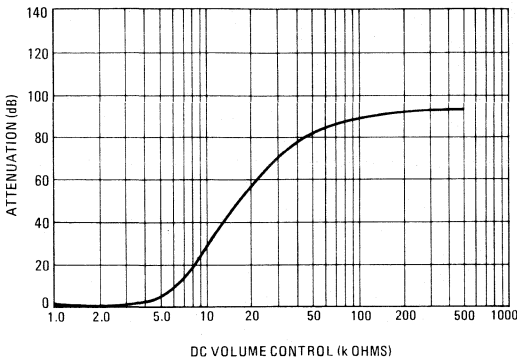


FIGURE 9 – AUDIO AMPLIFIER THD

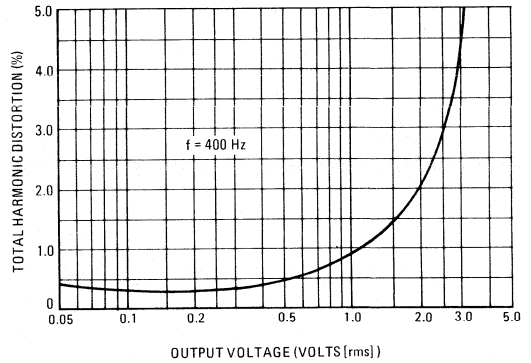


FIGURE 10 – IF FREQUENCY RESPONSE

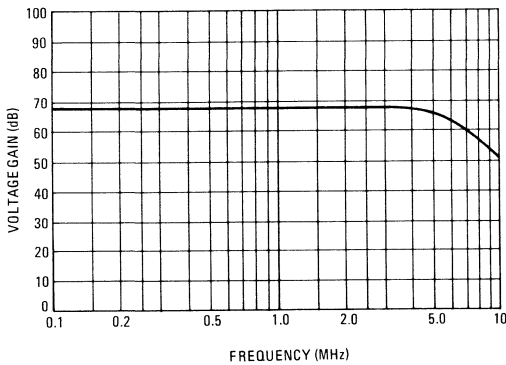


FIGURE 11 – IF FREQUENCY RESPONSE TEST CIRCUIT

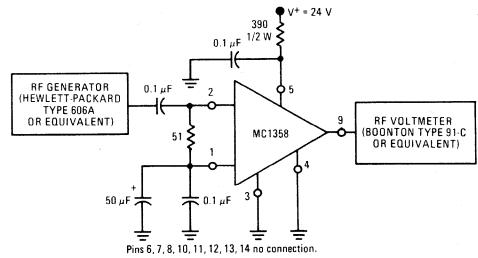


FIGURE 12 – AM REJECTION, DETECTED AUDIO, THD, ATTENUATION TEST CIRCUIT

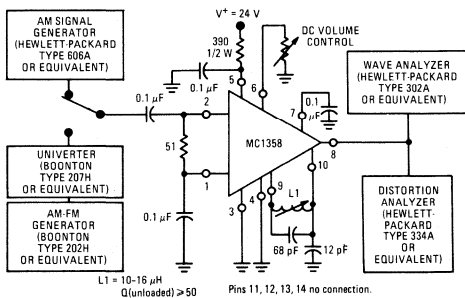


FIGURE 13 – AUDIO VOLTAGE GAIN, AUDIO THD TEST CIRCUIT

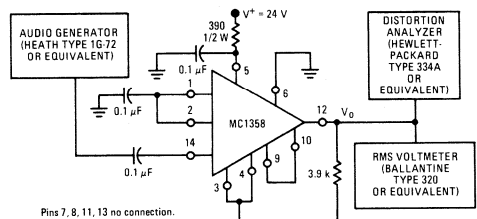
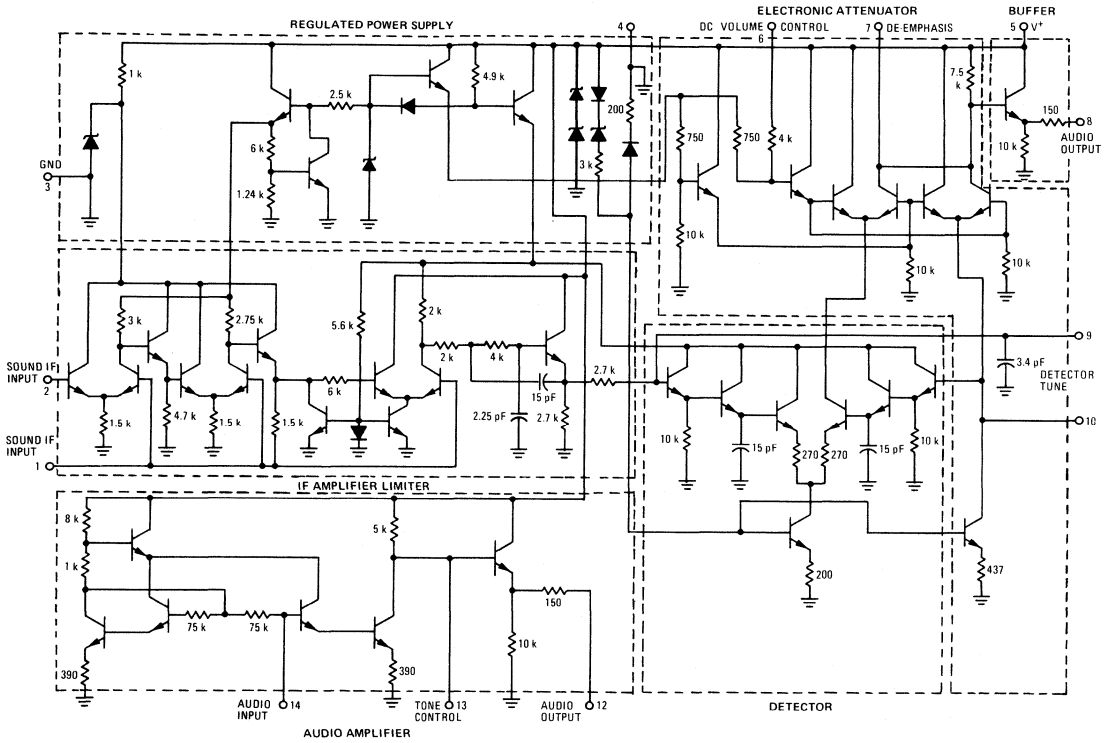


FIGURE 14 – CIRCUIT SCHEMATIC



7

MC1364

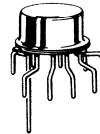
AUTOMATIC FREQUENCY CONTROL

MONOLITHIC TV AUTOMATIC FREQUENCY CONTROL

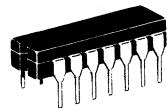
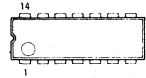
- High Gain Amplifier – 18 mV Input for Full Output
- Direct Replacement for the CA3064
- Also Available in the 14-Lead Dual In-Line Package

AUTOMATIC FREQUENCY CONTROL

MONOLITHIC SILICON INTEGRATED CIRCUIT

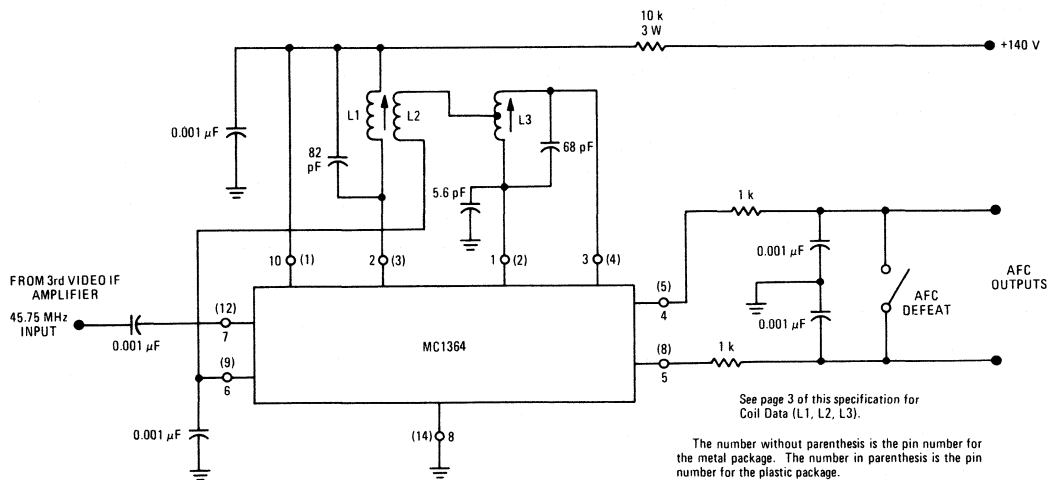


G SUFFIX
CASE 686
METAL PACKAGE



P SUFFIX
CASE 646
(TO-116)
PLASTIC PACKAGE

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



See page 3 of this specification for
Coil Data (L1, L2, L3).

The number without parenthesis is the pin number for the metal package. The number in parenthesis is the pin number for the plastic package.

Metal Package, Pin 9 – no connection
Plastic Package, Pins 6,7,10,11,13 – no connection

See Packaging Information Section for outline dimensions.

MC1364 (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted, see Note 1)

| Rating | MC1364G | MC1364P | Unit |
|---|-------------|-------------|-------------|
| Input Signal Voltage (Pin 7 to 8) | +2.0, -10 | +2.0, -10 | Vdc |
| Output Collector Voltage (Pins 2 and 8) | 20 | 20 | Volts |
| Power Dissipation (Package Limitation) Derate above T _A = +25°C | 680 5.6 | 625 5.0 | mW mW/°C |
| Operating Temperature Range | -40 to +85 | 0 to +75 | °C |
| Storage Temperature Range | -65 to +150 | -65 to +125 | °C |

ELECTRICAL CHARACTERISTICS (V_{CC} = +30 Vdc, T_A = +25°C, see Test Circuit of Figure 4 unless otherwise noted.)

| Characteristic | Min | Typ | Max | Unit |
|---|------|------|------|------|
| Total Device Dissipation | — | 140 | — | mW |
| Total Supply Current | — | 12 | — | mA |
| Current Drain, Total (Reduce V _{CC} so that V _{I0} = 10.5 Vdc) | 4.0 | 6.5 | 9.5 | mA |
| Zener Regulating Voltage | 10.9 | 11.8 | 12.8 | V |
| Quiescent Current to Pin 2 | 1.0 | 2.0 | 4.0 | mA |
| Quiescent Voltage at Pin 4 or Pin 5 | 5.0 | 6.6 | 8.0 | V |
| Output Offset Voltage (Pin 4 to Pin 5) | -1.0 | 0 | +1.0 | V |

DESIGN PARAMETERS, TYPICAL VALUES (V_{CC} = +30 Vdc, R_S = 1.5 k, f = 45.75 MHz)

| Parameter | Symbol | Typ | Unit |
|-----------------------------|-----------------|------------|-------|
| Input Admittance | Y ₁₁ | 0.4 + j1 | mmho |
| Reverse Transfer Admittance | Y ₁₂ | 0 + j3.4 | μmho |
| Forward Transfer Admittance | Y ₂₁ | 110 + j140 | mmhos |
| Output Admittance (Pin 2) | Y ₂₂ | 0.02 + j1 | mmho |

Note 1: Pin numbers used in the above tables are for the metal package, Case 686. For corresponding pin numbers for the plastic package, Case 646, see the Test Circuit, Figure 4.

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

TYPICAL CHARACTERISTICS

(See Test Circuit of Figure 2)

FIGURE 2 – TYPICAL NARROW BAND DYNAMIC CHARACTERISTICS

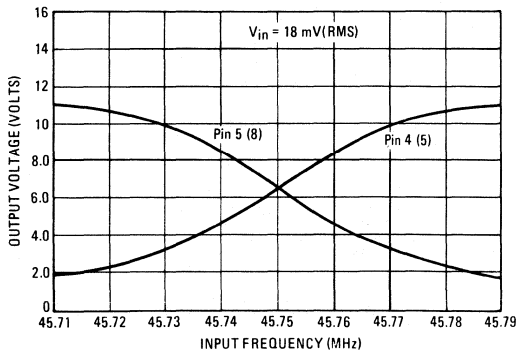


FIGURE 3 – TYPICAL WIDE BAND DYNAMIC CHARACTERISTICS

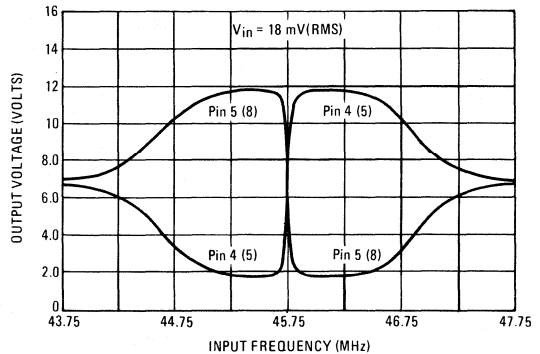
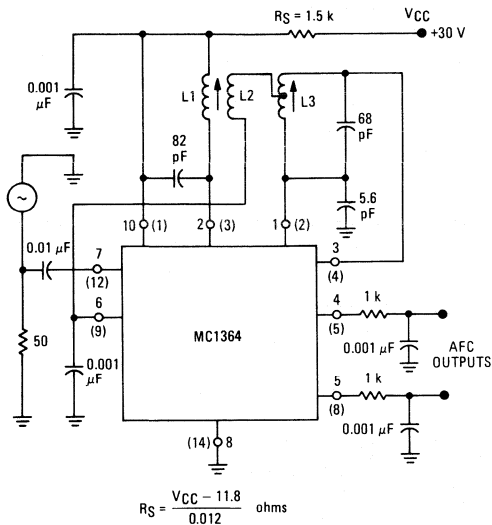


FIGURE 4 – TEST CIRCUIT



$$R_S = \frac{V_{CC} - 11.8}{0.012} \text{ ohms}$$

The number without parenthesis is the pin number for the metal package. The number in parenthesis is the pin number for the plastic package.

Metal Package, Pin 9 – no connection
Plastic Package, Pins 6,7,10,11,13 – no connection

COIL DATA FOR DISCRIMINATOR WINDINGS FOR FIGURES 1 AND 4

- L1 – Discriminator Primary: 3-1/6 turns; AWG #20 enamel-covered wire – close-wound, at bottom of coil form. Inductance of L1 = 0.165 μH; Q_o = 120 at f_o = 45.75 MHz. Start winding at Terminal #6; finish at Terminal #1. See Notes below.
- L2 – Tertiary Windings: 2-1/6 turns; AWG #20 enamel-covered wire – close-wound over bottom end of L1. Start winding at Terminal #3; finish at Terminal #4. See Notes below.
- L3 – Discriminator Secondary: 3-1/2 turns; AWG #20 enamel-covered wire, center-tapped, space wound at bottom of coil form. Start winding at Terminal #2; finish at Terminal #5, connect center tap to Terminal #7. See Notes below.

- Notes:
1. Coil Forms; Cylindrical; –0.30" Dia. Max.
 2. Tuning Core: 0.250" Dia. x 0.37" Length. Material: Carbinol J or equivalent.
 3. Coil Form Base: See drawing below.
 4. End of coil nearest terminal board to be designated the winding start end.
 5. Mount the coils 3/4" apart, center to center.

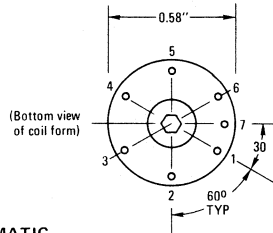
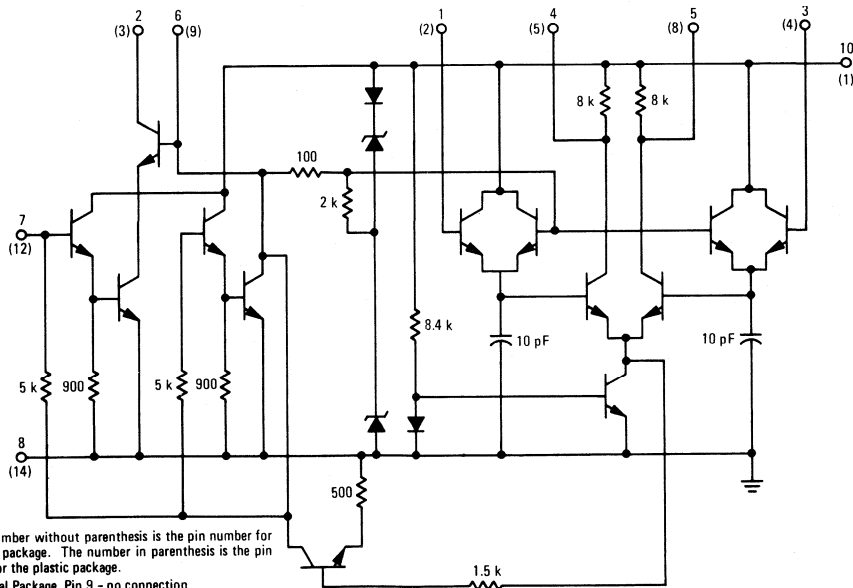


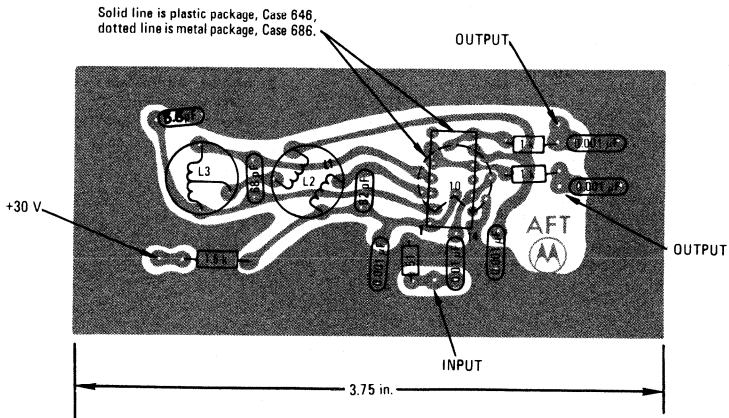
FIGURE 5 – CIRCUIT SCHEMATIC



The number without parenthesis is the pin number for the metal package. The number in parenthesis is the pin number for the plastic package.

Metal Package, Pin 9 – no connection
Plastic Package, Pins 6,7,10,11,13 – no connection

FIGURE 6 – PRINTED CIRCUIT BOARD AND PARTS ARRANGEMENT
(Copper Side)



MC1370P

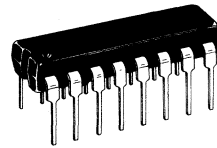
CHROMA SUBCARRIER SYSTEM

TELEVISION CHROMA SUBCARRIER REGENERATOR

... a monolithic device designed for solid-state television receivers, provides a gated voltage controlled oscillator, phase-locked loop and dc hue control.

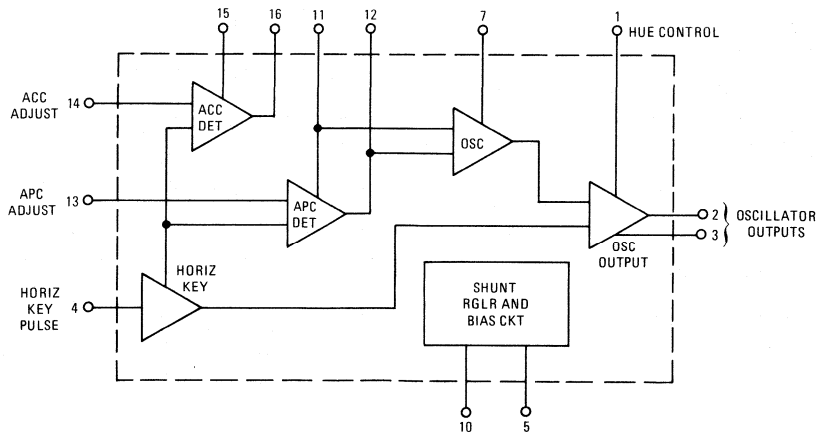
- Sensitive Voltage Controlled 3.58 MHz Crystal Oscillator
- High-Gain Automatic Phase Control (APC) Loop
- Wide-Range dc Control of Regenerated Subcarrier Phase
- Synchronous Automatic Chroma Control (ACC) Detector
- Internal Shunt Regulated Power Supply
- Internal Gating for Color Burst
- Complements MC1371P Color IF Amplifier
- Direct Replacement for the CA3070

TELEVISION CHROMA SUBCARRIER REGENERATOR MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

FIGURE 1 - MC1370P SYSTEM BLOCK DIAGRAM



MC1370P (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Value | Unit |
|---|-------------|----------------------------|
| Maximum Supply Voltage (through 470 ohms to pin 10) | 30 | Vdc |
| Power Dissipation (Package Limitation) Plastic Package Derate above $T_A = +25^\circ\text{C}$ | 625 5.0 | mW mW/ $^\circ\text{C}$ |
| Operating Temperature Range (Ambient) | 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | -65 to +150 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS ($V_{CC} = +24\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Min | Typ | Max | Unit |
|----------------|-----|-----|-----|------|
|----------------|-----|-----|-----|------|

STATIC CHARACTERISTICS (See Test Circuit of Figure 2, S1, S2 and S3 in position 1 unless otherwise noted.)

| | | | | |
|---|------|------|------|---------------|
| Power Supply Current (S2 in position 2) | — | 27 | — | mA |
| Regulator Voltage (pin 10) | 11 | 11.8 | 12.9 | Vdc |
| Load Regulation (pin 10) (V_{CC} from +21 V to +27 V) | — | 35 | — | mVdc |
| Oscillator Current (pins 2 and 3, S2 in position 2) | 4.1 | 6.5 | 7.5 | mA |
| APC Detector Current (pin 11 or pin 12) | 1.0 | 1.5 | 1.8 | mA |
| ACC Detector Current (pin 15 or pin 16) | 1.0 | 1.5 | 1.8 | mA |
| APC Detector Leakage Current (pin 11 or 12, S2 in position 3) | — | — | 40 | μA |
| ACC Detector Leakage Current (pin 15 or 16, S2 in position 3) | — | — | 30 | μA |
| APC Detector Balance (voltage between pins 11 and 12) | -375 | -40 | +375 | mVdc |
| ACC Detector Balance (voltage between pins 15 and 16) | -300 | -50 | +300 | mVdc |
| Oscillator Control Balance (voltage between pins 7 and 8, S2 in position 3, S3 in position 2) | -330 | -10 | +330 | mVdc |
| Oscillator Gate Leakage (pin 2 and pin 3) | — | — | 2.0 | μA |
| Voltage (pin 1) | — | 100 | 300 | mVdc |
| S2 in position 2 | — | 7.2 | 7.7 | Vdc |
| S1 and S2 in position 2 | — | 6.0 | 6.5 | 7.0 |
| (pin 13) S2 in position 2 | — | 6.0 | 6.5 | 7.0 |
| (pin 14) S2 in position 2 | — | 6.0 | 6.5 | 7.0 |
| (pin 6) S2 in position 2 | — | 2.8 | — | — |

DYNAMIC CHARACTERISTICS ($E_{\text{burst}} = 200\text{ mVp-p}$ at pin 13, see test circuit of Figure 3 and note for setup.)

| | | | | | |
|---|--|--------|--------------|--------|------------|
| Oscillator Output Voltage | (pin 2, S1 in position 1) (pin 3, S1 in position 3) | — — | 1.6 1.6 | — — | Vp-p |
| Oscillator Control Sensitivity (β) | | — | 10 | — | Hz/mV |
| Oscillator Pull-in Range | (Above $f_O = 3.579545\text{ MHz}$) (Below $f_O = 3.579545\text{ MHz}$) | — — | +400 -600 | — — | Hz |
| APC Loop Static Phase Error (with oscillator free-running frequency offset) | | — | 0.02 | — | Deg/Hz |
| APC Detector Sensitivity (μ) | | — | 5.0 | — | mV/Deg |
| ACC Detector Sensitivity (ACC output level change for input burst level change) | | — | 1.4 | — | mVdc/mVp-p |
| Oscillator Noise Bandwidth (f_{NN}) | | — | 150 | — | Hz |
| APC Filter Damping Coefficient (K) | | — | 0.5 | — | — |
| Input Impedance (pin 13) | | — | 2.1 | — | k Ω |
| (pin 14) | | — | 2.1 | — | — |
| (pin 6) | | — | 2.2 | — | — |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

MC1370P (continued)

FIGURE 2 – STATIC CHARACTERISTICS TEST CIRCUIT

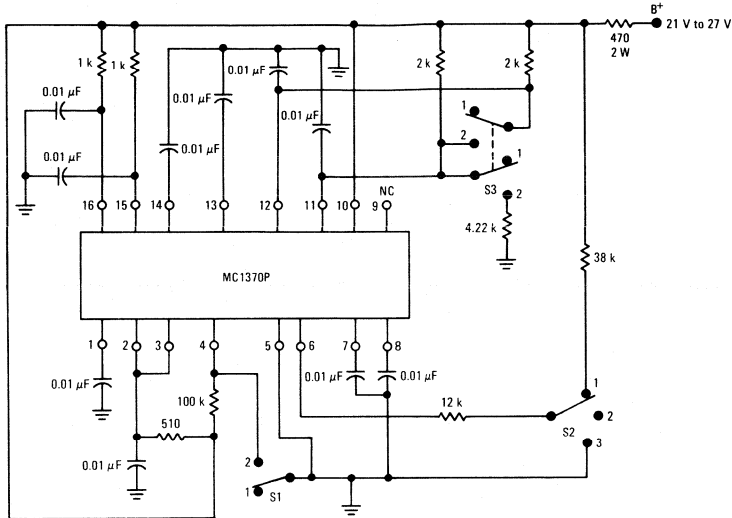
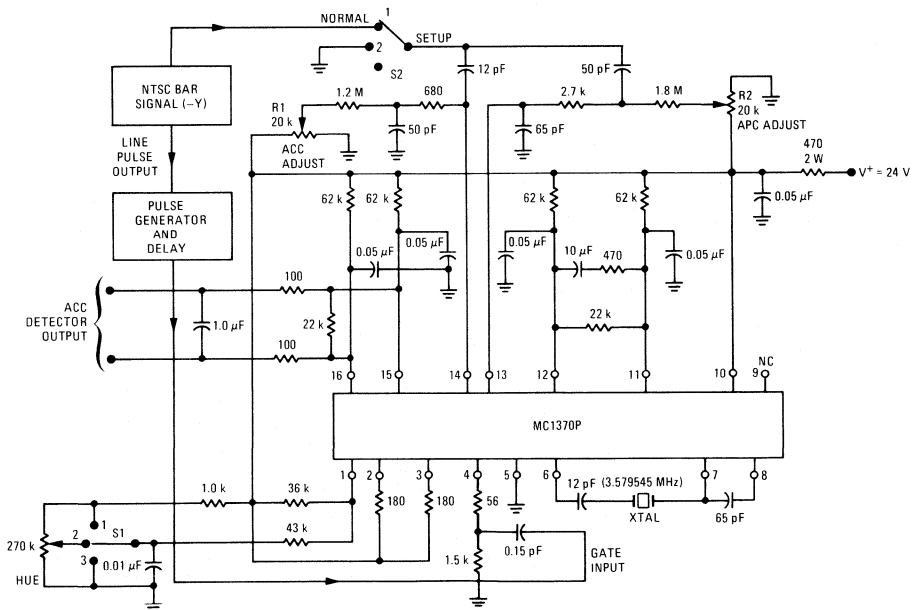


FIGURE 3 – DYNAMIC CHARACTERISTICS TEST CIRCUIT



NOTE: The Set-up Procedure for Dynamic Characteristics Test Circuit

The signal source is an NTSC color bar generator (minus luminance or Y content) applied through an adjustable 3.58 MHz attenuator. The generator horizontal output is used to trigger a pulse generator set to give an output pulse of +4.0 volts, 4.5 µs wide, at a repetition rate of 15.734 kHz. The pulse delay is adjusted

to center the pulse during the burst of the color signal (compare gated portion of output at pin 2 or 3 with burst pulse of signal). With S1 set to position 2 and S2 set to position 2, the oscillator is adjusted to 3.579545 MHz by R2. R1 is adjusted to produce zero offset between pins 15 and 16. When S2 is set to position 1, the oscillator should synchronize to the incoming signal.

FIGURE 4 — TYPICAL CHROMA APPLICATIONS CIRCUIT
(MC1370P, MC1371, MC1328 AND MPSU10)

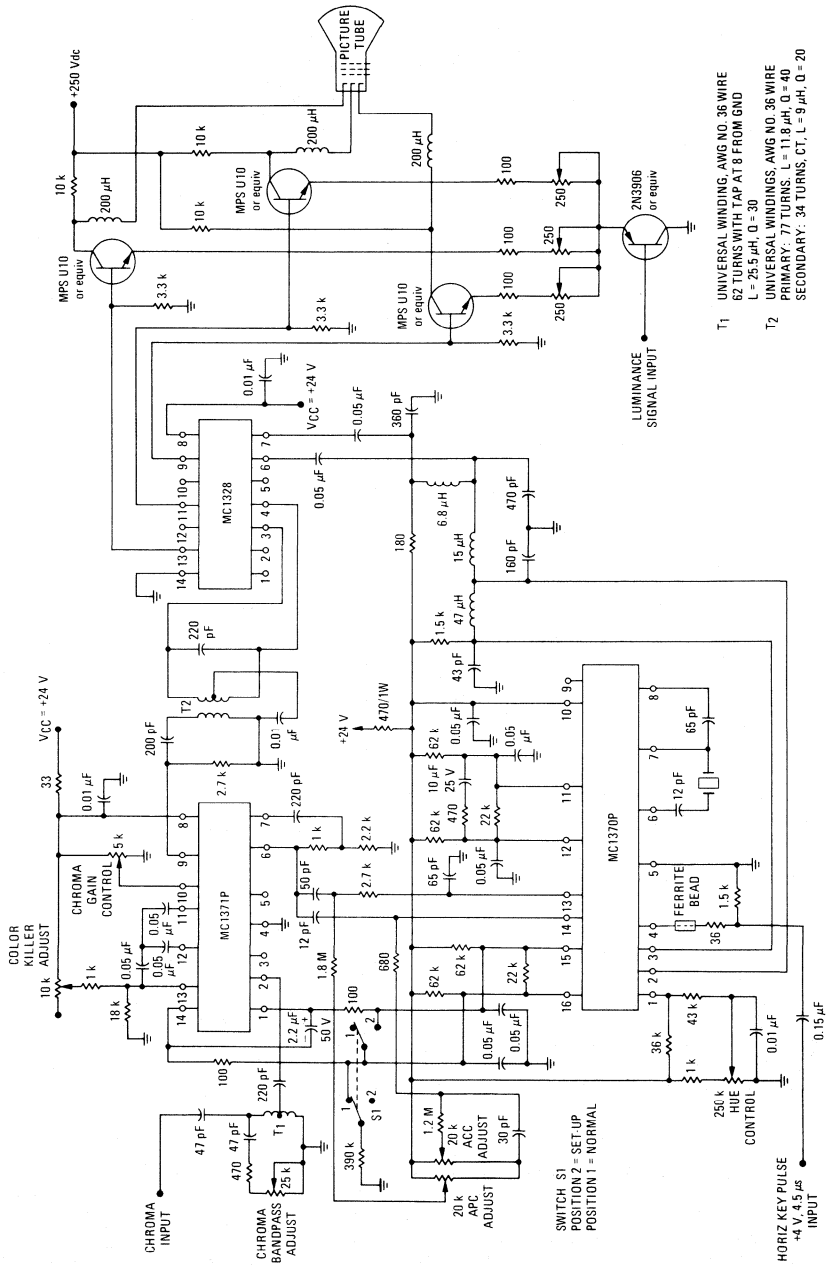
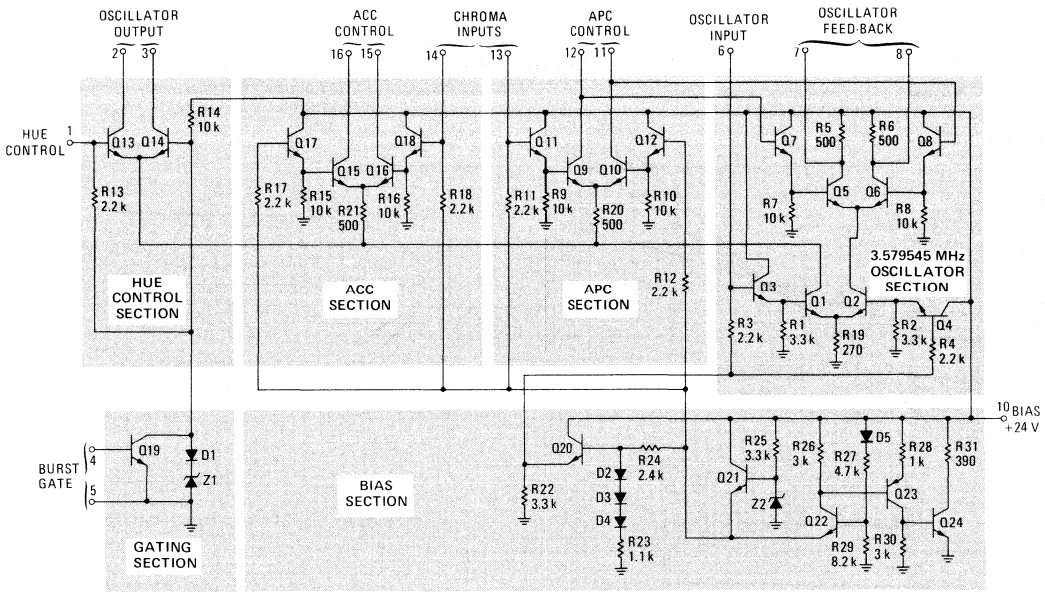


FIGURE 5 – CIRCUIT SCHEMATIC



Pin 9 no connection.

CIRCUIT DESCRIPTION

The MC1370 monolithic circuit provides the sub-carrier regeneration function necessary for a color television receiver to decode the NTSC color signal. An internal gate extracts the burst voltage and this signal is processed in two-phase detectors, the quadrature detector controls the phase of the local oscillator and the in-phase detector is used to provide a noise immune ACC and color killer control voltage. A shunt regulator sets the bias voltages and ensures stable operation when there are supply voltage variations.

The basic 3.579545 MHz oscillator consists of the differential amplifier (Q1 and Q2) with a feed-back loop through a quartz crystal operating in series resonance from Q2 collector to the noninverting input of the amplifier represented by Q1 base. To control the oscillator frequency the phase shift of the feed-back path is made variable by the addition of Q5 and Q6. A capacitor connected between pins 7 and 8, together with the collector loads, forms a RC phase-shift network. Consequently, the oscillator signal appearing at pin 7 can be moved in phase over a 45° range by the differential bias applied to Q5 and Q6 bases. The crystal between pins 7 and 6 completes the feed-back loop. The automatic phase control to the upper differential pairs of the (Q5, Q6) oscillator is through the buffer stages Q7 and Q8. The oscillator amplifier is buffered by Q3 and Q4. Output from the oscillator is obtained from the collector of Q1 and is essentially a square wave of 9 mA peak-to-peak with a frequency range of several hundred Hertz.

The control voltage for Q5 and Q6 is obtained from the phase detector Q9 and Q10. As Q1 is the current source for this pair, the voltages appearing at pins 11 and 12 will correspond to the phase difference between the oscillator current and the burst signal applied to pin 13. The loop characteristics are controlled in part

by a filter connected between pins 11 and 12. This is usually a double-time constant network to yield good pull-in times with a low-noise bandwidth.

To ensure that the quadrature phase detector functions only during the burst portion of the incoming chroma signal, the detector is gated into conduction by a pulse from the line flyback transformer — applied at pin 4. This has the additional advantage that the average current in the phase detector has been reduced by the gate duty factor thus relaxing the input offset stability requirements of the differential pair and enabling them to be used with high dc gain.

For the ACC control voltage and color-killer function a similar phase detector, Q15 and Q16, is used. However, the chroma signal input to pin 14 is phase shifted externally by 90° with respect to pin 13. As a result, Q15 and Q16 is an in-phase detector and the control voltage at pins 15 and 16 will be proportional to the amplitude of the burst. Thus filtering of pins 15 and 16 provides the control voltage for the gain control stage in the chroma IF and an indication of the incoming signal strength for the color-killer circuit.

When the phase detectors are not gated "on" by a positive pulse at pin 4, the bases of Q13 and Q14 are held above the bases of the phase detector inputs. Therefore, between gate pulses, all the current from the oscillator output Q1 passes through Q13 and Q14 to pins 2 and 3. When a phase-shift network is connected between pins 2 and 3, the phase of the oscillator drive to the demodulators can be controlled by changing the relative conduction of Q13 and Q14 with a bias on pin 1. As a result the oscillator output is controlled in phase providing a dc hue control and is gated "off" during the burst period, negating the need for burst blanking in the chroma IF amplifier.



TYPICAL CHARACTERISTICS

FIGURE 6 – STATIC PHASE ERROR versus FREQUENCY OFFSET

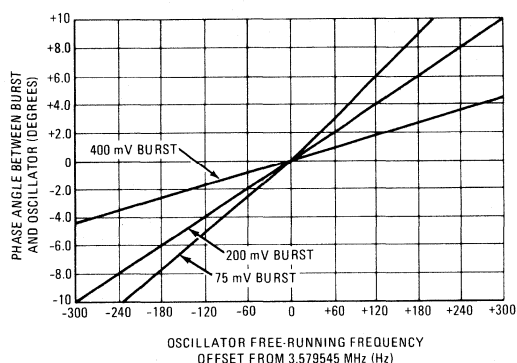


FIGURE 7 – PULL-IN FREQUENCY RANGE versus BURST INPUT VOLTAGE LEVEL

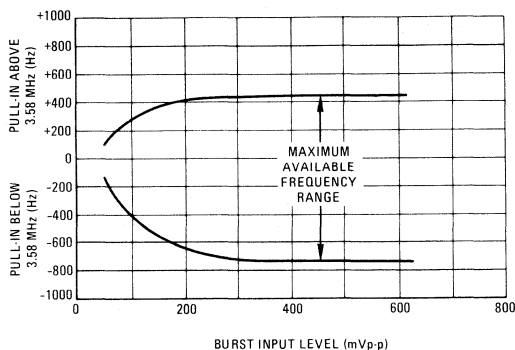


FIGURE 8 – ACC DETECTOR SENSITIVITY

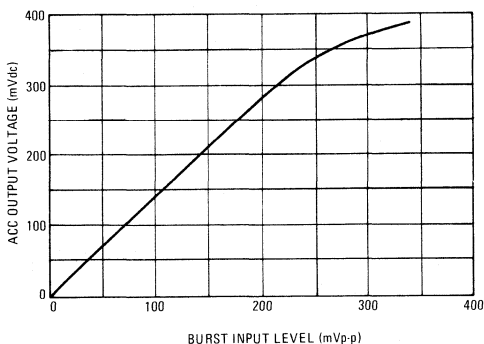
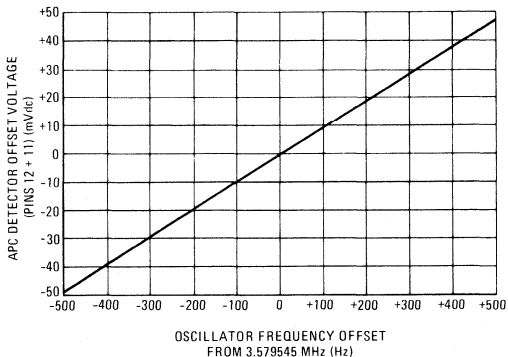


FIGURE 9 – OSCILLATOR SENSITIVITY



DEFINITIONS

Oscillator Sensitivity (β)

... the change in oscillator free-running frequency for a change in differential control voltage, measured in Hertz/millivolts.

APC Detector Sensitivity (μ)

... the differential voltage change produced at the detector output for a given change in oscillator phase relative to burst phase, measured for a given burst input amplitude in millivolts/degrees.

ACC Detector Sensitivity

... the differential voltage produced at the detector output for a

given change in burst input amplitude with the oscillator locked in synchronism, measured in millivolts dc/millivolts (p-p).

Noise Bandwidth (f_N)

... actually noise semibandwidth, $f_{NN} (= 2 \times f_N)$; a measure of the susceptibility of the burst channel to thermal noise (i.e. dynamic phase error).

Filter Damping Coefficient (K)

... describes the shape of the loop input phase versus output phase response ($Q\omega$) - $K = 1$ represents critical damping, $K > 1$ over damping.

MC1371P

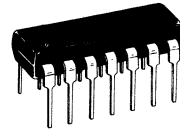
CHROMA IF AMPLIFIER

TELEVISION CHROMA IF AMPLIFIER

... a monolithic device designed to provide the basic control and color signal amplification stages of a solid-state color television receiver. The MC1371 is a combination of two wideband chroma amplifiers and a color control circuit.

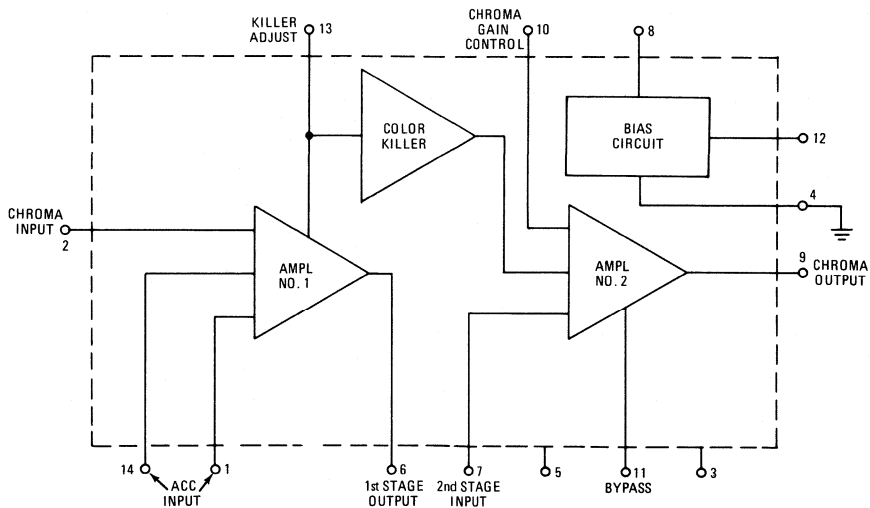
- Schmitt Color-Killer Circuit with Adjustable Trigger Level
- Linear Action dc Manual Gain Control
- Short-Circuit Protected
- Gain Stabilized Against Supply Voltage and Temperature Changes
- Low Phase Distortion
- Excellent Gain Linearity Over Full Output Range
- Direct Replacement for the CA3071

TELEVISION CHROMA IF AMPLIFIER MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646
TO-116

FIGURE 1 - MC1371P SYSTEM BLOCK DIAGRAM



MC1371P (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

| Rating | Value | Unit |
|---|-------------|-------|
| Power Supply Voltage | 30 | Vdc |
| Amplifier Output Short-Circuit Duration | 30 | s |
| Power Dissipation (Package Limitation) | | |
| Plastic Dual In-Line Package | 625 | mW |
| Derate above T _A = +25°C | 5.0 | mW/°C |
| Operating Temperature Range (Ambient) | 0 to +75 | °C |
| Storage Temperature Range | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V_{CC} = +24 Vdc, T_A = +25°C unless otherwise noted. See Test Circuit of Figure 2; switch S1 in position 1, R1 wiper at ground, R2 = 10 kilohms.)

| Characteristic | Min | Typ | Max | Unit |
|---|------|------|------|------|
| Static Characteristics | | | | |
| Quiescent Power Supply Current | 17 | 28 | 31 | mA |
| Short-Circuit Current | | | | mA |
| (pin 6 momentarily grounded) | — | 68 | — | |
| (pin 9 momentarily grounded) | — | 48 | — | |
| First Chroma Stage Input Bias Voltage (pin 2) | — | 1.7 | — | Vdc |
| First Chroma Stage Output Bias Voltage (pin 6) | | | | Vdc |
| ACC Balanced (S1 in position 1) | 13.7 | 16.3 | 20 | |
| ACC Unbalanced (S1 in position 2) | 7.5 | 10.5 | 13.5 | |
| Second Chroma Stage Input Bias Voltage (pin 7) | — | 1.4 | — | Vdc |
| Second Chroma Stage Output Bias Voltage (pin 9) | 16.6 | 17.6 | 18.6 | Vdc |
| Quiescent Bias Voltage (pin 12) | 13.8 | 14.8 | 15.7 | Vdc |

Dynamic Characteristics (f = 3.579545 MHz, input pin 2 = 35 mV [RMS] unless otherwise noted.)

| | | | | |
|--|-------------|----------------------|-------------------|---------|
| First Chroma Amplifier Stage Gain (ACC Balanced) | 14 | 17 | 20 | dB |
| Second Chroma Amplifier Stage Gain (R1 wiper at ground) | 12 | 15.5 | 17 | dB |
| Maximum Linear Output (output level at pin 9) | — | 2.0 | — | V(RMS) |
| Output Voltage, pin 9 (input pin 2 = 50 mV [RMS]) (R1 wiper at V _{CC}) (R1 wiper at ground, R2 adjusted for abrupt ac change in pin 9 output voltage) | — | — | 12 | mV(RMS) |
| | — | — | 12 | |
| Pin 10 Bias Voltage (R1 set for 10% of pin 9 maximum output) (R1 set for 90% of pin 9 maximum output) | 16.7 2.5 | 20.2 3.2 | 21.6 4.5 | Vdc |
| Second Amplifier Gain Stability (V _{CC} + 15%) (V _{CC} - 15%) (T _A = +25°C to +75°C) | — — — | +0.5 -0.5 +0.5 | +1.5 -1.5 — | dB |
| Input Impedance (pin 2) | — | 2.0 | — | kΩ |
| | — | 3.5 | — | pF |
| (pin 7) | — | 2.2 | — | kΩ |
| | — | 3.6 | — | pF |
| Output Impedance (pin 6) (pin 9) | — — | 85 85 | — — | ohms |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

TYPICAL CHARACTERISTICS

($V_{CC} = +24$ Vdc, $f_0 = 3.579545$ MHz, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 2 – TEST CIRCUIT

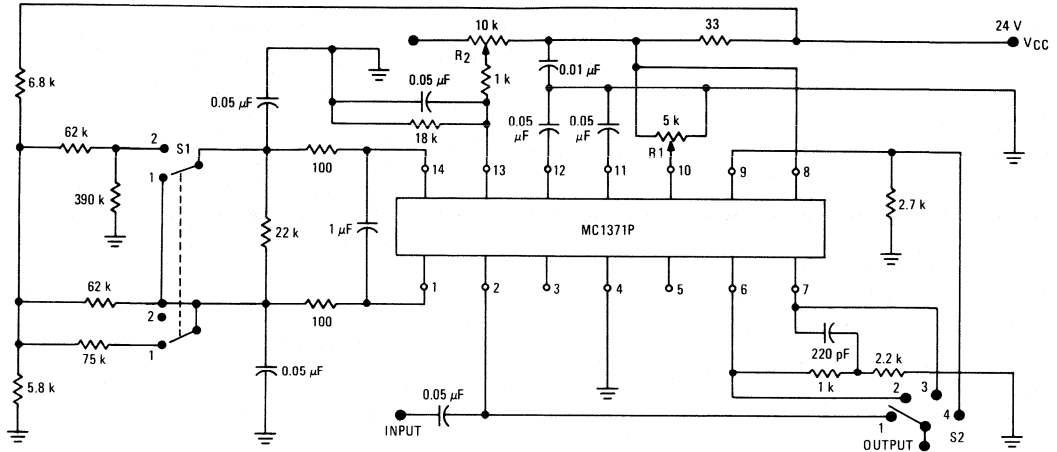


FIGURE 3 – MANUAL GAIN CONTROL LINEARITY

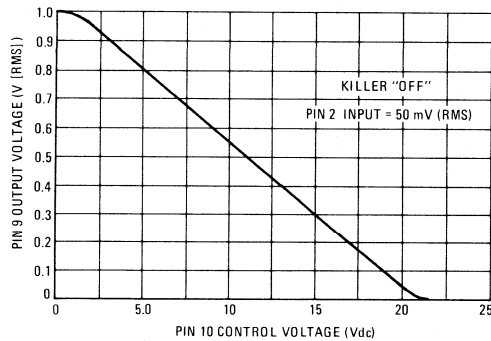


FIGURE 4 – FIRST STAGE GAIN WITH ACC BIAS

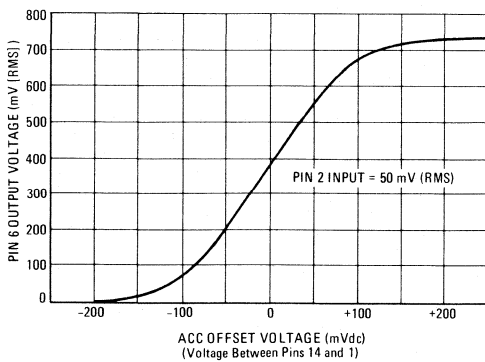


FIGURE 5 – AMPLIFIER LINEARITY

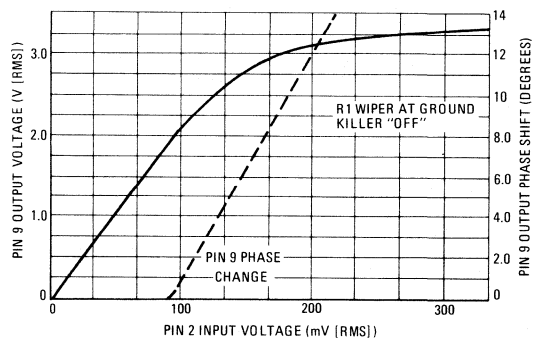
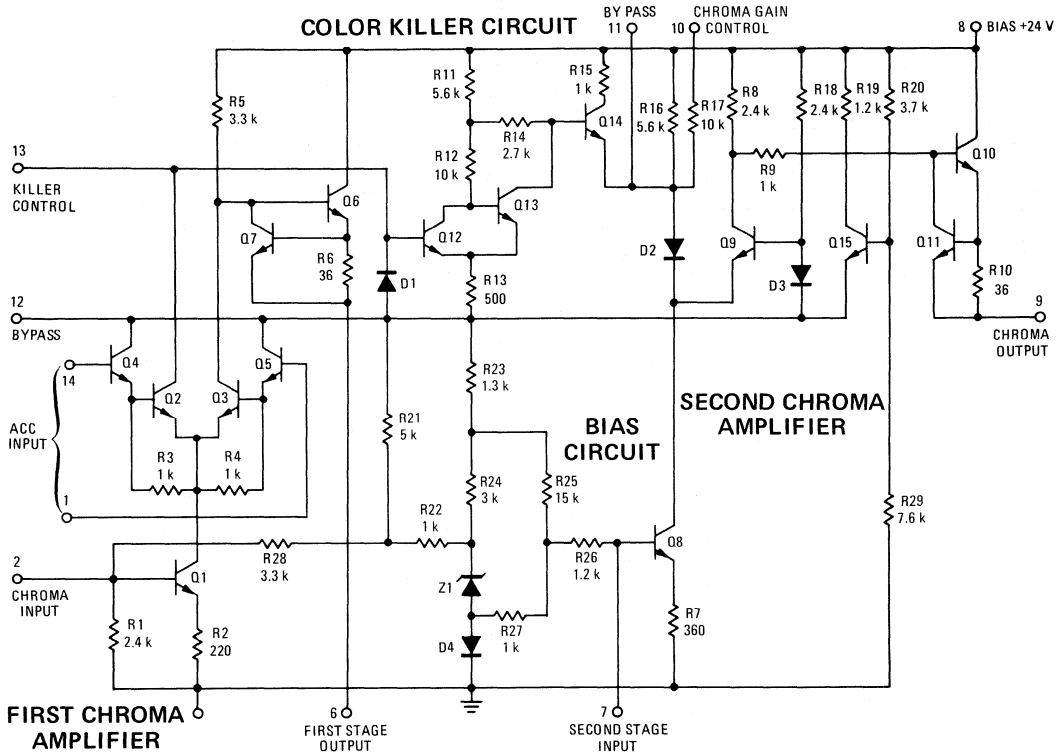


FIGURE 6 - CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1371 is a monolithic wide-band amplifier circuit that functions as the basic control and color signal amplification stages of a color television receiver. The first stage contains the gain control function of the ACC loop and the second stage performs the dc manual gain control function. Also included is a Schmitt trigger circuit providing effective color-killer action during mono-chrome transmissions.

Q1 is a current source modulated by the input signal applied at pin 2. The current in Q1 is divided between the differential pair (Q2 and Q3) in a ratio determined by the ACC voltage applied through the buffer stages, Q4 and Q5. Pin 14 is usually offset with respect to pin 1 by a resistor connected to ground so that at low-signal levels most of the signal current is taken by Q3 and passed to the load resistor R5 (the input stage appears as a cascode amplifier to the signal with the intrinsic ac stability of that configuration). The amplified signal is then buffered at pin 6 by the emitter follower stage Q6 which is protected from accidental grounding at the output by the current limiter Q7.

At strong signals when the amplitude of the burst is high, the ACC voltages at pins 1 and 14 divert most of the signal current from Q3. The signal is "dumped" into the collector load of Q2. Q2 is connected externally at pin 13 and bypassed to ground at signal frequencies by a capacitor. However, the dc voltage at the collector of Q2 is dependent on the burst amplitude and therefore

on the input signal strength. As the input signal level falls, more current is fed into Q3 by the ACC loop and the output at pin 6 remains constant while Q2 collector voltage increases. At a point predetermined by Q2 collector load (the killer-control setting) the input Q12 of the color-killer circuit is biased "on", shutting down the second chroma amplifier stage.

The second chroma stage is similar in configuration to the first stage. The signal input at pin 7 (which is the output from pin 6) modulates the current source Q8. For a maximum gain voltage setting on pin 10 the signal current passes through Q9 to the output buffer stage Q10. Q10 is protected from short circuit currents by Q11. To reduce the stage gain, current is diverted from Q9 by biasing the diode D2 into conduction. D2 can be regarded as a transistor with 100% dc negative feedback applied between collector and base. Without the feedback path the gain characteristic of the second stage is that of a differential pair, this S shaped curve would make tracking of ganged color level and contrast controls quite difficult. In this limiting form the current through D2 is directly proportional to the voltage difference between the supply and D2 anode and hence to the control voltage at pin 10. When the input to the color-killer is biased "on", Q13 is turned "off" and the voltage at the base of Q14 rises abruptly. D2 then takes all the current from Q8 and the output at pin 9 is suppressed.

MC1398P

TV COLOR PROCESSING CIRCUIT

TV COLOR PROCESSING CIRCUIT

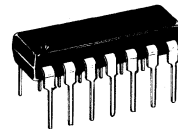
... a chroma IF amplifier with automatic chroma control, color killer, dc chroma control, and injection lock reference system followed by dc hue control.

MC1398P is a monolithic device designed for use in solid-state color television receivers.

- Minimum Number of External Components
- DC Control of Both Chroma Amplitude and Hue Shift
- Crystal-Controlled Internal Feedback Oscillator
- Built-in Noise Immunity
- Schmitt Trigger Color Killer
- Automatic Chroma Control
- Internal Burst Gate and Gate Pulse Shaping Circuit
- High Oscillator Lock-in Sensitivity
- Built-in Supply Regulation

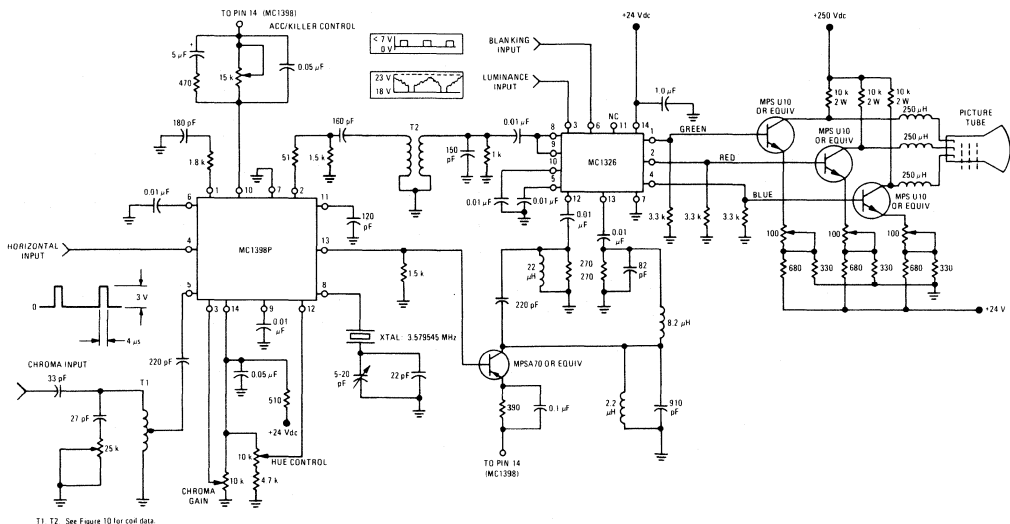
TV COLOR PROCESSING CIRCUIT

MONOLITHIC SILICON
INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646
(TO-116)

FIGURE 1 - TYPICAL CHROMA APPLICATIONS CIRCUIT
(MC1398P, MC1326 and MPSU10)



See Packaging Information Section for outline dimensions.

MC1398P(continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Value | Unit |
|---|-------------|-------------|
| Power Supply Current | 35 | mAdc |
| Horizontal Pulse Input Current | 250 | μA Peak |
| Power Dissipation (package limitation) Derate above T _A = +25°C | 625 5.0 | mW mW/°C |
| Operating Temperature Range (Ambient) | -20 to +75 | °C |
| Storage Temperature Range | -65 to +150 | °C |

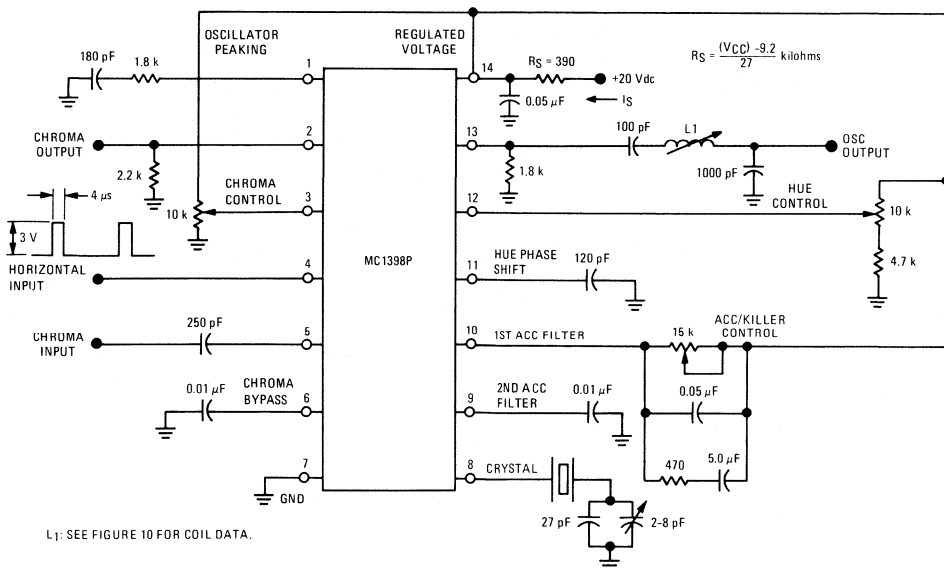
ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, R_S = 390 ohms, T_A = +25°C unless otherwise noted.)

| Characteristic | Min | Typ | Max | Unit |
|--|----------|--------------|-----------|------------|
| Regulated Voltage (I _S = 35 mA) (I _S = 27 mA) | 9.0 — | 9.6 9.2 | 11.5 — | Vdc |
| Maximum Undistorted Chroma Output, See Note 1, E _(pin 3) = E _(pin 14) | 0.8 | 1.75 | — | V(p-p) |
| Maximum Chroma Gain E _(pin 3) = E _(pin 14) . See Note 1 | 34 | 40 | — | dB |
| Automatic Chroma Control Range (ACC) -3.0 dB down from maximum undistorted output, see Note 1 | — | 19 | — | dB |
| Chroma Burst Level to Kill, See Note 1 | — | 1.4 | — | mV(p-p) |
| Manual Chroma Gain Control Range (ΔV _(pin 3) (V _(pin 14) to 0 Vdc) | 50 | 60 | — | dB |
| Chroma Input Resistance | — | 2.3 | — | k ohms |
| Chroma Input Capacitance | — | 13 | — | pF |
| Chroma Output Impedance | — | 15 | — | ohms |
| Horizontal Input Pulse | 2.2 | 3.0 | 4.0 | Vp |
| Oscillator Output | 100 | — | — | mV(RMS) |
| Oscillator Output Impedance | — | 15 | — | ohms |
| Hue Control Range (ΔV _(pin 12) (V _(pin 14) to 4.3 Vdc) | 100 | 126 | — | degrees |
| Oscillator Pull-In Range | 1200 | — | — | Hz |
| Oscillator Noise Bandwidth (f _N) | — | 900 | — | Hz |
| Static Phase Error with Oscillator Detuning 25 mV(p-p) Burst Amplitude 2.0 mV(p-p) Burst Amplitude | — — | 0.20 0.25 | — — | degrees/Hz |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

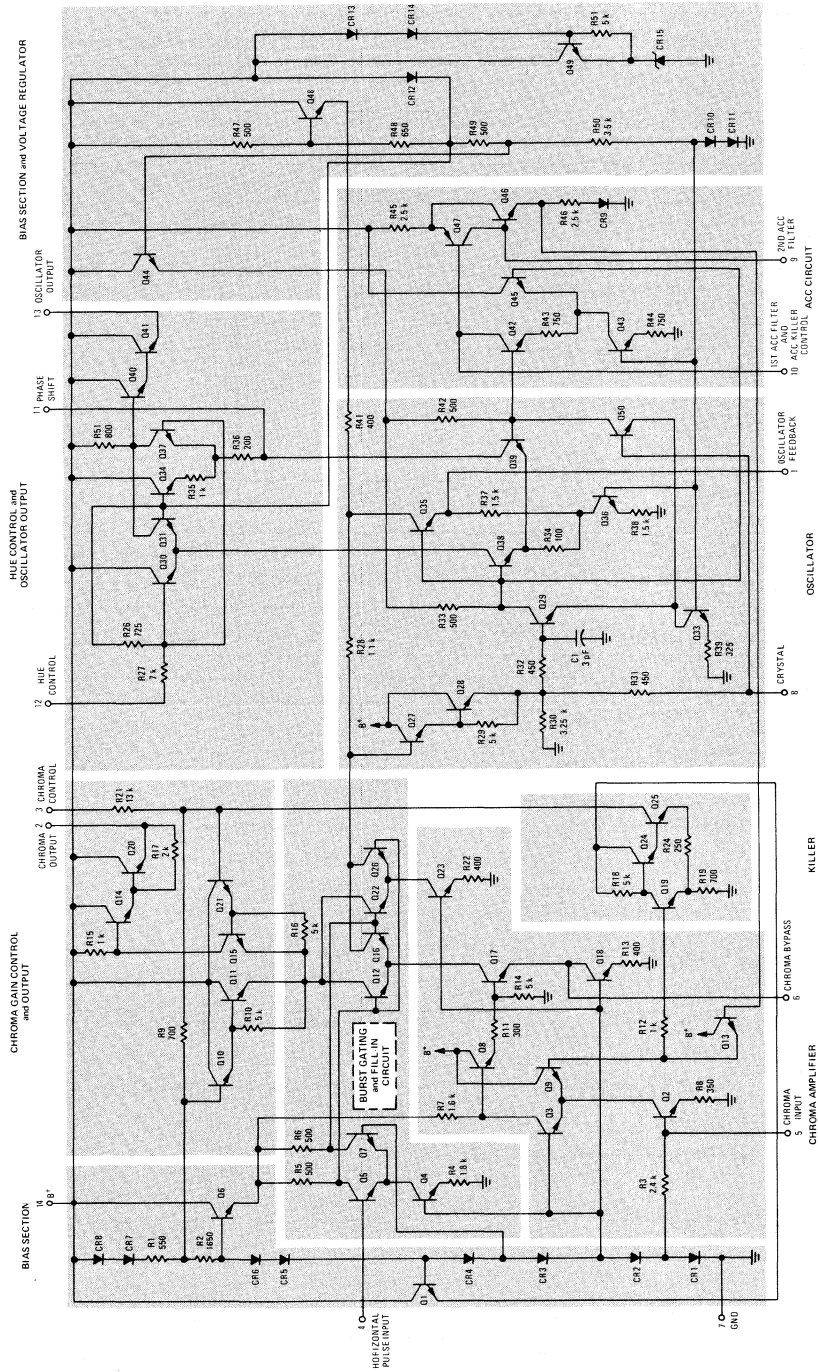
Note 1: With 5.0 mV(p-p) burst input at pin 5
set E_(pin 10) to just "unkill".

FIGURE 2 – MC1398P TEST CIRCUIT



7

FIGURE 3 — MC1398 CIRCUIT SCHEMATIC



7

TYPICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$ unless otherwise noted)

(Figures 4 through 9, See Test Circuit of Figure 2.)

FIGURE 4 – INPUT/OUTPUT CHARACTERISTICS

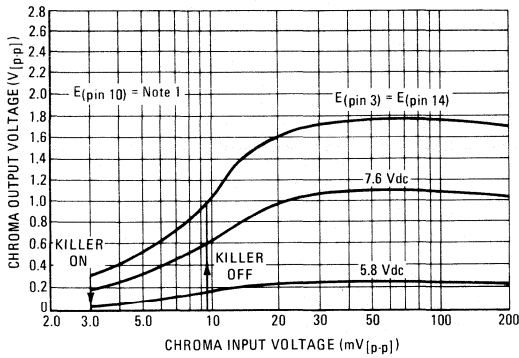


FIGURE 5 – REGULATED VOLTAGE

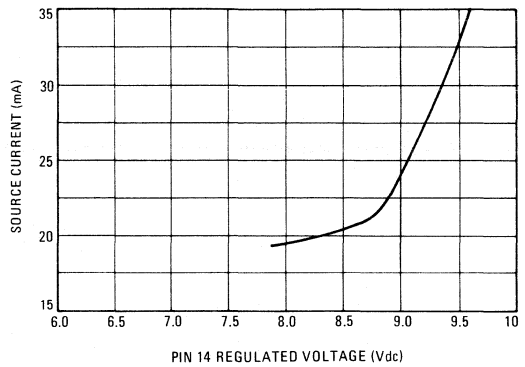


FIGURE 6 – HUE CONTROL OPERATION

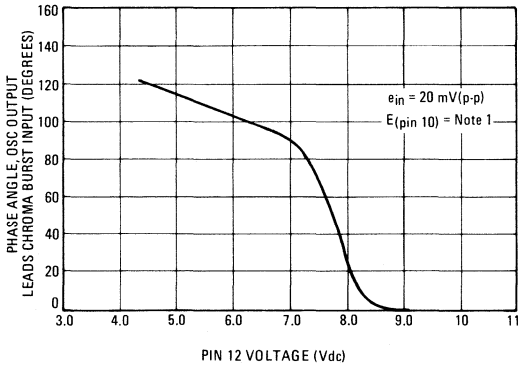


FIGURE 7 – OSCILLATOR OUTPUT versus PIN 12 VOLTAGE

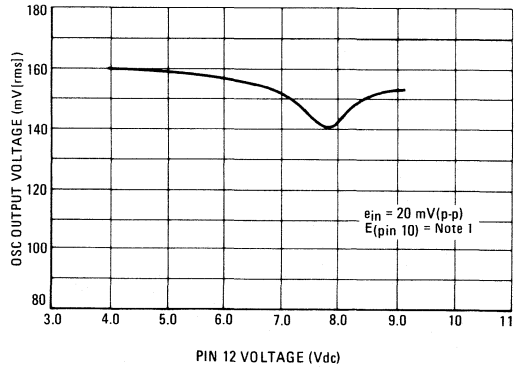


FIGURE 8 – STATIC PHASE ERROR

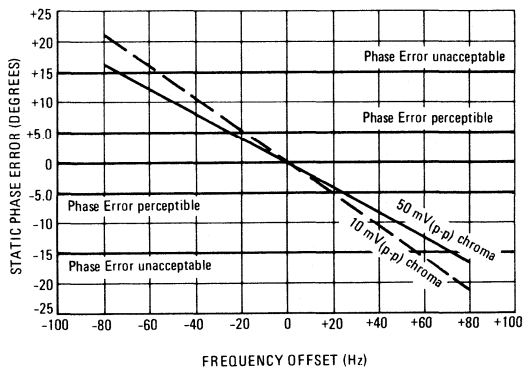


FIGURE 9 – TEMPERATURE STABILITY of the MC1398 OSCILLATOR

(I/C only subjected to temperature change)

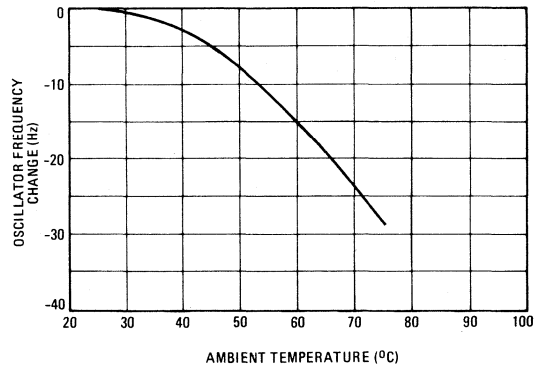
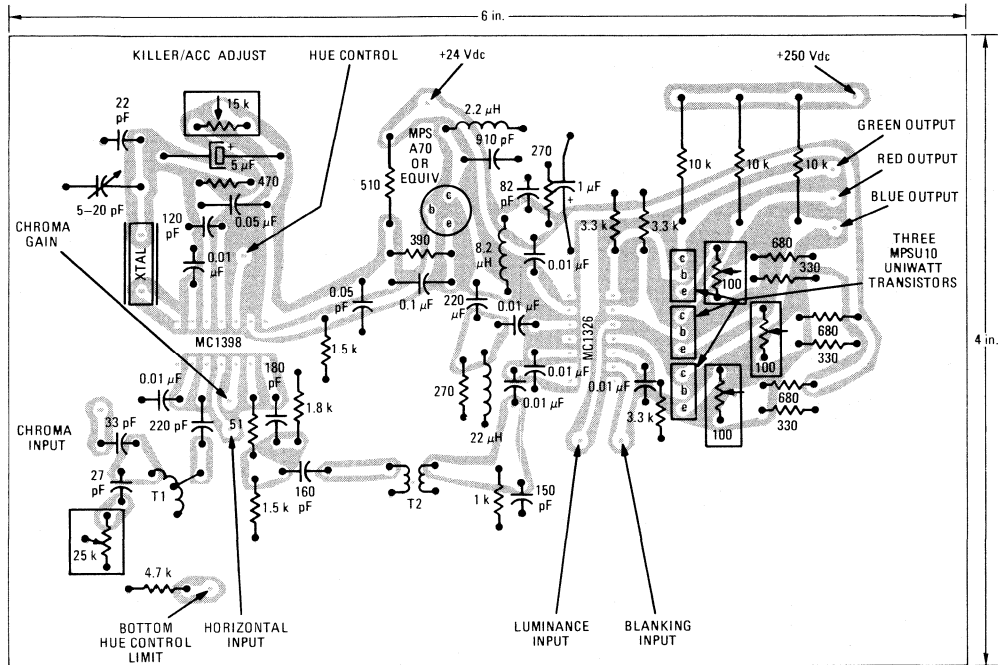
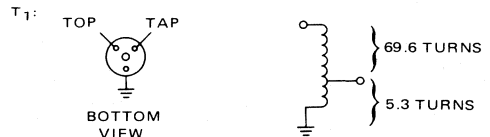
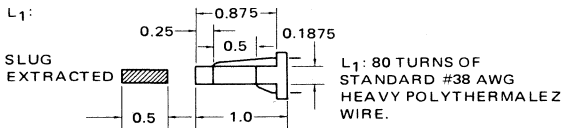


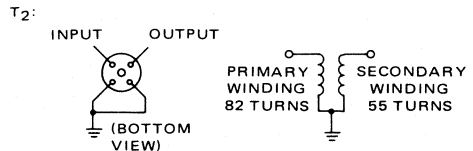
FIGURE 10 – PRINTED CIRCUIT LAYOUT OF MC1398P, MC1326, and MPSU 10 TRANSISTORS



NOTES:
All resistors are 1/4 W unless otherwise noted.
(Copper Side Shown)



COILCRAFT FORM #10-32 OR EQUIV
UNIVERSAL AWG #36 WIRE OR EQUIV
 $L = 26 \mu\text{H}$



COILCRAFT FORM #10-32 OR EQUIV
UNIVERSAL AWG #36 WIRE OR EQUIV
 $L_p = 12 \mu\text{H}$ primary winding
 $L_s = 8.8 \mu\text{H}$ secondary winding
 $K = 0.4$

This coil data is intended as an aid only. It is expected that many designers will want to use other approaches.

MC1398P APPLICATIONS INFORMATION

MC1398P is a multifunction circuit with considerable gain associated with the chroma amplifier and oscillator sections. It is important to the circuit layout utilizing the MC1398P that the chroma amplifier, oscillator, and oscillator output/hue section grounds are separated from each other. Ground loop problems will interfere with oscillation stability and lock-up if this precaution is not observed.

Care must be exercised to avoid coupling from the oscillator output to the crystal circuitry connected to pin 8. Stray coupling of these two points can result in excessive oscillator shift; or in some cases, oscillator drop-out during adjustment of the hue control.

A suitable circuit layout for the MC1398P is shown in Figure 10.

An adjustable capacitor (1.5–20 pF in parallel with a fixed 22 pF capacitor) is shown in series with the 3.58 MHz crystal. This capacitor is used to adjust the oscillator exactly on frequency, and ensures excellent oscillator lock-up. However, acceptable oscillator performance can be obtained with a fixed value of capacitance (this value is dependent on the designers' choice of crystals).

MC1398P (continued)

MC1398P CIRCUIT DESCRIPTION

The MC1398P is capable of providing the entire color processing function between the second detector and the demodulator for television color receivers.

A band pass filter from the second detector provides a 50 mV (p-p) signal (for a saturated color bar pattern) at the input to the first chroma amplifier stage (Q₂, Q₃, Q₈, Q₉). Because of Q₂ emitter load resistor the input impedance is determined primarily by the bias resistor (R₃) and is about 2.3 kilohms. Since Q₂ is the current source for the differential pair (Q₃ and Q₉), the chroma information will pass to the load resistor (R₇) and then to the second chroma amplifier (Q₁₇). To avoid overload of Q₁₇, the maximum gain to Q₁₇ base is only X3 and by varying the bias at the base of Q₉ it is possible to reduce the stage gain by 23 dB without signal distortion; the signal being "dumped" by Q₉ collector into the supply. Since this automatic chroma control action will vary the dc bias at Q₁₇ base the emitter load of Q₁₇ is the current source Q₁₈, maintaining the dc operating current. Q₁₈ collector is bypassed externally to prevent ac signal attenuation.

During picture scan time, the chroma signal passes through the output level control amplifier (Q₁₀, Q₁₁, Q₁₅, Q₂₁). By changing the bias on Q₁₁ and Q₁₅ bases the signal can either pass to the output pin 2 or be "dumped" into the supply through Q₁₁. The use of buffer stages Q₁₀ and Q₂₁ prevent distortion at low-signal levels and the control range is better than 70 dB. The signal output is also buffered by Q₁₄ and Q₂₀, thus providing a low impedance drive of up to 2.0 V (p-p) to the demodulator, with an overall gain between pins 5 and 2 of 40 dB. To enable the chroma signal output to reach the amplifiers from Q₁₇ collector, Q₁₂ is held in conduction by Q₅ which in the absence of any input on pin 4 is not conducting. This high collector voltage also holds Q₂₆ in conduction, clamping the input to the burst channel and preventing chroma information reaching the oscillator. During picture retrace time, a positive-going 4.0 μs pulse from the line sweep transformer will turn Q₅ "on" and Q₇ "off". When Q₅ collector goes low, Q₁₂ will become "cut-off" preventing the burst signal at Q₁₇ collector from reaching the output pin 2. At the same time, Q₂₆ turns "off" opening the burst channel. The high collector voltage of Q₇ turns on Q₁₆ and Q₂₂. Q₁₆ passes the burst signal from Q₁₇ collector to the subcarrier regenerator and Q₂₂ "fills-in" for Q₁₂ during the gate period to prevent a dc shift in the pin 2 output voltage.

The gated burst signal is applied to the oscillator through Q₂₇ and Q₂₈. Q₂₉, Q₅₀ and Q₃₅ together with Q₂₇ and Q₂₈ form an injection locked oscillator circuit. At series resonance of the crystal connected to pin 8 the impedance of pin 8 is very low, thereby reducing the 3.579545 MHz carrier level at the base of Q₅₀. The signal at the base of Q₂₉ is not reduced but the output voltages in R₃₃ and R₄₂ will change. Any signals outside the

response band of the crystal will appear equally at Q₅₀ and Q₂₉ bases and be suppressed in the output by the differential amplifier common-mode rejection ratio (about 40 dB). To maintain oscillation, a feedback signal with the correct phase is passed by Q₃₅ back to the input of Q₂₇. Careful control of the resistor ratios ensures that Q₂₉ and Q₅₀ are operated linearly with about 350 mV (p-p) at R₃₃ and R₄₂, due to self oscillation. A burst signal as low as 2.0 mV (p-p) at the chroma input is sufficient to cause the oscillator to lock to the reference phase and frequency.

As the burst amplitude increases, the level at Q₂₉ and Q₅₀ collectors changes and this shift is used to provide the automatic chroma control function. Q₄₂ and Q₄₅ form a modified differential amplifier and with zero offset bias Q₄₅ conducts most of the current from Q₄₃. As an increasing burst level swings Q₂₉ and Q₅₀ collectors, the current from Q₄₃ is shunted into Q₄₂. At a point predetermined by the setting of the automatic chroma control connected to pin 10, the composite lateral PNP of Q₄₇ and Q₄₆ will be biased into conduction. This amplifier has a gain of unity and a filter capacitor (connected to Q₄₆ base) prevents any tendency to oscillations. Diode CR₉ provides thermal compensation to ensure a steady color-killer threshold point. The increasing current through Q₁₃ emitter is used to control Q₉ base, attenuating the input signal as the burst amplitude increases. The current from Q₁₃ also keeps Q₁₉ in saturation. When the input signal becomes too small for satisfactory color rendition, Q₁₃ current falls and Q₁₉ comes out of saturation. This means Q₂₅ will saturate, clamping Q₂₁ base and "killing" the chroma output stage. R₂₄ in the Schmitt trigger circuit ensures that the color-killer will have hysteresis to prevent fluttering between "on" and "off" states.

The oscillator output voltages at R₃₃ and R₄₂ are used to drive Q₃₈ and Q₃₉ into limiting so that as the burst amplitude increases the oscillator activity to around 700 mV (p-p), there will be no change in the oscillator output amplitude at pin 13. Q₃₈ and Q₃₉ are used as current sources with a 180° phase difference for the differential pairs Q₃₀ and Q₃₁, Q₃₄ and Q₃₇. A small capacitor attached externally to Q₃₉ collector adjusts the total phase difference to 135°. Since the signal appearing in the load resistor R₅₁ will be the vector sum of Q₃₁ and Q₃₇ signals, varying the base bias of Q₃₀ and Q₃₄ will change the oscillator output phase over the 135° range. Q₄₀ and Q₄₁ buffer the oscillator output providing a low impedance drive at pin 13 for the demodulator.

To minimize crosstalk between the burst and chroma channels, separate bias chains are used. Further, the oscillator bias chain is zener regulated to prevent phase shifts in the reference output with power-supply variations.

MC1414L

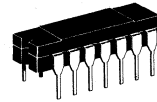
DUAL DIFFERENTIAL COMPARATOR

MONOLITHIC DUAL DIFFERENTIAL VOLTAGE COMPARATOR

... designed for use in level detection, low-level sensing, and memory applications.

Typical Amplifier Features:

- Two Separate Outputs
- Strobe Capability
- High Output Sink Current – 1.6 mA min Each Comparator
- Differential Input Characteristics:
Input Offset Voltage = 1.5 mV
Offset Voltage Drift = 5.0 $\mu\text{V}/^\circ\text{C}$
- Short Propagation Delay Time – 40 ns
- Output Compatible with All Saturating Logic Forms
 $V_{\text{out}} = +3.2 \text{ V to } -0.5 \text{ V typical}$

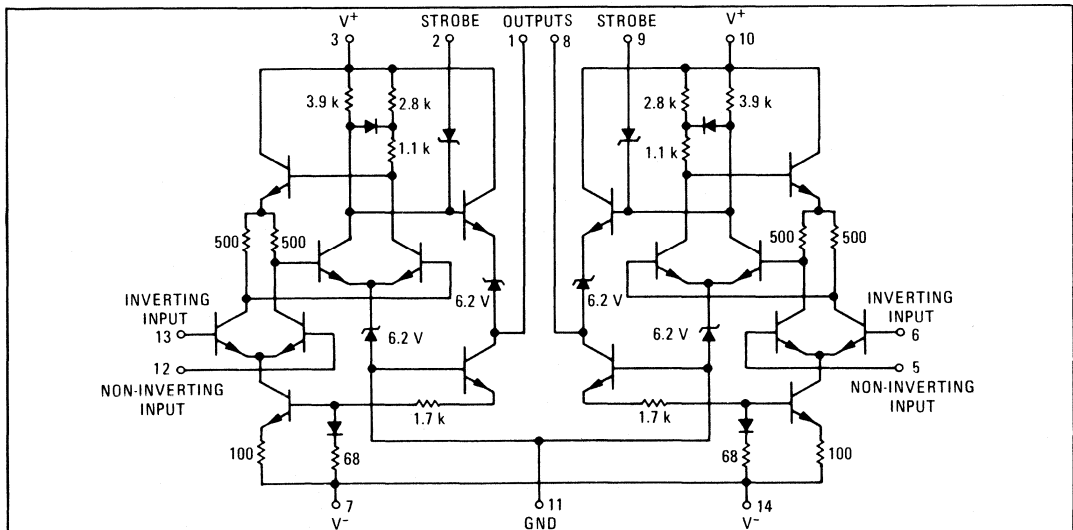


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|--------------------------|-------------|----------------------------------|
| Power Supply Voltage | V^+ V^- | +14 -7.0 | Vdc Vdc |
| Differential Input Signal | V_{in} | ± 5.0 | Volts |
| Common Mode Input Swing | CMV_{in} | ± 7.0 | Volts |
| Peak Load Current | I_L | 10 | mA |
| Power Dissipation (package limitation) Ceramic Dual In-Line Package Derate above $T_A = 50^\circ\text{C}$ | P_D | 750 6.0 | mW $\text{mW}/^\circ\text{C}$ |
| Operating Temperature Range | T_A | 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

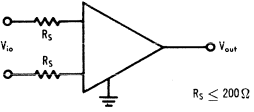
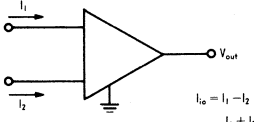
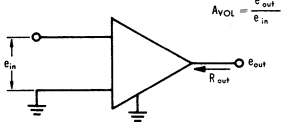
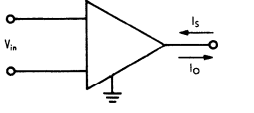
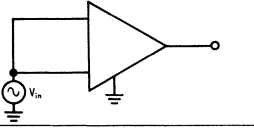
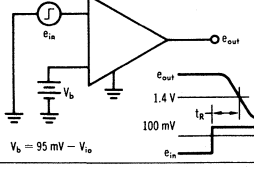
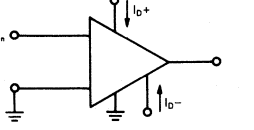
CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MC1414L (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +1.2$ Vdc, $V^- = -6$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted) (Each Comparator)

| Characteristic Definitions (linear operation) | Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|------------------------|-----------|------|-----|------------------------------|
|  | Input Offset Voltage $V_{out} = 1.4$ Vdc, $T_A = 25^\circ\text{C}$ $V_{out} = 1.8$ Vdc, $T_A = 0^\circ\text{C}$ $V_{out} = 1.0$ Vdc, $T_A = +75^\circ\text{C}$ | V_{io} | - | 1.5 | 5.0 | mVdc |
| | Temperature Coefficient of Input Offset Voltage | $TC_{V_{io}}$ | - | 5.0 | - | $\mu\text{V}/^\circ\text{C}$ |
|  | Input Offset Current $V_{out} = 1.4$ Vdc, $T_A = 25^\circ\text{C}$ $V_{out} = 1.8$ Vdc, $T_A = 0^\circ\text{C}$ $V_{out} = 1.0$ Vdc, $T_A = +75^\circ\text{C}$ | I_{io} | - | 1.0 | 5.0 | μA dc |
| | Input Bias Current $V_{out} = 1.4$ Vdc, $T_A = 25^\circ\text{C}$ $V_{out} = 1.8$ Vdc, $T_A = 0^\circ\text{C}$ $V_{out} = 1.0$ Vdc, $T_A = +75^\circ\text{C}$ | I_b | - | 15 | 25 | μA dc |
|  | Open Loop Voltage Gain $T_A = 25^\circ\text{C}$ $T_A = 0$ to $+75^\circ\text{C}$ | A_{VOL} | 1000 | 1500 | - | V/V |
| | Output Resistance | R_{out} | - | 200 | - | ohms |
|  | Differential Voltage Range | V_{in} | ± 5.0 | - | - | Vdc |
| | Positive Output Voltage $V_{in} \cong 5.0$ mV, $0 \leq I_o \leq 5.0$ mA | V_{OH} | 2.5 | 3.2 | 4.0 | Vdc |
| | Negative Output Voltage $V_{in} \cong -5.0$ mV | V_{OL} | -1.0 | -0.5 | 0 | Vdc |
| | Output Sink Current $V_{in} \cong -5.0$ mV, $V_{out} \cong 0$, $T_A = 0$ to $+75^\circ\text{C}$ | I_s | 1.6 | 2.5 | - | mA |
|  | Input Common Mode Range $V^- = -7.0$ Vdc | CMV_{in} | ± 5.0 | - | - | Volts |
| | Common Mode Rejection Ratio $V^- = -7.0$ Vdc, $R_S \leq 200 \Omega$ | CM_{rej} | 70 | 100 | - | dB |
|  | Propagation Delay Time For Positive and Negative Going Input Pulse | t_{pd} | - | 40 | - | ns |
|  | Total Power Supply Current $V_{out} \leq 0$ Vdc | I_{D^+} I_{D^-} | - | 12.8 | 18 | mA |
| | Total Power Consumption | | - | 230 | 300 | mW |

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

(Each Comparator)

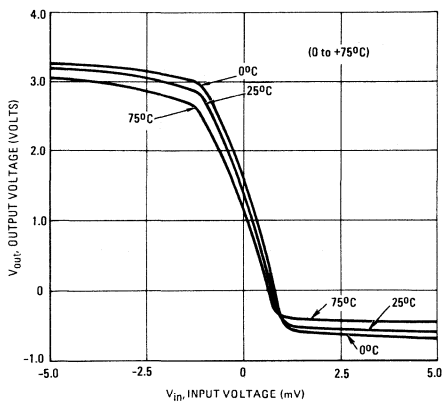


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

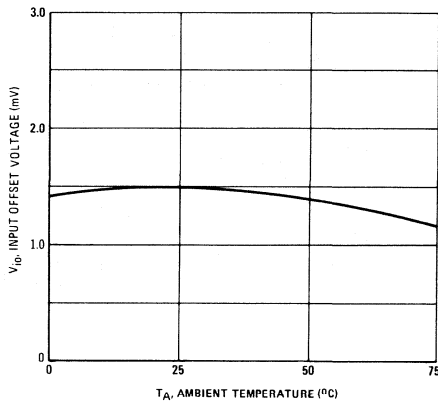


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

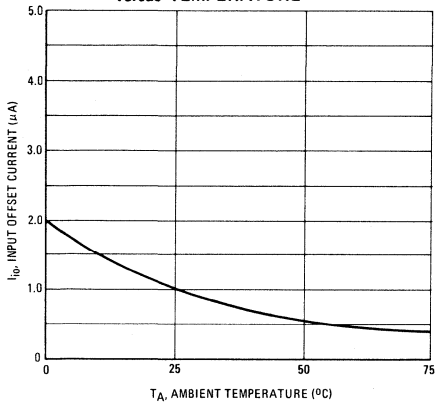


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE

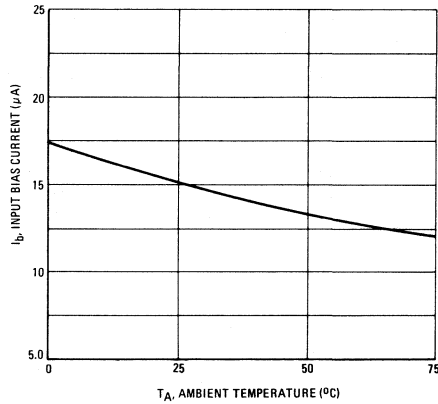


FIGURE 5 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

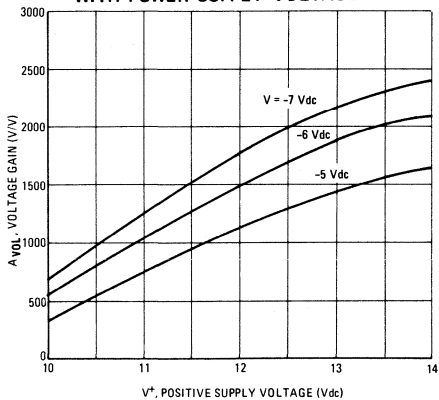
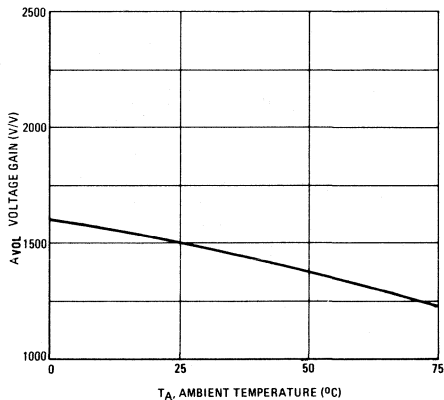


FIGURE 6 – VOLTAGE GAIN versus TEMPERATURE



MC1414L (continued)

FIGURE 7 – RESPONSE TIME

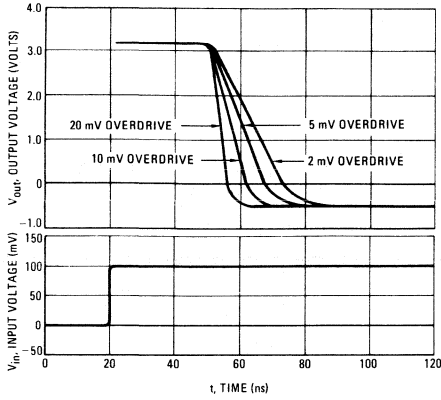


FIGURE 8 – POWER DISSIPATION versus TEMPERATURE

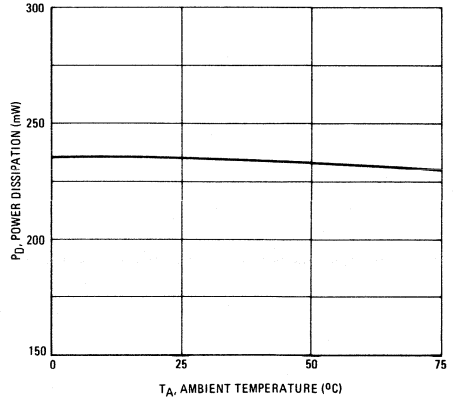


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

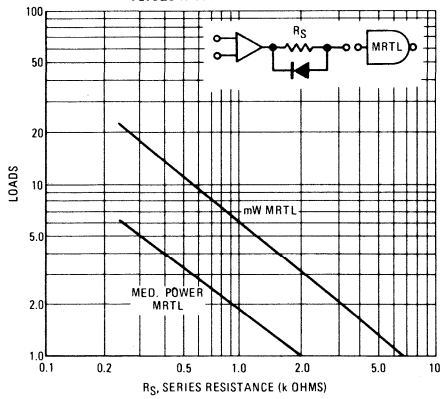


FIGURE 10 – SINK CURRENT versus TEMPERATURE

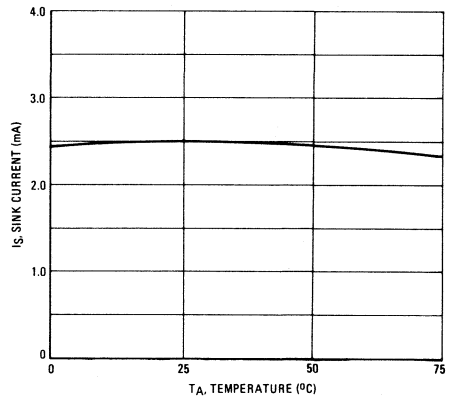
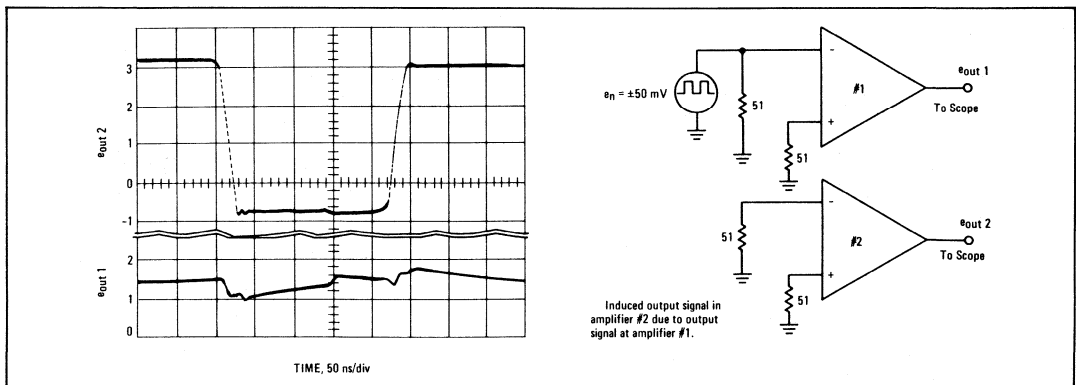


FIGURE 11 – CROSSTALK†



†Worst case condition shown – no load.

MC1488L

QUAD LINE DRIVER

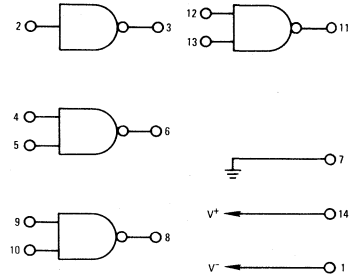
The MC1488L is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

Features:

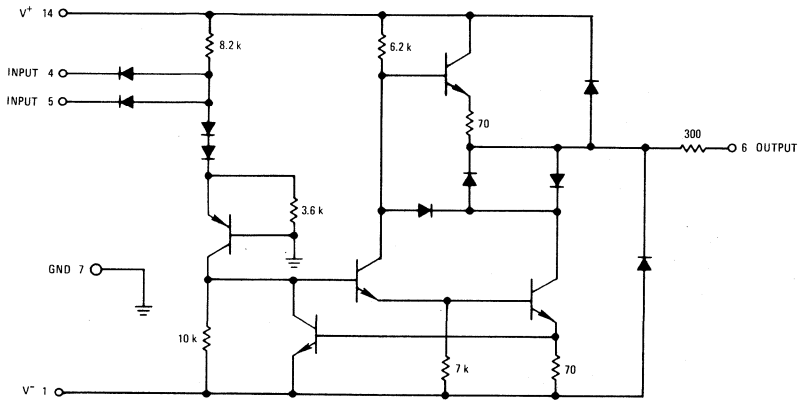
- Current Limited Output
10 mA typ
- Power-Off Source Impedance
300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola DTL and TTL Logic Families

QUAD MDTL LINE DRIVER RS-232C INTEGRATED CIRCUIT

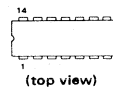
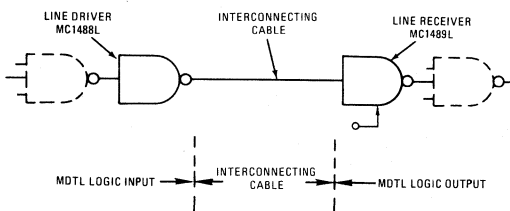
LOGIC DIAGRAM



CIRCUIT SCHEMATIC 1/4 OF CIRCUIT SHOWN



TYPICAL APPLICATION



CERAMIC PACKAGE
CASE 632
TO-116

See Packaging Information Section for outline dimensions.

MC1488L (continued)

Maximum Rating ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|--------------------------|----------------------------|----------------------------|
| Power Supply Voltage | V^+ V^- | +15 -15 | Vdc |
| Input Signal Voltage | V_{in} | $-15 \leq V_{in} \leq 7.0$ | Vdc |
| Output Signal Voltage | V_o | ± 15 | Vdc |
| Power Derating (Package Limitation, Ceramic Dual-In-Line Package) Derate above $T_A = +25^\circ\text{C}$ | P_D $1/\theta_{JA}$ | 1000 6.7 | mW mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +175 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS ($V^+ = +9.0 \pm 1\% \text{ Vdc}$, $V^- = -9.0 \pm 1\% \text{ Vdc}$, $T_A = 0$ to $+75^\circ\text{C}$ unless otherwise noted)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|--|--------|-----------|----------------------------|--------------------------------------|--|---------------|
| Forward Input Current ($V_{in} = 0 \text{ Vdc}$) | 1 | I_F | — | 1.0 | 1.6 | mA |
| Reverse Input Current ($V_{in} = +5.0 \text{ Vdc}$) | 1 | I_R | — | — | 10 | μA |
| Output Voltage High ($V_{in} = 0.8 \text{ Vdc}$, $R_L = 3.0 \text{ k}\Omega$, $V^+ = +9.0 \text{ Vdc}$, $V^- = -9.0 \text{ Vdc}$) ($V_{in} = 0.8 \text{ Vdc}$, $R_L = 3.0 \text{ k}\Omega$, $V^+ = +13.2 \text{ Vdc}$, $V^- = -13.2 \text{ Vdc}$) | 2 | V_{OH} | +6.0 +9.0 | +7.0 +10.5 | — — | Vdc |
| Output Voltage Low ($V_{in} = 1.9 \text{ Vdc}$, $R_L = 3.0 \text{ k}\Omega$, $V^+ = +9.0 \text{ Vdc}$, $V^- = -9.0 \text{ Vdc}$) ($V_{in} = 1.9 \text{ Vdc}$, $R_L = 3.0 \text{ k}\Omega$, $V^+ = +13.2 \text{ Vdc}$, $V^- = -13.2 \text{ Vdc}$) | 2 | V_{OL} | -6.0 -9.0 | -7.0 -10.5 | — — | Vdc |
| Positive Output Short-Circuit Current | 3 | I_{SC+} | +6.0 | +10 | +12 | mA |
| Negative Output Short-Circuit Current | 3 | I_{SC-} | -6.0 | -10 | -12 | mA |
| Output Resistance ($V^+ = V^- = 0$, $ V_o = \pm 2.0 \text{ V}$) | 4 | R_o | 300 | — | — | Ohms |
| Positive Supply Current ($R_L = \infty$) ($V_{in} = 1.9 \text{ Vdc}$, $V^+ = +9.0 \text{ Vdc}$) ($V_{in} = 0.8 \text{ Vdc}$, $V^+ = +9.0 \text{ Vdc}$) ($V_{in} = 1.9 \text{ Vdc}$, $V^+ = +12 \text{ Vdc}$) ($V_{in} = 0.8 \text{ Vdc}$, $V^+ = +12 \text{ Vdc}$) ($V_{in} = 1.9 \text{ Vdc}$, $V^+ = +15 \text{ Vdc}$) ($V_{in} = 0.8 \text{ Vdc}$, $V^+ = +15 \text{ Vdc}$) | 5 | I^+ | — — — — — — | +15 +4.5 +19 +5.5 — — | +20 +6.0 +25 +7.0 +34 +12 | mA |
| Negative Supply Current ($R_L = \infty$) ($V_{in} = 1.9 \text{ Vdc}$, $V^- = -9.0 \text{ Vdc}$) ($V_{in} = 0.8 \text{ Vdc}$, $V^- = -9.0 \text{ Vdc}$) ($V_{in} = 1.9 \text{ Vdc}$, $V^- = -12 \text{ Vdc}$) ($V_{in} = 0.8 \text{ Vdc}$, $V^- = -12 \text{ Vdc}$) ($V_{in} = 1.9 \text{ Vdc}$, $V^- = -15 \text{ Vdc}$) ($V_{in} = 0.8 \text{ Vdc}$, $V^- = -15 \text{ Vdc}$) | 5 | I^- | — — — — — — | -13 0 -18 0 — — | -17 0 -23 0 -34 -2.5 | mA |
| Power Dissipation ($V^+ = 9.0 \text{ Vdc}$, $V^- = -9.0 \text{ Vdc}$) ($V^+ = 12 \text{ Vdc}$, $V^- = -12 \text{ Vdc}$) | | P_D | — — | — — | 333 576 | mW |

SWITCHING CHARACTERISTICS ($V^+ = +9.0 \pm 1\% \text{ Vdc}$, $V^- = -9.0 \pm 1\% \text{ Vdc}$, $T_A = +25^\circ\text{C}$)

| | | | | | | |
|--|---|------------|---|-----|-----|----|
| Propagation Delay Time ($Z_L = 3.0 \text{ k}$ and 15 pF) | 6 | t_{pd}^+ | — | 150 | 200 | ns |
| Fall Time ($Z_L = 3.0 \text{ k}$ and 15 pF) | 6 | t_f | — | 45 | 75 | ns |
| Propagation Delay Time ($Z_L = 3.0 \text{ k}$ and 15 pF) | 6 | t_{pd}^- | — | 65 | 120 | ns |
| Rise Time ($Z_L = 3.0 \text{ k}$ and 15 pF) | 6 | t_r | — | 55 | 100 | ns |

CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

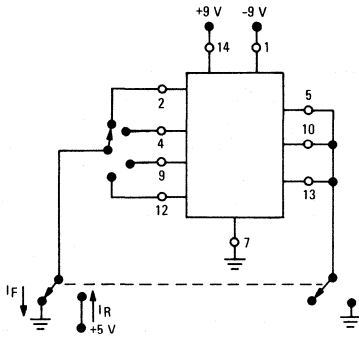


FIGURE 2 – OUTPUT VOLTAGE

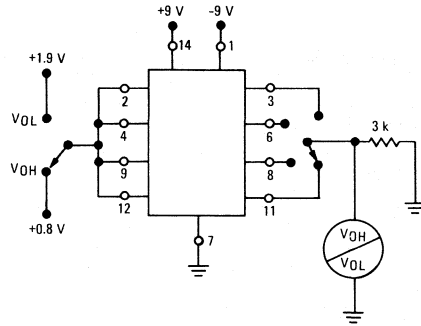


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

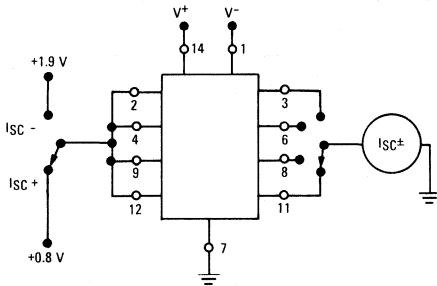


FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

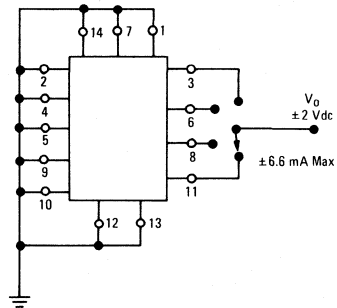


FIGURE 5 – POWER-SUPPLY CURRENTS

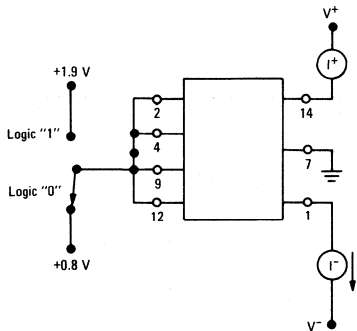
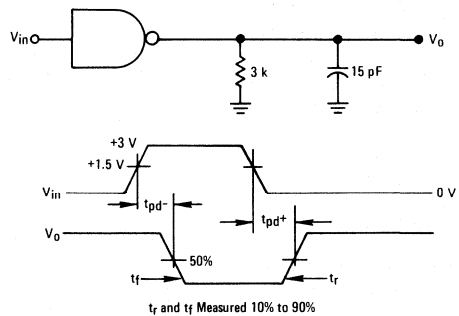


FIGURE 6 – SWITCHING RESPONSE



t_r and t_f Measured 10% to 90%

TYPICAL CHARACTERISTICS
($T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 7 – TRANSFER CHARACTERISTICS
versus POWER-SUPPLY VOLTAGE

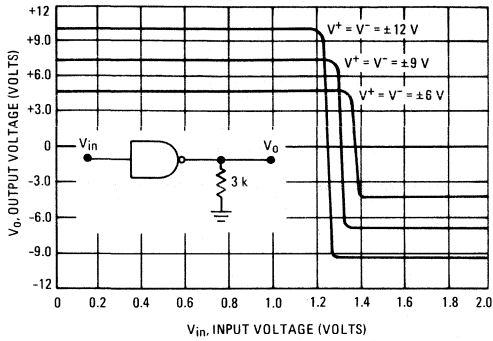


FIGURE 8 – SHORT-CIRCUIT OUTPUT CURRENT
versus TEMPERATURE

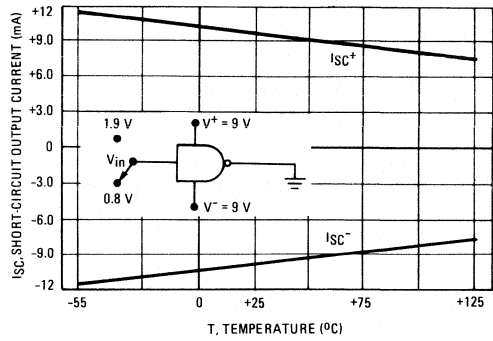


FIGURE 9 – OUTPUT SLEW RATE versus LOAD CAPACITANCE

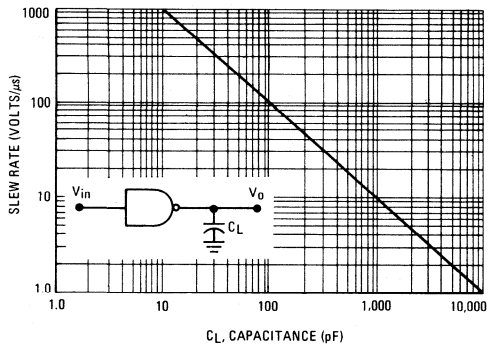


FIGURE 10 – OUTPUT VOLTAGE
AND CURRENT-LIMITING CHARACTERISTICS

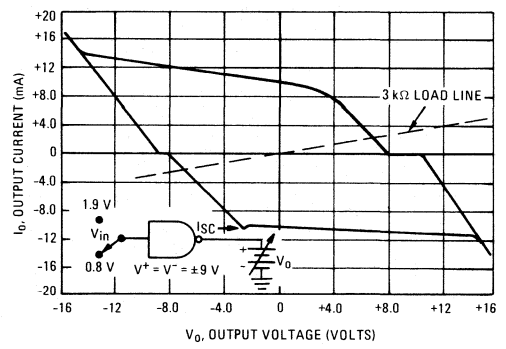
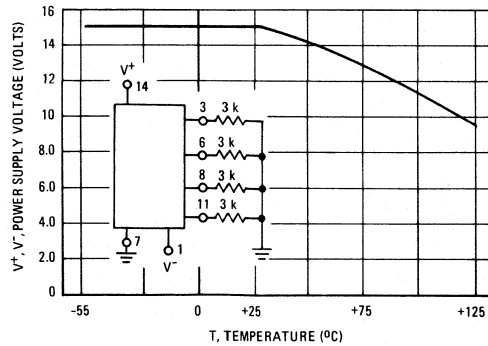


FIGURE 11 – MAXIMUM OPERATING TEMPERATURE
versus POWER-SUPPLY VOLTAGE



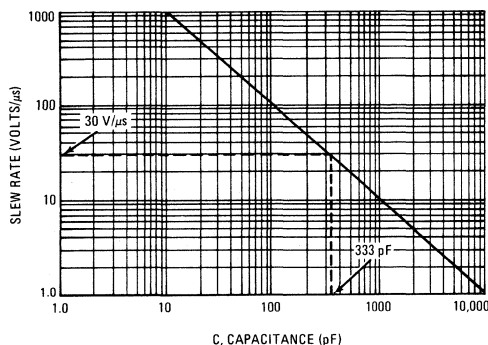
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488L quad driver and its companion circuit, the MC1489L quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15 volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488L meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488L is much too

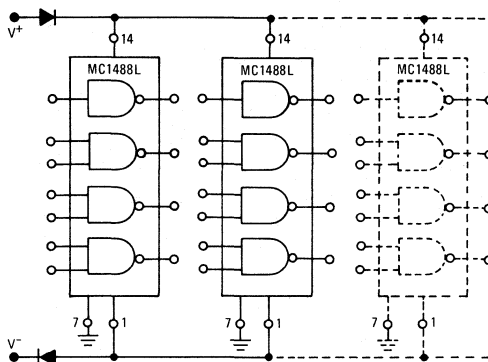
FIGURE 12 — SLEW RATE versus CAPACITANCE FOR $I_{SC} = 10 \text{ mA}$



fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{SC} \times \Delta T / \Delta V$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 volt, 500 mA source. The MC1488L is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V^+ \geq 9.0 \text{ V}$; $V^- \leq -9.0 \text{ V}$). In some power-supply designs, a loss of system power causes a low impedance to ground would exist at the power inputs to the MC1488L effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors

FIGURE 13 — POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488L to withstand momentary shorts to the ± 25 -volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488L to withstand faults with power-supplies of less than the 9.0 volts stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488L is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting — this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488L used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.
2. Power-Supply Range — as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488L will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

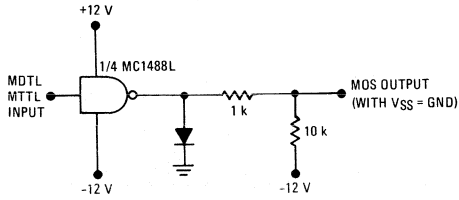
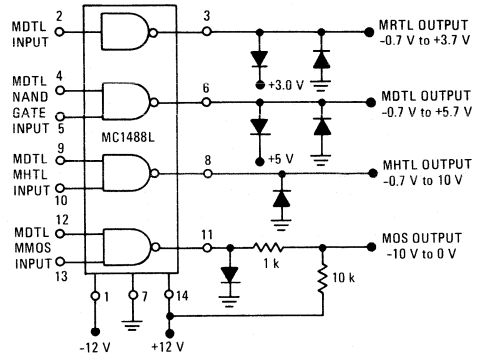


FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS



LINEAR/DIGITAL INTERFACE CIRCUITS

MC1489L MC1489AL

QUAD LINE RECEIVERS

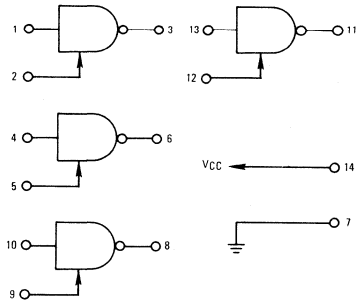
The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

- Input Resistance — 3.0 k to 7.0 kilohms
- Input Signal Range — ± 30 Volts
- Input Threshold Hysteresis Built In
- Response Control
 - a) Logic Threshold Shifting
 - b) Input Noise Filtering

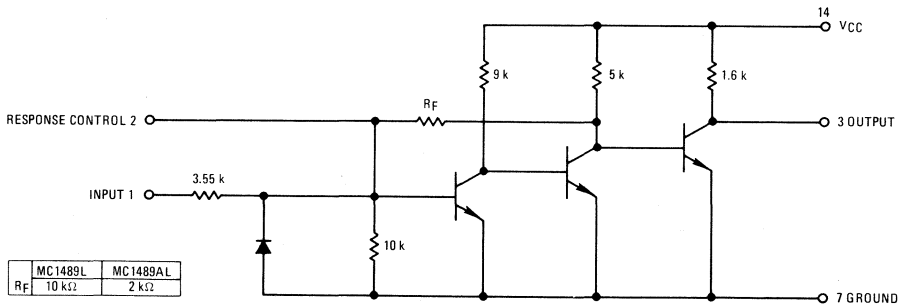
QUAD MDTL LINE RECEIVERS RS-232C

INTEGRATED CIRCUIT

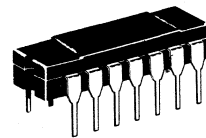
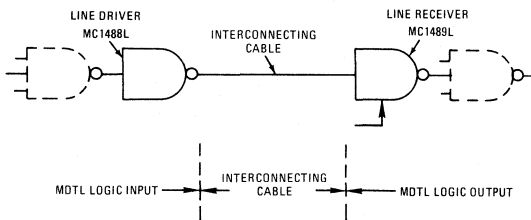
LOGIC DIAGRAM



CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



TYPICAL APPLICATION



CERAMIC PACKAGE
CASE 632
TO-116

See Packaging Information Section for outline dimensions.

MC1489L, MC1489AL (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|-------------------------------------|-------------|-----------------|
| Power Supply Voltage | V _{CC} | 10 | V _{dc} |
| Input Signal Range | V _{in} | ±30 | V _{dc} |
| Output Load Current | I _L | 20 | mA |
| Power Dissipation (Package Limitation, Ceramic Dual In-Line Package) Derate above T _A = +25°C | P _D 1/θ _{JA} | 1000 6.7 | mW mW/°C |
| Operating Temperature Range | T _A | 0 to +75 | °C |
| Storage Temperature Range | T _{stg} | -65 to +175 | °C |

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = +5.0 Vdc ±1%, T_A = 0 to +75°C unless otherwise noted)

| Characteristics | Figure | Symbol | Min | Typ | Max | Unit |
|---|--------|-----------------|---------------|------------|--------------|-----------------|
| Positive Input Current (V _{in} = +25 Vdc) (V _{in} = +3.0 Vdc) | 1 | I _{IH} | 3.6 0.43 | — | 8.3 — | mA |
| Negative Input Current (V _{in} = -25 Vdc) (V _{in} = -3.0 Vdc) | 1 | I _{IL} | -3.6 -0.43 | — | -8.3 — | mA |
| Input Turn-On Threshold Voltage (T _A = +25°C, V _{OL} ≤ 0.45 V) | 2 | V _{IH} | 1.0 1.75 | — 1.95 | 1.5 2.25 | V _{dc} |
| Input Turn-Off Threshold Voltage (T _A = +25°C, V _{OH} ≥ 2.5 V, I _L = -0.5 mA) | 2 | V _{IL} | 0.75 0.75 | — 0.8 | 1.25 1.25 | V _{dc} |
| Output Voltage High (V _{in} = 0.75 V, I _L = -0.5 mA) (Input Open Circuit, I _L = -0.5 mA) | 2 | V _{OH} | 2.6 2.6 | 4.0 4.0 | 5.0 5.0 | V _{dc} |
| Output Voltage Low (V _{in} = 3.0 V, I _L = 10 mA) | 2 | V _{OL} | — | 0.2 | 0.45 | V _{dc} |
| Output Short-Circuit Current | 3 | I _{SC} | — | 3.0 | — | mA |
| Power Supply Current (V _{in} = +5.0 Vdc) | 4 | I ⁺ | — | 20 | 26 | mA |
| Power Dissipation (V _{in} = +5.0 Vdc) | 4 | P _D | — | 100 | 130 | mW |

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 1%, T_A = +25°C)

| | | | | | | |
|---|---|------------------|---|-----|-----|----|
| Propagation Delay Time (R _L = 3.9 kΩ) | 5 | t _{PLH} | — | 25 | 85 | ns |
| Rise Time (R _L = 3.9 kΩ) | 5 | t _r | — | 120 | 175 | ns |
| Propagation Delay Time (R _L = 390 Ω) | 5 | t _{PHL} | — | 25 | 50 | ns |
| Fall Time (R _L = 390 Ω) | 5 | t _f | — | 10 | 20 | ns |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

TEST CIRCUITS

FIGURE 1 – INPUT CURRENT

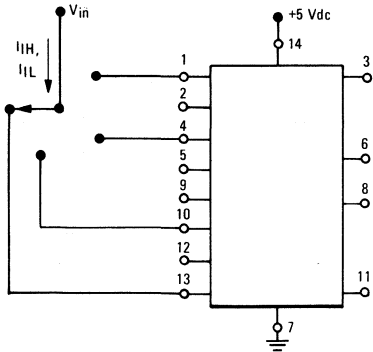


FIGURE 2 – OUTPUT VOLTAGE and INPUT THRESHOLD VOLTAGE

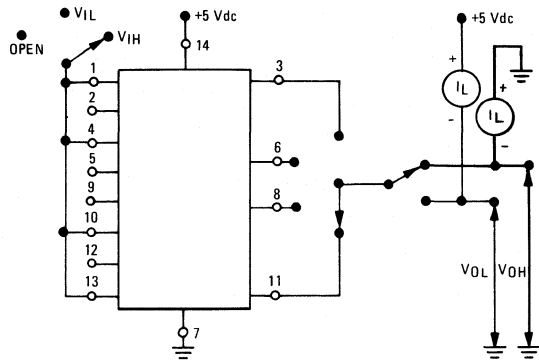


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

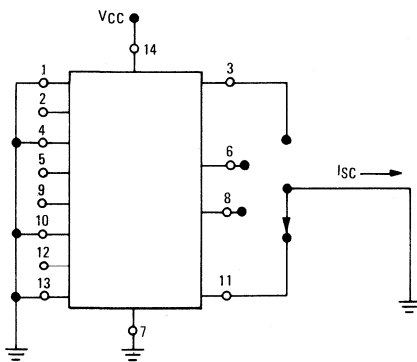


FIGURE 4 – POWER-SUPPLY CURRENT

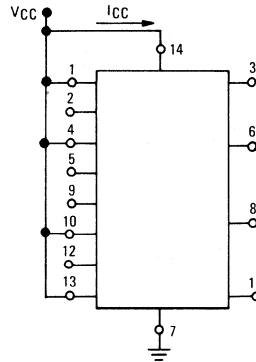


FIGURE 5 – SWITCHING RESPONSE

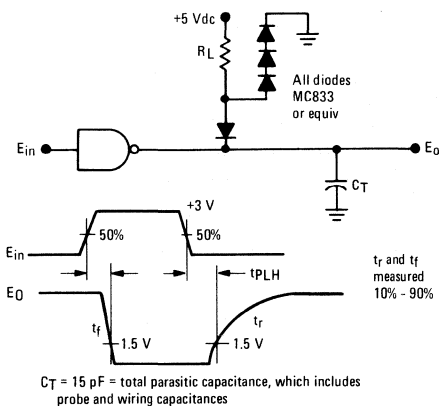
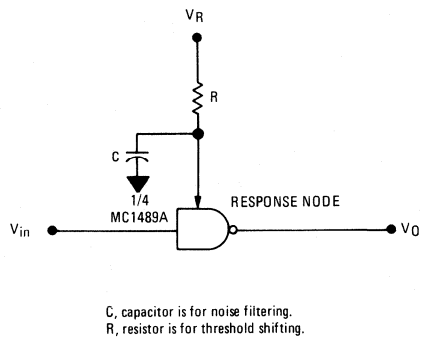


FIGURE 6 – RESPONSE CONTROL NODE



MC1489L, MC1489AL (continued)

TYPICAL CHARACTERISTICS

($V_{CC} = 5.0 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 7 – INPUT CURRENT

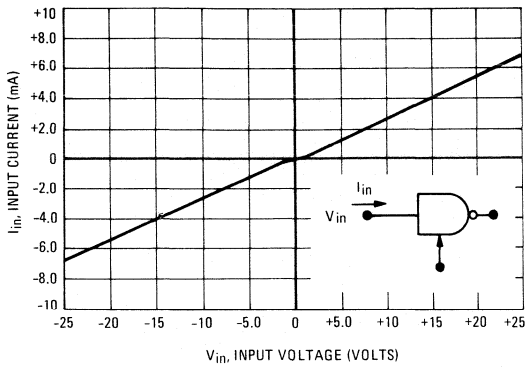


FIGURE 8 – MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

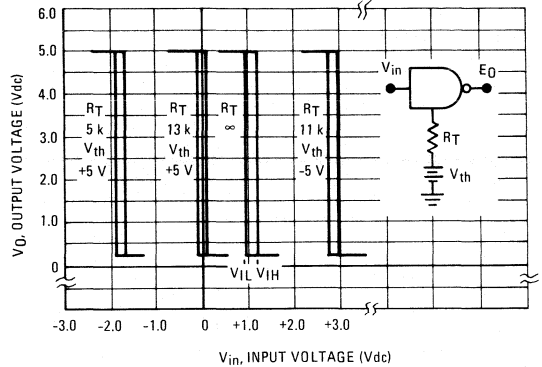


FIGURE 9 – MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

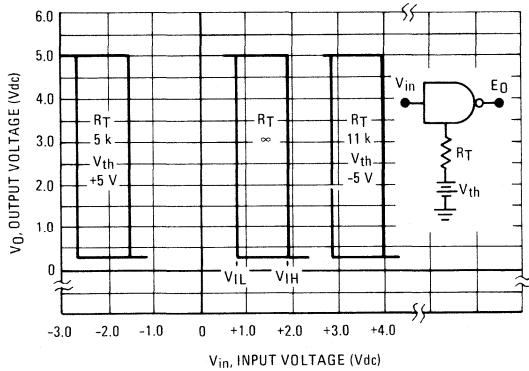


FIGURE 10 – INPUT THRESHOLD VOLTAGE versus TEMPERATURE

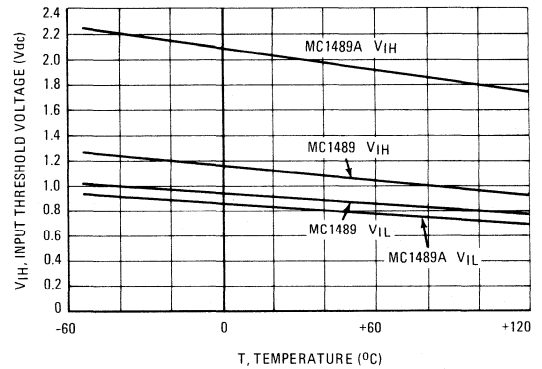
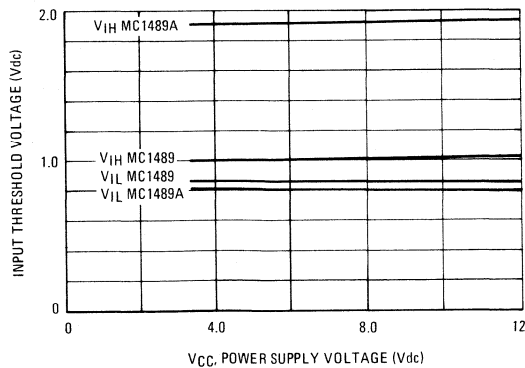


FIGURE 11 – INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488L quad driver and its companion circuit, the MC1489L quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE} (Ref. Sect. 2.4).

The receiver shall detect a voltage between -3.0 and -25 volts as a logic "1" and inputs between +3.0 and +25 volts as a logic "0" (Ref. Sect. 2.3). On some interchange leads, an open circuit or power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or logic "1" (Ref. Sect. 2.5). For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise

rejection. The MC1489L input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489AL has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 6, 8 and 9 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 12 and 13 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 14)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 15 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

FIGURE 12 – TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

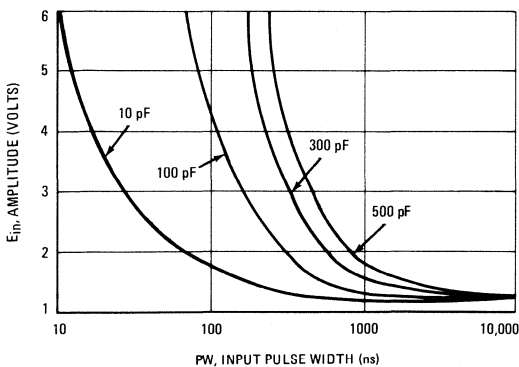
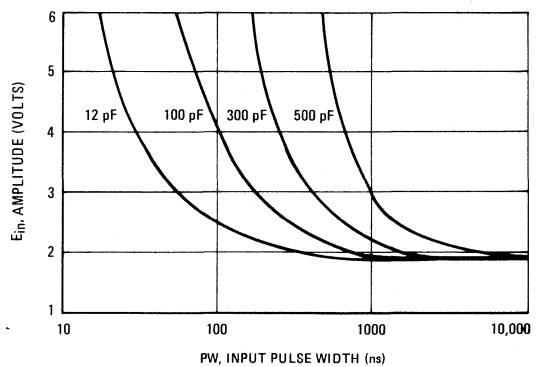


FIGURE 13 – TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



MC1489L, MC1489AL (continued)

APPLICATIONS INFORMATION (continued)

FIGURE 14 – TYPICAL TRANSLATOR APPLICATION – MOS TO DTL OR TTL

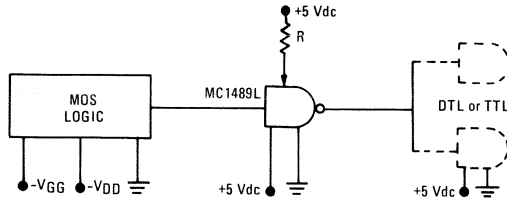
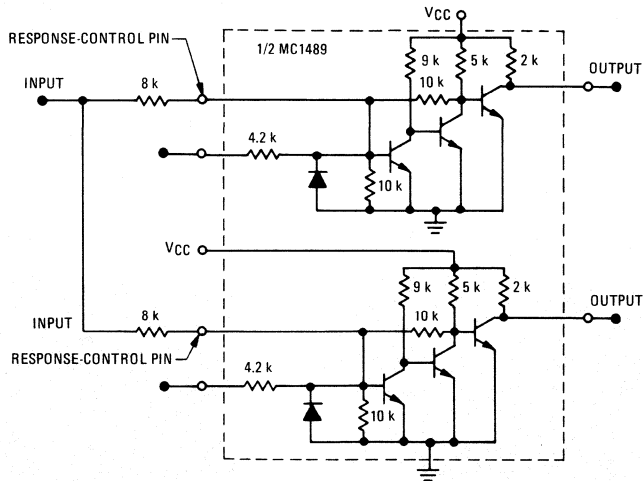


FIGURE 15 – TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C



**MC1506L
MC1406L**

**Specifications and Applications
Information**

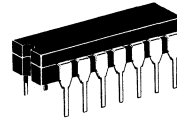
**MONOLITHIC SIX BIT, MULTIPLYING
DIGITAL-TO-ANALOG CONVERTER**

... designed for use where the output current is a linear product of a six-bit digital word and an analog input voltage.

- Digital Inputs are MDTL and MTTL Compatible
- Relative Accuracy – $\pm 0.78\%$ Error maximum
- Low Power Dissipation – 85 mW typical @ ± 5.0 V
- Adjustable Output Current Scaling
- Fast Settling Time – 150 ns typical
- Standard Supply Voltage: +5.0 V and -5.0 V to -15 V

**SIX BIT, MULTIPLYING
DIGITAL-TO-ANALOG
CONVERTER**

MONOLITHIC
SILICON INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 632
TO-116

**FIGURE 1 – OUTPUT CURRENT SETTLING TIME
(ALL BITS SWITCHED, $R_L = 50 \Omega$)**

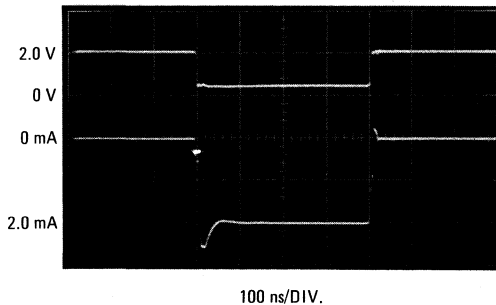
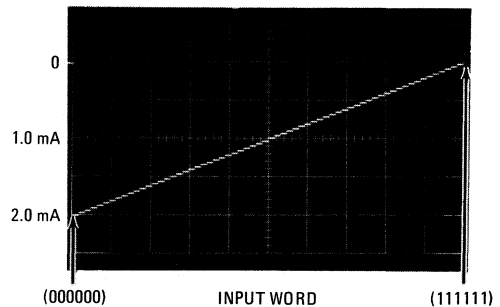


FIGURE 2 – D-to-A TRANSFER CHARACTERISTICS



TYPICAL APPLICATIONS

- | | |
|---|--|
| <ul style="list-style-type: none"> • Tracking A-to-D Converters • Successive Approximation A-to-D Converters • Digital-to-Analog Meter Readout • Sample and Hold • Peak Detector • Programmable Gain and Attenuation • Digital Varicap Tuning • Video Systems | <ul style="list-style-type: none"> • Stepping Motor Drive • CRT Character Generation • Digital Addition and Subtraction • Analog-Digital Multiplication • Digital-Digital Multiplication • Analog-Digital Division • Programmable Power Supplies • Speech Encoding |
|---|--|

See Packaging Information Section for outline dimensions.

7

MC1506L, MC1406L (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|--|-------------------------------------|-----------------------------------|-------------|
| Power Supply Voltage | V _{CC} V _{EE} | +5.5 -16.5 | Vdc |
| Digital Input Voltage | V ₅ thru V ₁₀ | +8.0, V _{EE} | Vdc |
| Applied Output Voltage | V _O | ±5.0 | Vdc |
| Reference Current | I ₁₂ | 5.0 | mA |
| Reference Amplifier Inputs | V ₁₂ , V ₁₃ | V _{CC} , V _{EE} | Vdc |
| Power Dissipation (Package Limitation) Ceramic Package Derate above T _A = +25°C | P _D | 1000 6.7 | mW mW/°C |
| Operating Temperature Range MC1506L MC1406L | T _A | -55 to +125 0 to +75 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R_{12}} = 2.0$ mA, T_A = T_{low}* to T_{high}* unless otherwise noted. All digital inputs at low logic levels.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|---------|--|---------------|--------------|-----------------|--------|
| Relative Accuracy (Error relative to full scale I _O) | 10 | E _r | — | — | ±0.78 | % |
| Settling Time (within 1/2 LSB [includes t _d] T _A = +25°C) | 9 | t _S | — | 150 | 300 | ns |
| Propagation Delay Time T _A = +25°C | 9 | t _{PHL} , t _{PLH} | — | 10 | 50 | ns |
| Output Full Scale Current Drift | | TCI _O | — | 80 | — | PPM/°C |
| Digital Input Logic Levels High Level, Logic "1" (MC1406L, MC1506L) Low Level, Logic "0" (MC1406L) (MC1506L) | 3,14 | V _{IH} V _{IL} | 2.0 — — | — — — | — 0.8 0.5 | Vdc |
| Digital Input Current High Level, V _{IH} = 5.0 V Low Level, V _{IL} = 0.8 V | 3,13 | I _{IH} I _{IL} | — — | 0 -0.7 | +0.01 -1.5 | mA |
| Reference Input Bias Current (Pin 13) | 3 | I ₁₃ | — | -0.002 | -0.01 | mA |
| Output Current Range V _{EE} = -5.0 V V _{EE} = -6.0 to -15 V | 3 | I _{OR} | 0 0 | 2.0 2.0 | 2.1 4.2 | mA |
| Output Current V _{ref} = 2.000 V, R ₁₂ = 1.000 kΩ | 3 | I _O | 1.9 | 1.97 | 2.1 | mA |
| Output Current (all bits high) | 3 | I _{O(min)} | — | 0 | 10 | μA |
| Output Voltage Compliance (E _r ≤ ±0.78% at T _A = +25°C) | 3,4,5 | V _O | — | — | ±0.4 | Vdc |
| Reference Current Slew Rate (T _A = +25°C) | 8,15 | SR I _{ref} | — | 2.0 | — | mA/μs |
| Output Current Power Supply Sensitivity | 10 | PSRR (-) | — | 0.002 | 0.010 | mA/V |
| Power Supply Current A1 thru A6; V _{IL} = 0.8 V A1 thru A6; V _{IH} = 2.0 V | 3,11,12 | I _{CC} I _{EE} | — — | +7.2 -9.0 | +11 -11 | mA |
| Power Dissipation (all bits high) V _{EE} = -5.0 Vdc V _{EE} = -15 Vdc | | P _D | — — | 85 175 | 120 240 | mW |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

*T_{high} = +75°C for MC1406L T_{low} = 0°C for MC1406L
 = +125°C for MC1506L = -55°C for MC1506L

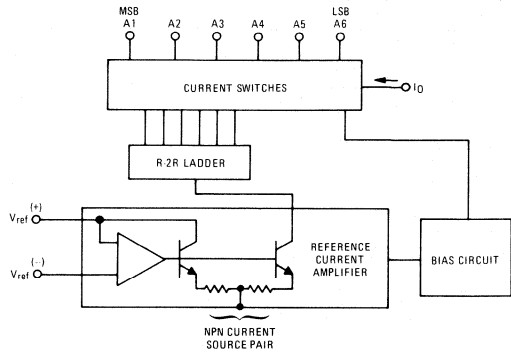
MC1506L, MC1406L (continued)

The MC1506L consists of a reference current amplifier, and R-2R ladder, and six high-speed current switches. For many applications, only a reference resistor and a reference supply voltage need be added.

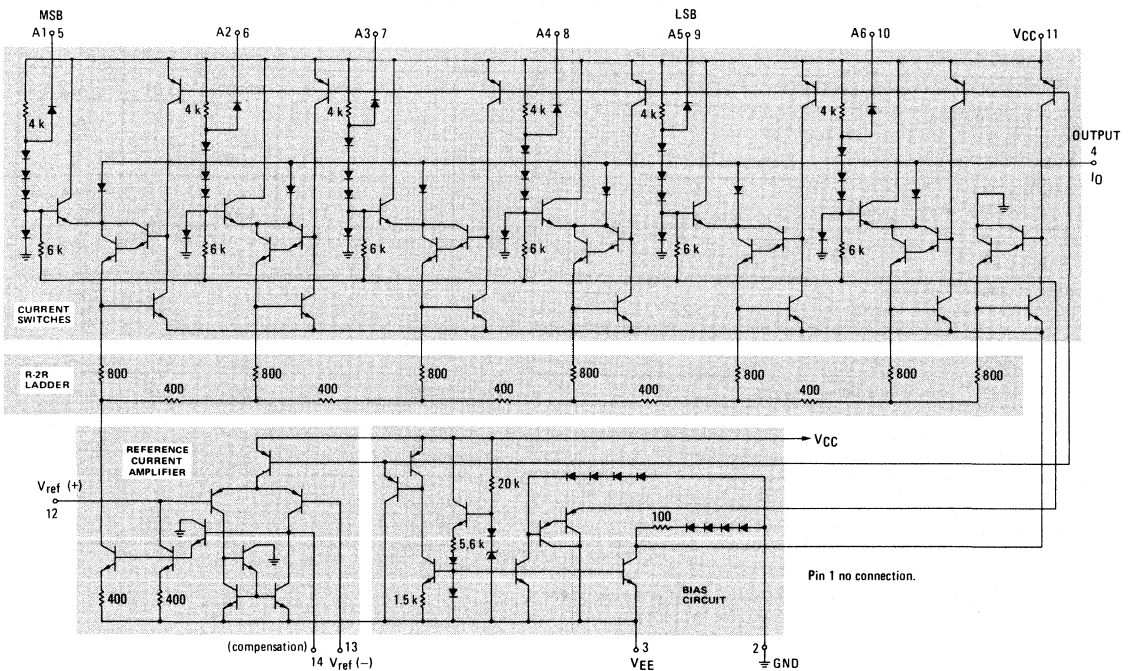
The switches are inverting in operation, therefore a low state at the input turns on the specified output current component. The switches use a current steering technique for high speed and a termination amplifier that consists of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binary-related components which are fed to the switches. Note that there is always a remainder current that is equal to the least significant bit. This current is shunted to ground, and the maximum current is 63/64 of the reference amplifier current, or 1.969 mA for a 2.0 mA reference current if the NPN current source pair is perfectly matched.

BLOCK DIAGRAM



COMPLETE CIRCUIT SCHEMATIC (Digital Inputs; pins 5,6,7,8,9,10)



TEST CIRCUITS AND TYPICAL CHARACTERISTICS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT

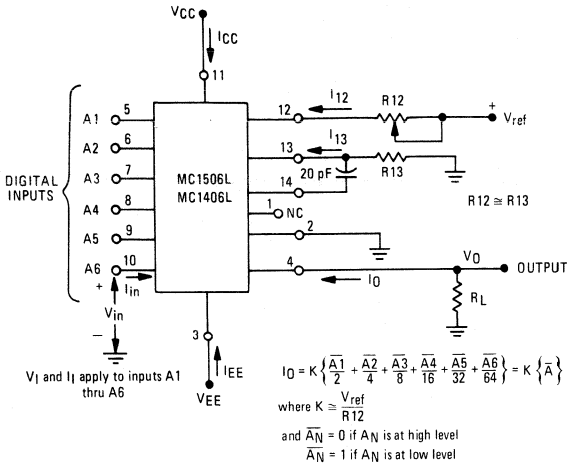


FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE

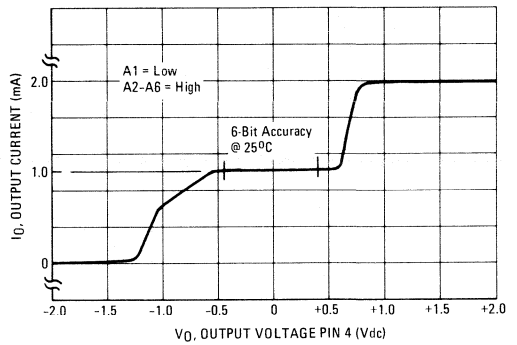


FIGURE 5 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE

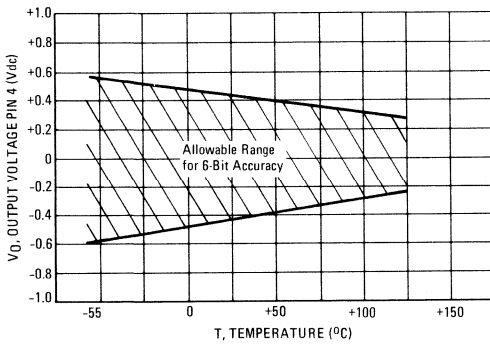


FIGURE 6 – POSITIVE V_{ref}

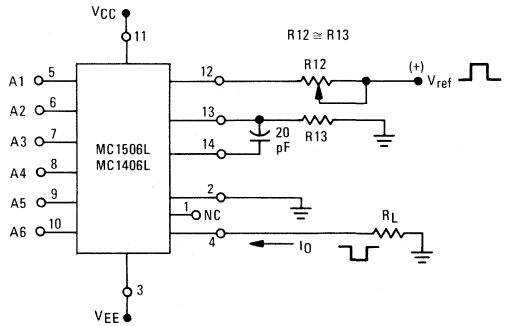


FIGURE 7 – NEGATIVE V_{ref}

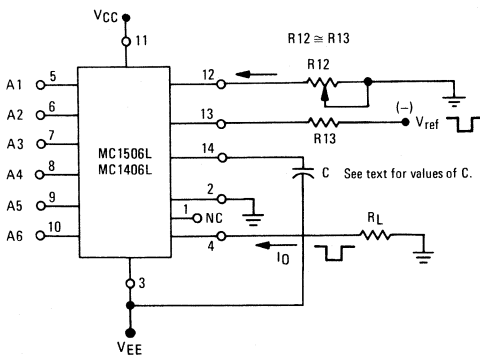
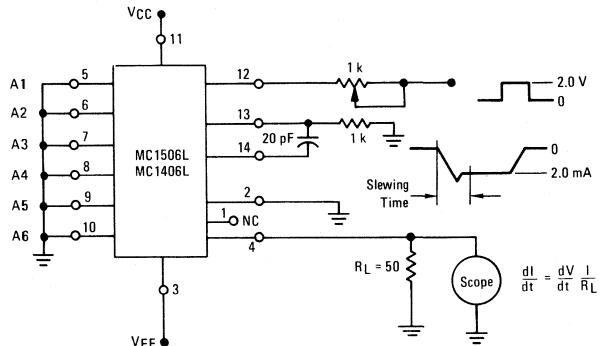


FIGURE 8 – REFERENCE CURRENT SLEW RATE MEASUREMENT TEST CIRCUIT



TEST CIRCUITS and TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – TRANSIENT RESPONSE

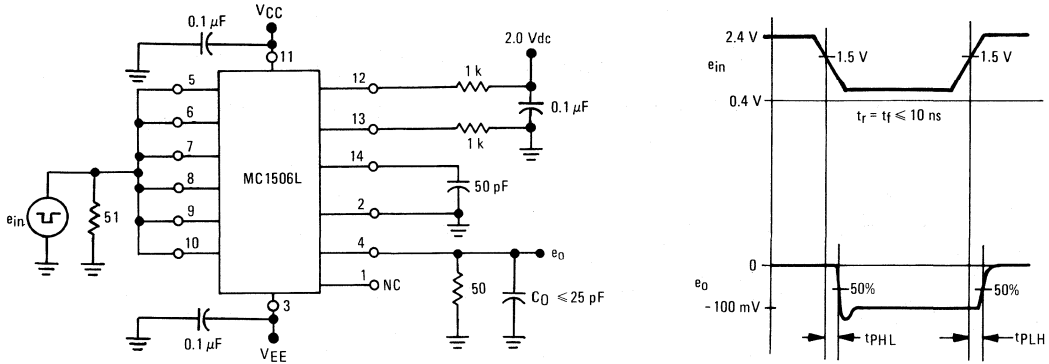


FIGURE 10 – RELATIVE ACCURACY TEST CIRCUIT

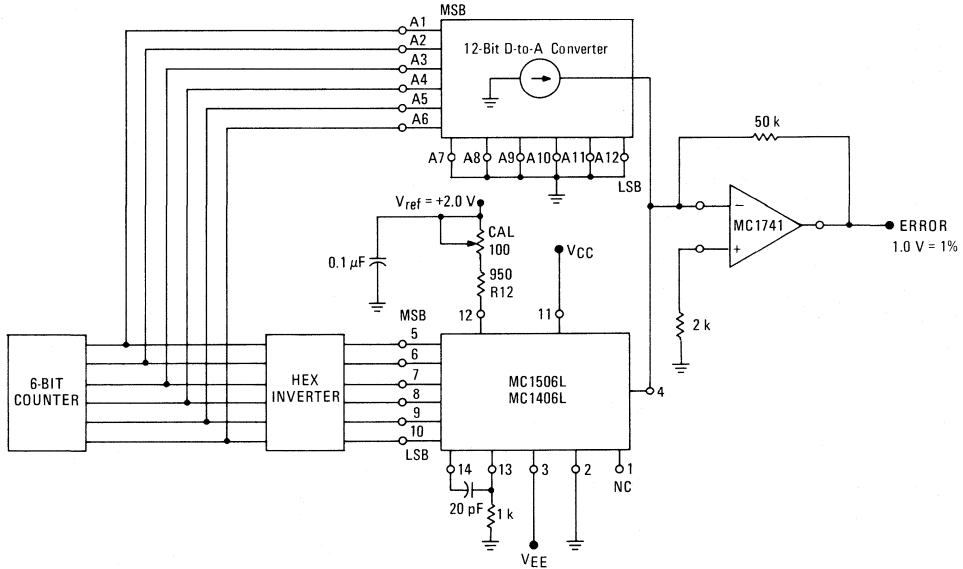


FIGURE 11 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE

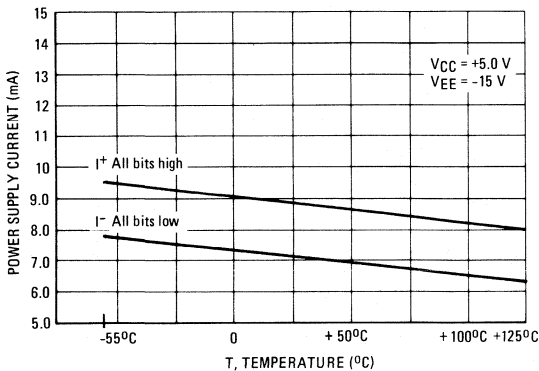
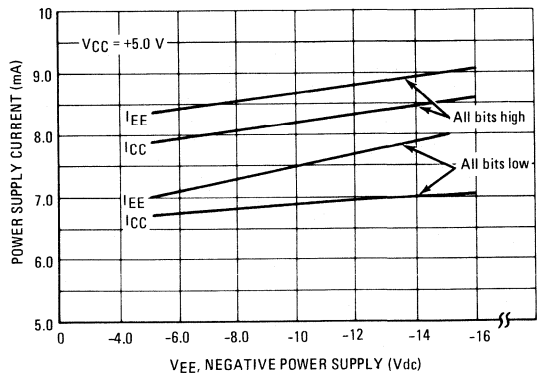


FIGURE 12 – TYPICAL POWER SUPPLY CURRENT versus VEE



TYPICAL CHARACTERISTICS (continued)

FIGURE 13 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

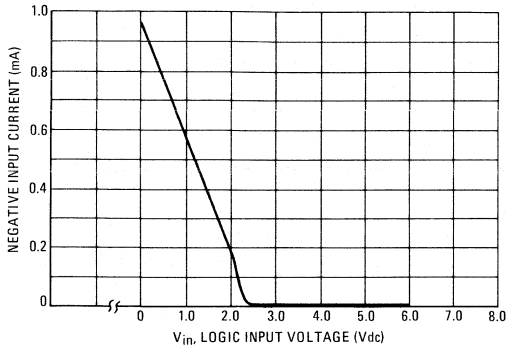


FIGURE 14 – MSB TRANSFER CHARACTERISTICS versus TEMPERATURE (MSB IS "WORST CASE")

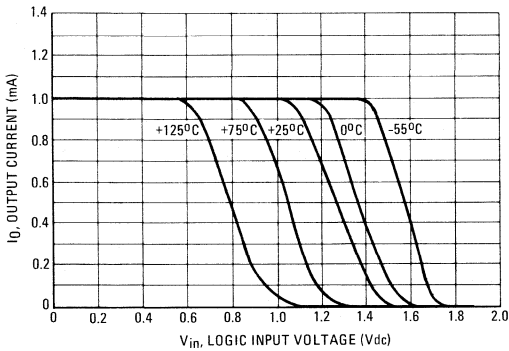
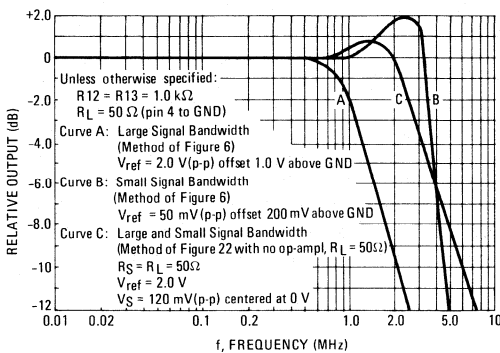


FIGURE 15 – REFERENCE INPUT FREQUENCY RESPONSE



GENERAL INFORMATION

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages below -6.0 volts, due to the increased voltage drop across the 400-ohm resistors in the reference current amplifier.

Output Voltage Compliance

The MC1506L current switches have been designed for high-speed operation and as a result have a restricted output voltage range, as shown in Figures 4 and 5. When a current switch is turned "off", the follower emitter is near ground and a positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington amplifier is one diode voltage below ground; thus a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

For example, at +25°C the allowable voltage compliance on pin 4 to maintain six-bit accuracy is ±0.4 volt. With a full scale output current of 2.0 mA, the maximum resistor value that can be connected from pin 4 to ground is 200 ohms.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1506L is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current.

The best temperature performance is achieved with a -6.0 V supply and a reference voltage of -3.0 volts. These conditions match the voltage across the NPN current source pair in the reference amplifier at the lowest possible voltage, matching and optimizing the output impedance of the pair.

The MC1506L/MC1406L is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.969 mA. This corresponds to a reference amplifier output current drive to the ladder of 2.0 mA, with the loss of one LSB = 31 μA that is the ladder remainder shunted to ground. The input current to pin 12 has a guaranteed current range value of between 1.9 to 2.1 mA, allowing

GENERAL INFORMATION (continued)

some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 10. The 12-bit converter is calibrated for a full scale output current of 1.969 mA. This is an optional step since the MC1506L accuracy is essentially the same between 1.5 to 2.5 mA. Then the MC1506L full scale current is trimmed to the same value with R12 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 6-bit D-to-A converters may not be used to construct a 12-bit accurate D-to-A converter. 12-bit accuracy implies a total error of $\pm 1/2$ of one part in 4096, or $\pm 0.012\%$, which is more accurate than the $\pm 0.78\%$ specification provided by the MC1506L.

Multiplying Accuracy

The MC1506L may be used in the multiplying mode with six-bit accuracy when the reference current is varied over a range of 64:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions these six amplifiers can contribute a total of $6.0 \mu\text{A}$ extra current at the output terminal. If the reference current in the multiplying mode ranges from $60 \mu\text{A}$ to 4.0 mA, the $6.0 \mu\text{A}$ contributes an error of 0.1 LSB. This is well within six-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1506L is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a high-to-low transition for all bits. This time is typically 150 ns to within $\pm 1/2$ LSB, while the turn "off" is typically under 50 ns.

The slowest single switch is the least significant bit, which turns "on" and settles in 50 ns and turns "off" in 30 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 150 ns may be realized.

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 12 for converting the reference voltage to a current, and a turn-

around circuit or current mirror for feeding the ladder. The reference amplifier input current, I12, must always flow into pin 12 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6. The reference voltage source supplies the full current I12. Compensation is accomplished by Miller feedback from pin 14 to pin 13. This compensation method yields the best slew rate, typically better than $2.0 \text{ mA}/\mu\text{s}$, and is independent of the value of R12. R13 must be used to establish the proper impedance for compensation at pin 13. For bipolar reference signals, as in the multiplying mode, R13 can be tied to a negative voltage corresponding to the minimum input level. Another method is shown in Figure 22.

It is possible to eliminate R13 with only a small sacrifice in accuracy and temperature drift. For instance when high-speed operation is not needed, a capacitor is connected from pin 14 to V_{EE} . The capacitor value must be increased when R12 is made larger to maintain a proper phase margin. For R12 values of 1.0, 2.5, and 5.0 kilohms, minimum capacitor values are 50, 125, and 250 pF.

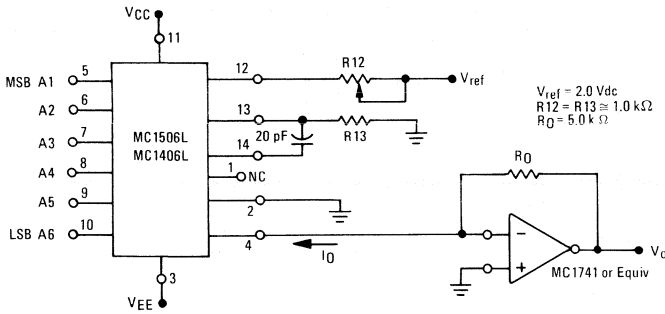
Connections for a negative reference voltage are shown in Figure 7. A high input impedance is the advantage of this method, but Miller feedback cannot be used because it feeds the input signal around the PNP directly into the high impedance node, causing slewing problems and high frequency peaking. Compensation involves a capacitor to V_{EE} on pin 14, using the values of the previous paragraph. The negative reference voltage must be at least 3.0 V above V_{EE} . Bipolar input signals may be handled by connecting R12 to a positive reference voltage equal to the peak positive input level at pin 13.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0 V logic supply is not recommended as a reference voltage. If a well regulated 5.0 V supply which drives logic is to be used as the reference, R12 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with $0.1 \mu\text{F}$ to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 12 and ground.

If pin 12 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, thus decreasing the overall bandwidth.

APPLICATIONS INFORMATION

FIGURE 16 – OUTPUT CURRENT VOLTAGE CONVERSION



$V_{ref} = 2.0 \text{ Vdc}$
 $R_{12} = R_{13} \cong 1.0 \text{ k}\Omega$
 $R_O = 5.0 \text{ k}\Omega$

Theoretical V_O

$$V_O = \frac{V_{ref}}{R_{12}} (R_O) \left(\frac{\bar{A}1}{2} + \frac{\bar{A}2}{4} + \frac{\bar{A}3}{8} + \frac{\bar{A}4}{16} + \frac{\bar{A}5}{32} + \frac{\bar{A}6}{64} \right) = K R_O \left\{ \bar{A} \right\}$$

1) Adjust R_{ref} so that V_O with all digital inputs at low level is equal to 9.844 volts.

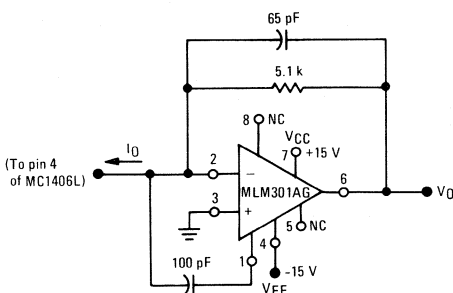
$$V_O = \frac{2 \text{ V}}{1 \text{ k}} (5 \text{ k}) \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} \right) = 10 \text{ V} \left(\frac{63}{64} \right) = 9.844 \text{ V}$$

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1506L at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

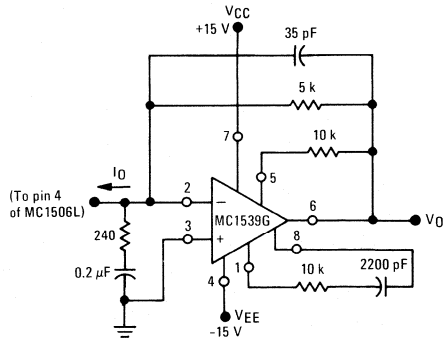
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs .

FIGURE 17

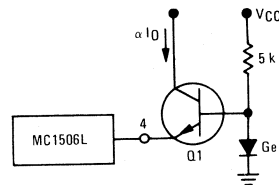


An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μs . See Motorola Application Note AN-459 for more details on this concept.

FIGURE 18



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.



The output voltage range for this circuit is 0 volts to $BVCBO$ of the transistor. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing.

APPLICATIONS INFORMATION (continued)

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1506L requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive, with the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current, see Figure 19. Instead of powering the MC1723G from a single positive voltage supply, it uses a negative bias as well. Although the reference voltage of the MC1723G is then developed with respect to that negative voltage it appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

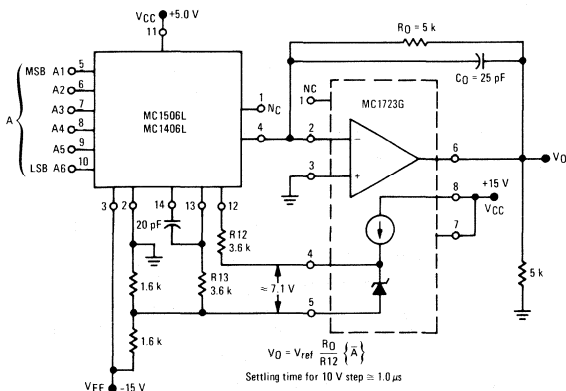
Since ± 15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pull-down resistor on the amplifier output is necessary for fast negative transitions.

Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same $R_O C_O$ product if maximum speed is desired.

Programmable Power Supply

The circuit of Figure 19 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +6.3 volts in 0.1-volt increments, ± 0.05 volt; or 0 to 31.5 volts in 0.5-volt increments, ± 0.25 volt.

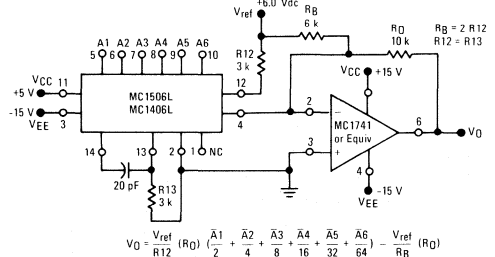
FIGURE 19 — COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



Bipolar or Negative Output Voltage

The circuit of Figure 20 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 6-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V (p-p) output range.

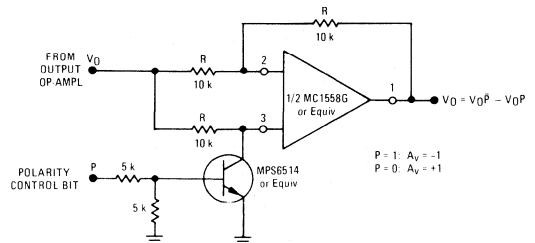
FIGURE 20 — BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



Polarity Switching Circuit, 6-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 21, gives 6-bits magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and -1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 21 — POLARITY SWITCHING CIRCUIT (6-Bit Magnitude Plus Sign D-to-A Converter)

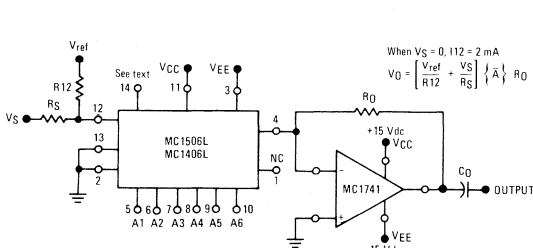


APPLICATIONS INFORMATION (continued)

Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1506L can be applied as a digital attenuator. See Figure 22. One advantage of this technique is that if $R_S = 50$ ohms, no compensation capacitor is needed and a wide large signal bandwidth is achieved. The small and large signal bandwidths are now identical and are shown in Figure 15.

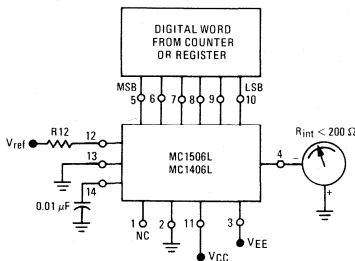
FIGURE 22 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



Panel Meter Readout

The MC1506L can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R12 or Vref.

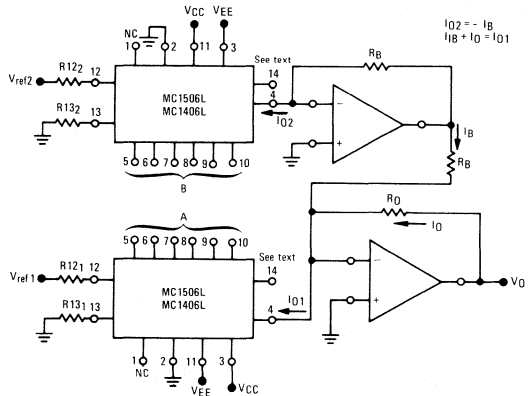
FIGURE 23 – PANEL METER READOUT CIRCUIT



The best frequency response is obtained by not allowing I_{12} to reach zero. R_S can be set for a ± 1.0 mA variation in relation to I_{12} . I_{12} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word that makes ac coupling necessary.

FIGURE 24 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



$$I_0 = I_{01} - I_{02} = \frac{V_{ref1}}{R_{121}} \{A\} - \frac{V_{ref2}}{R_{122}} \{B\}$$

Digital Subtraction:
let $\frac{V_{ref1}}{R_{121}} = \frac{V_{ref2}}{R_{122}}$

$$V_0 = \frac{V_{ref1}}{R_{121}} R_0 \{ \{A\} - \{B\} \}$$

Programmable Amplifier:
Connect digital inputs so $A = B$

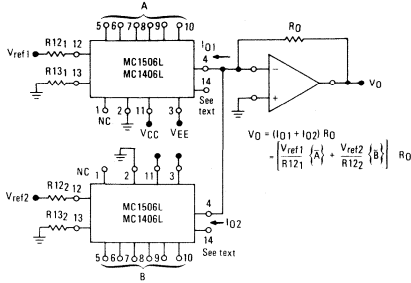
$$V_0 = \frac{V_{ref1}}{R_{121}} \left| \frac{V_{ref1}}{R_{121}} - \frac{V_{ref2}}{R_{122}} \right|$$

This digital subtraction application is useful for indicating when one digital word is approaching another in value. More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods, or applied differentially to R121 and R122 or R131 and R132. VO will be a bipolar signal defined by the above equation. Note that the circuit shown accepts bipolar differential signals but does not have a negative common-mode range. A very useful method is to connect R121 and R122 to a positive reference higher than the most positive input, and drive R131 and R132. This yields high input impedance, bipolar differential and common-mode range. The compensation depends on the input method used, as shown in previous sections.

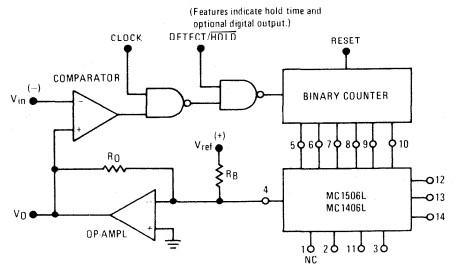
APPLICATIONS INFORMATION (continued)

FIGURE 25 — DIGITAL SUMMING and CHARACTER GENERATION



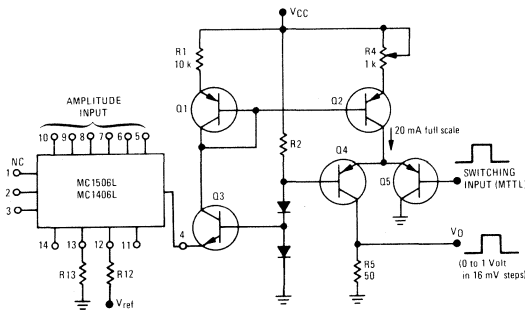
In a character generation system one MC1506L circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 12-bit D-to-A converter (see Accuracy Section).

FIGURE 26 — PEAK DETECTING SAMPLE and HOLD (Features indefinite hold time and optional digital output.)



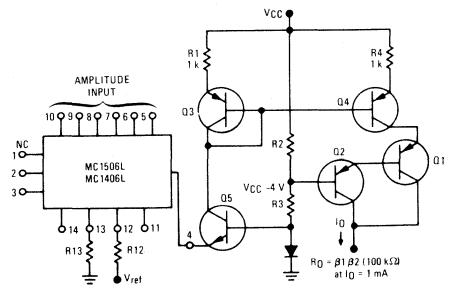
Positive peaks may be detected by inserting a hex inverter between the counter and MC1506L, reversing the comparator inputs, and connecting the output amplifier for unipolar operation.

FIGURE 27 — PROGRAMMABLE PULSE GENERATOR



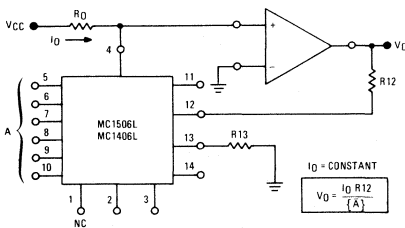
Fast rise and fall times require the use of high speed switching transistors for the differential pair, Q4 and Q5. Linear ramps and sine waves may be generated by the appropriate reference input.

FIGURE 28 — PROGRAMMABLE CONSTANT CURRENT SOURCE



Current pulses, ramps, staircases, and sine waves may be generated by the appropriate digital and reference inputs. This circuit is especially useful in curve tracer applications.

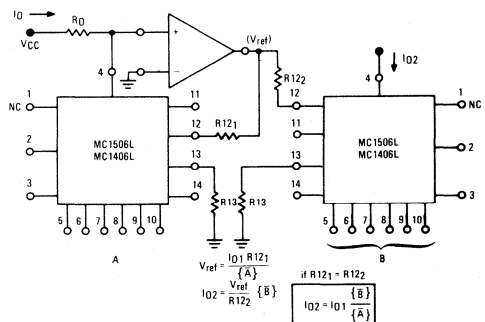
FIGURE 29 — ANALOG DIVISION BY DIGITAL WORD



This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation, IO can be set at 62 μA so that I12 will have a maximum value of 3.938 mA for a digital bit input configuration of 000001.

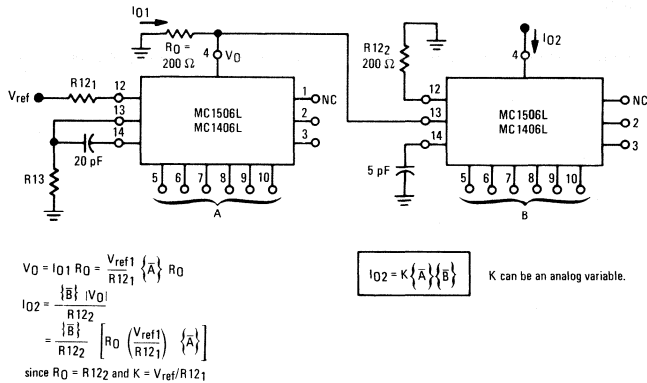
Compensation is necessary for loop stability and depends on the type of operational amplifier used. If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If this cannot be done, the reference amplifier can furnish the dominant pole with extra Miller feedback from pin 14 to 13. If the MC1723 or another wideband amplifier is used, the reference amplifier should always be overcompensated.

FIGURE 30 — ANALOG QUOTIENT OF TWO DIGITAL WORDS



APPLICATIONS INFORMATION (continued)

FIGURE 31 — ANALOG PRODUCT OF TWO DIGITAL WORDS
(High-Speed Operation)



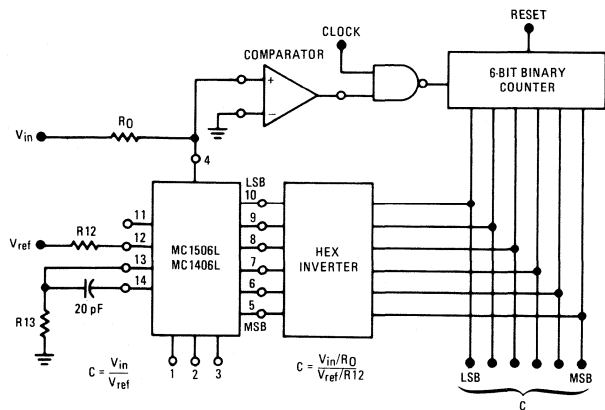
Two Digit BCD Conversion

MC1506L parts which meet the specification for 7-bit accuracy can be used for the most significant word when building a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a

resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten.

FIGURE 32 — DIGITAL QUOTIENT of TWO ANALOG VARIABLES
or ANALOG-TO-DIGITAL CONVERSION

The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.



MC1510G
MC1410G

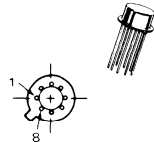
MONOLITHIC WIDEBAND VIDEO AMPLIFIER

... designed for use as a high-frequency differential amplifier with operating characteristics that provide a flat frequency response from dc to 40 MHz.

- High Gain Characteristics
 $A_V = 93$ typ
- Wide Bandwidth – dc to 40 MHz typ
- Large Output Voltage Swing
4.5 V p-p typical @ ± 6.0 V Supply
- Low Output Distortion
THD $\leq 1.5\%$ typ

**VIDEO AMPLIFIER
INTEGRATED CIRCUIT**

METAL PACKAGE
CASE 601
TO-99



(bottom view)

FIGURE 1 – VOLTAGE GAIN versus FREQUENCY

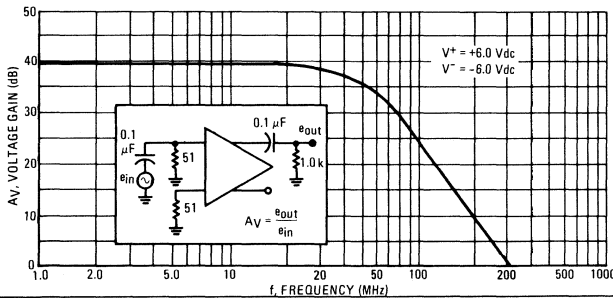
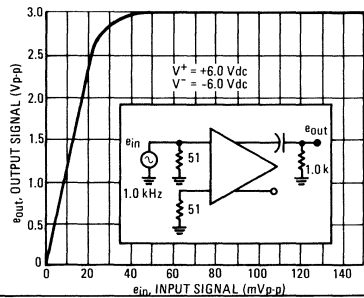
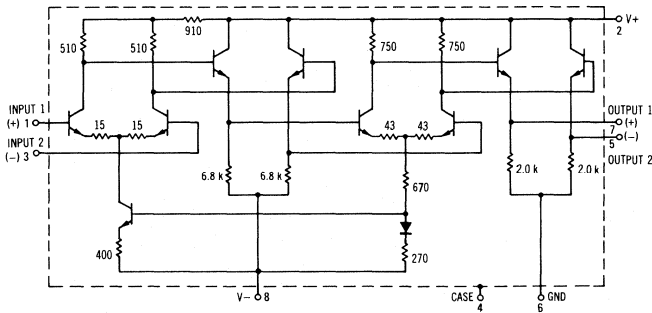


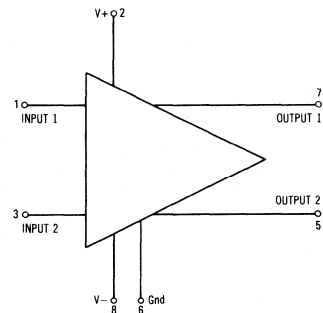
FIGURE 2 – LIMITING CHARACTERISTICS



CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

7

MC1510G, MC1410G (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|-------------------|-------------|-------|
| Power Supply Voltage | V ⁺ | +8.0 | Vdc |
| | V ⁻ | -8.0 | Vdc |
| Differential Input Signal | V _{in} | ±5.0 | Volts |
| Common Mode Input Swing | CMV _{in} | ±6.0 | Volts |
| Load Current | I _L | 10 | mA |
| Output Short Circuit Duration | t _s | 5.0 | s |
| Power Dissipation (Package Limitation) Metal Can Derate above T _A = +25°C | P _D | 680 | mW |
| | | 4.6 | mW/°C |
| Operating Temperature Range MC1410 MC1510 | T _A | 0 to +75 | °C |
| | | -55 to +125 | |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V⁺ = +6 Vdc, V⁻ = -6 Vdc, R_L = 5.0 kohms, T_A = +25°C unless otherwise noted)

| Characteristic | Symbol | MC1510 | | | MC1410 | | | Unit |
|--|----------------------|--------|------|-----|--------|------|-----|-------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Single Ended Voltage Gain | A _{V(se)} | 75 | 93 | 110 | 60 | 90 | 120 | V/V |
| Output Impedance (f = 20 kHz) | Z _{out} | — | 35 | — | — | 35 | — | Ω |
| Input Impedance (f = 20 kHz) | Z _{in} | — | 6.0 | — | — | 6.0 | — | kΩ |
| Bandwidth (-3.0 dB) | BW | — | 40 | — | — | 40 | — | MHz |
| Output Voltage Swing (f = 100 kHz) | V _{out} | — | 4.5 | — | — | 4.5 | — | V _{p-p} |
| Single Ended Output Distortion (e _{in} < 0.2% Distortion) | THD | — | 1.5 | 5.0 | — | 2.0 | — | % |
| Input Common Mode Voltage Swing | CMV _{in} | — | ±1.0 | — | — | ±1.0 | — | V _{peak} |
| Common Mode Voltage Gain (e _{in} = 0.3 V rms, f = 100 kHz) | AVCM | -30 | -45 | — | -20 | -40 | — | dB |
| Common Mode Rejection Ratio | CM _{rej} | — | 85 | — | — | 85 | — | |
| Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$ Differential Output = 0 | I _b | — | 20 | 80 | — | 50 | 100 | μA |
| Input Offset Current (I _{io} = I ₁ - I ₂) | I _{io} | — | 3.0 | 20 | — | 5.0 | 30 | μA |
| Output Offset Voltage Differential Mode (V _{in} = 0) Common Mode (Differential Output = 0) | V _{out(DM)} | — | 0.5 | 1.3 | — | 0.5 | 2.0 | Vdc |
| | V _{out(CM)} | 2.6 | 3.1 | 3.5 | 2.0 | 3.0 | 4.0 | |
| Step Response | t _f | — | 9.0 | 12 | — | 10 | 15 | ns |
| | t _{pd} | — | 9.0 | — | — | 9.0 | — | |
| | t _r | — | 9.0 | 12 | — | 10 | 15 | |
| Average Temperature Coefficient of Input Offset Voltage (R _S = 50 Ω, T _A = T _{low} * to T _{high} **) (R _S ≤ 10 k Ω, T _A = T _{low} to T _{high}) | TC _{Vio} | — | ±3.0 | — | — | ±3.0 | — | μV/°C |
| | | — | ±6.0 | — | — | ±6.0 | — | |
| DC Power Dissipation (Power Supply = ±6.0 V) | P _D | — | 150 | 220 | — | 165 | 220 | mW |
| Equivalent Average Input Noise Voltage (f = 10Hz to 500 kHz) (R _S = 0) | V _n | — | 5.0 | — | — | 5.0 | — | μV |

*T_{low} = 0°C for MC1410
or -55°C for MC1510

**T_{high} = +75°C for MC1410 or
+125°C for MC1510

TYPICAL CHARACTERISTICS

($V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 3
POWER DISSIPATION versus SUPPLY VOLTAGE

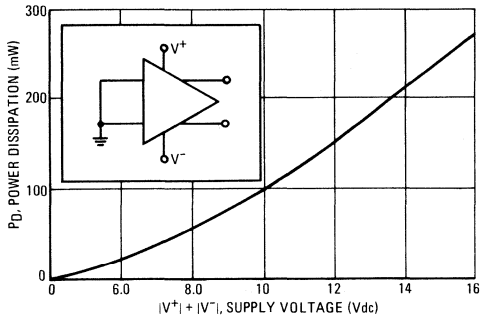


FIGURE 4
VOLTAGE GAIN versus SUPPLY VOLTAGE

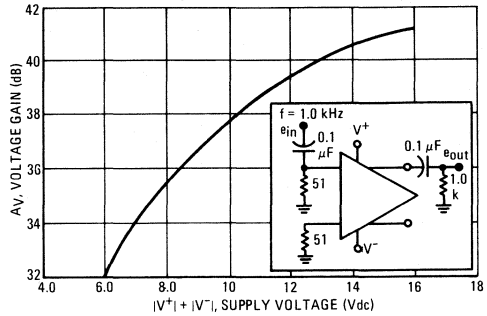


FIGURE 5
VOLTAGE GAIN versus TEMPERATURE

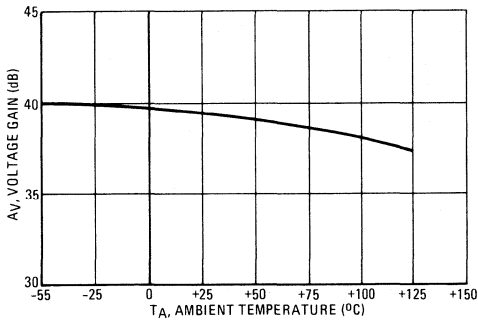


FIGURE 6
DC OUTPUT VOLTAGE versus TEMPERATURE

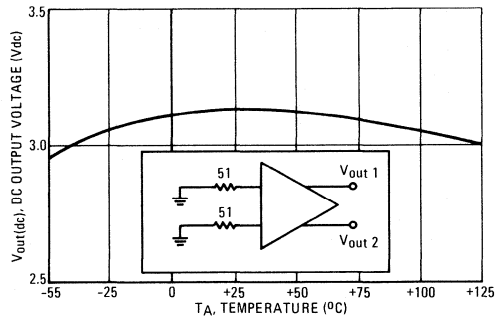


FIGURE 7
INPUT BIAS CURRENT versus TEMPERATURE

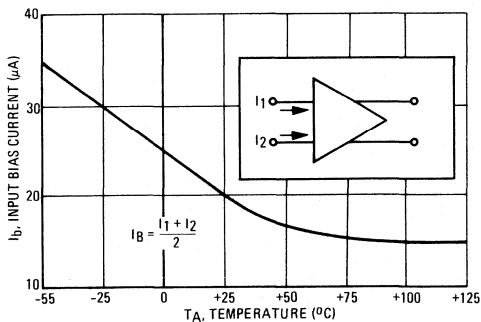
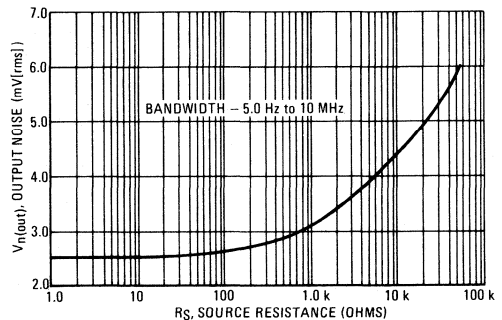


FIGURE 8
OUTPUT NOISE VOLTAGE versus SOURCE IMPEDANCE



7

TYPICAL APPLICATIONS

FIGURE 9
ENVELOPE DETECTOR

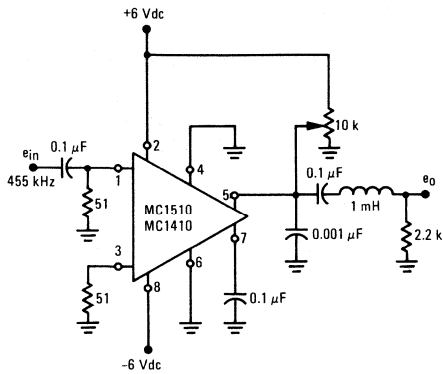


FIGURE 10
TWO STAGE VIDEO AMPLIFIER WITH ADJUSTABLE GAIN

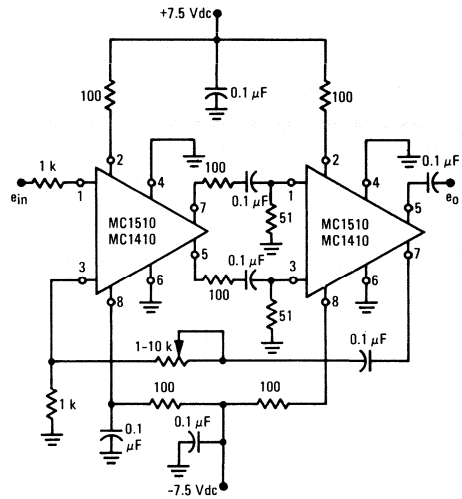


FIGURE 11
SINGLE STAGE WIDEBAND AMPLIFIER

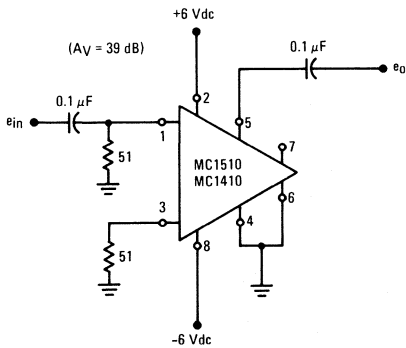
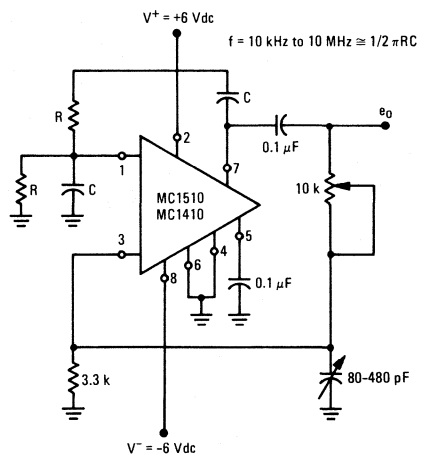


FIGURE 12
WEIN BRIDGE OSCILLATOR



MC1514L

DUAL DIFFERENTIAL COMPARATOR

MONOLITHIC DUAL DIFFERENTIAL VOLTAGE COMPARATOR

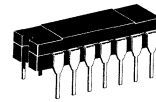
... designed for use in level detection, low-level sensing, and memory applications.

Typical Amplifier Features:

- Two Separate Outputs
- Strobe Capability
- High Output Sink Current – 2.8 mA min Each Comparator
- Differential Input Characteristics:
Input Offset Voltage = 1.0 mV
Offset Voltage Drift = 3.0 $\mu\text{V}/^\circ\text{C}$
- Short Propagation Delay Time – 40 ns
- Output Compatible with All Saturating Logic Forms
 $V_{\text{out}} = +3.2 \text{ V to } -0.5 \text{ V typical}$

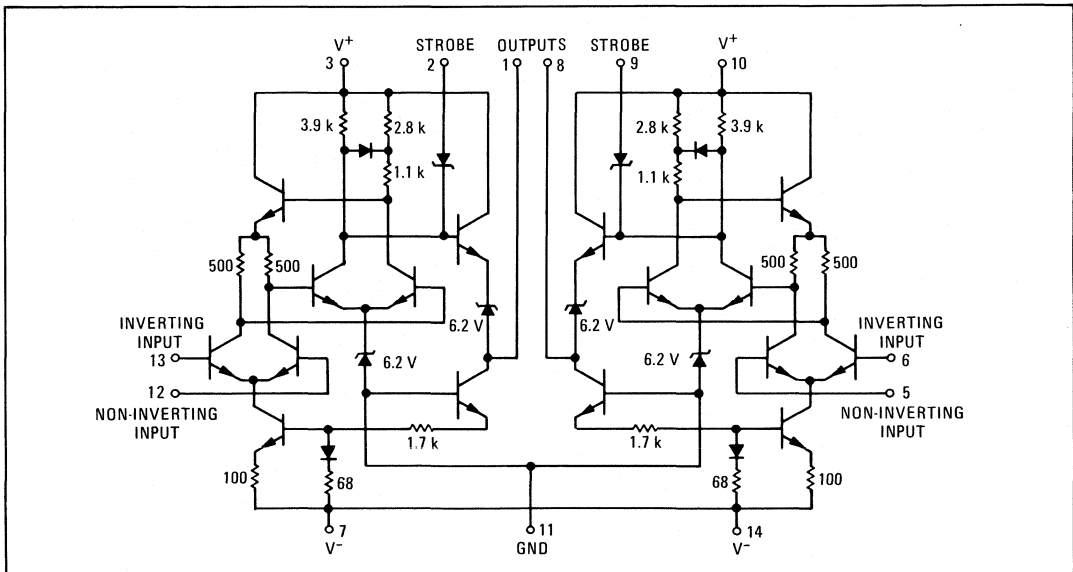
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|--------------------------|-------------|------------------------------------|
| Power Supply Voltage | V^+ V^- | +14 -7.0 | V_{dc} V_{dc} |
| Differential Input Signal | V_{in} | ± 5.0 | Volts |
| Common Mode Input Swing | CMV_{in} | ± 7.0 | Volts |
| Peak Load Current | I_L | 10 | mA |
| Power Dissipation (package limitation) Ceramic Dual-In-Line Package Derate above $T_A = +25^\circ\text{C}$ | P_D | 1000 6.7 | mW $\text{mW}/^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |



CERAMIC PACKAGE
CASE 632
TO-116

CIRCUIT SCHEMATIC

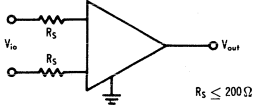
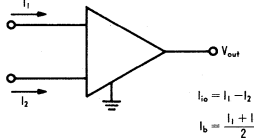
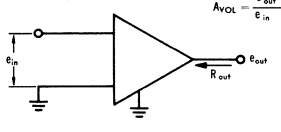
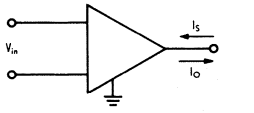
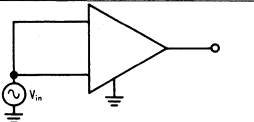
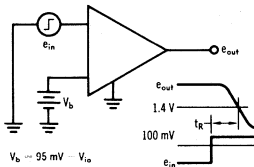
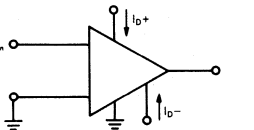


See Packaging Information Section for outline dimensions.

7

MC1514L (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +12$ Vdc, $V^- = -6$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted) (Each Comparator)

| Characteristic Definitions (linear operation) | Characteristic | Symbol | Min | Typ | Max | Unit |
|---|--|---|---------------------------------|-------------------------|--------------------|------------------------------|
|  | Input Offset Voltage $V_{out} = 1.4$ Vdc, $T_A = 25^\circ\text{C}$ $V_{out} = 1.8$ Vdc, $T_A = -55^\circ\text{C}$ $V_{out} = 1.0$ Vdc, $T_A = +125^\circ\text{C}$ | V_{io} | - | 1.0 | 2.0 | mVdc |
| | Temperature Coefficient of Input Offset Voltage | $TC_{V_{io}}$ | - | 3.0 | - | $\mu\text{V}/^\circ\text{C}$ |
|  | Input Offset Current $V_{out} = 1.4$ Vdc, $T_A = 25^\circ\text{C}$ $V_{out} = 1.8$ Vdc, $T_A = -55^\circ\text{C}$ $V_{out} = 1.0$ Vdc, $T_A = +125^\circ\text{C}$ | I_{io} | - | 1.0 | 3.0 | μA dc |
| | Input Bias Current $V_{out} = 1.4$ Vdc, $T_A = 25^\circ\text{C}$ $V_{out} = 1.8$ Vdc, $T_A = -55^\circ\text{C}$ $V_{out} = 1.0$ Vdc, $T_A = +125^\circ\text{C}$ | I_b | - | 12 | 20 | μA dc |
|  | Open Loop Voltage Gain $T_A = 25^\circ\text{C}$ $T_A = -55$ to $+125^\circ\text{C}$ | A_{VOL} | 1250 | 1700 | - | V/V |
| | Output Resistance | R_{out} | - | 200 | - | ohms |
|  | Differential Voltage Range $V_{in} \cong 5.0$ mV, $0 \cong I_o \cong 5.0$ mA Positive Output Voltage $V_{in} \cong -5.0$ mV Negative Output Voltage $V_{in} \cong -5.0$ mV Output Sink Current $V_{in} \cong -5.0$ mV, $V_{out} \cong 0$, $T_A = -55$ to $+125^\circ\text{C}$ | V_{in} V_{OH} V_{OL} I_s | ± 5.0 2.5 -1.0 2.8 | - 3.2 -0.5 3.4 | - 4.0 0 - | Vdc Vdc Vdc mA |
|  | Input Common Mode Range $V^- = -7.0$ Vdc Common Mode Rejection Ratio $V^- = -7.0$ Vdc, $R_S \cong 200\Omega$ | CMV_{in} CM_{rej} | ± 5.0 80 | - 100 | - - | Volts dB |
|  | Propagation Delay Time For Positive and Negative Going Input Pulse | t_{pd} | - | 40 | - | ns |
|  | Total Power Supply Current $V_{out} \cong 0$ Vdc Total Power Consumption | I_{D+} I_{D-} | - - | 12.8 11 | 18 14 | mA mW |

TYPICAL CHARACTERISTICS
(Each Comparator)

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

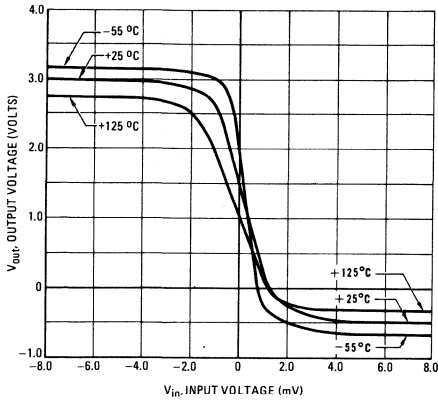


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

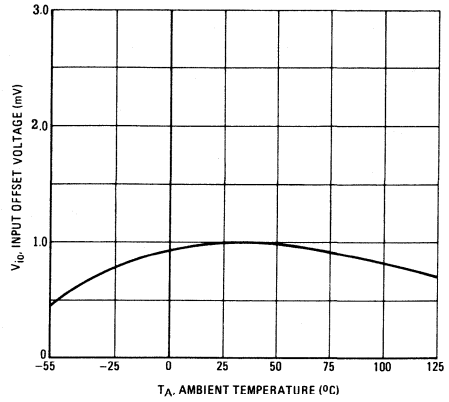


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

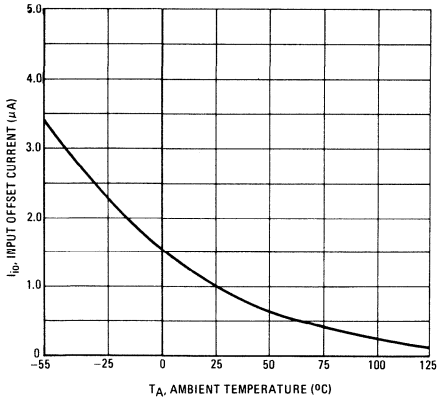


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE

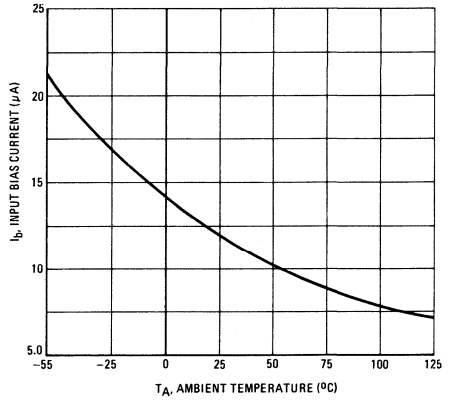


FIGURE 5 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

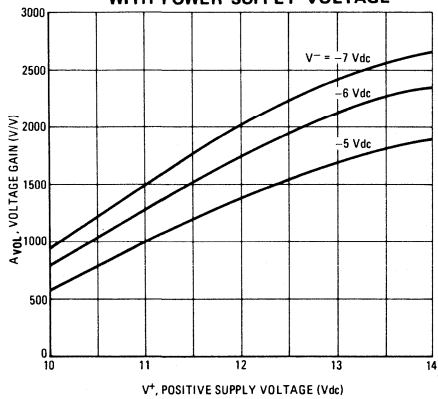
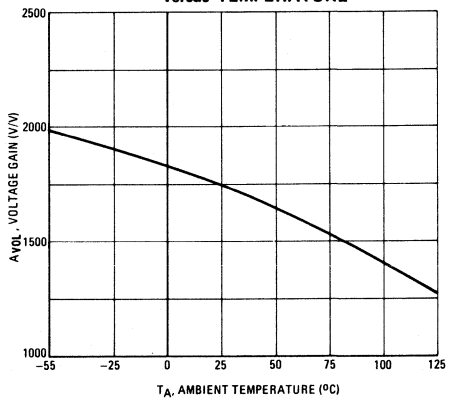


FIGURE 6 – VOLTAGE GAIN versus TEMPERATURE



MC1514L (continued)

FIGURE 7 – RESPONSE TIME

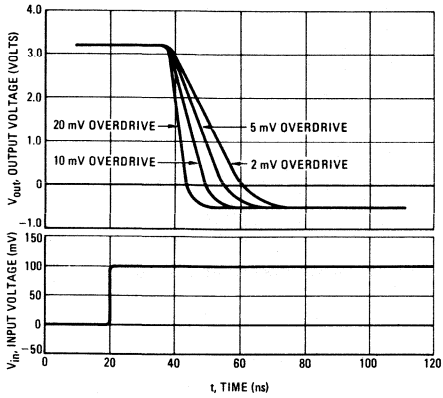


FIGURE 8 – POWER DISSIPATION versus TEMPERATURE

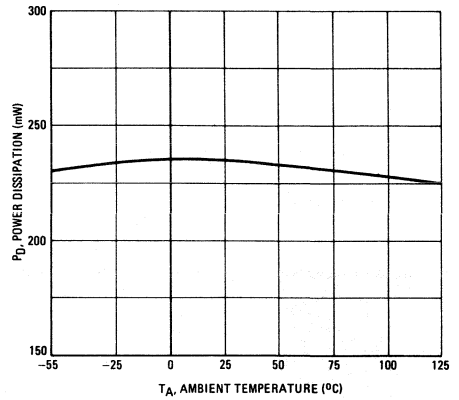


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

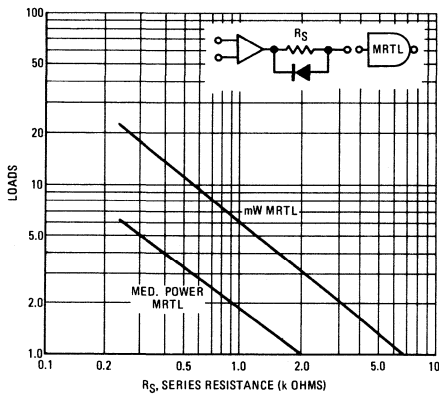


FIGURE 10 – SINK CURRENT versus TEMPERATURE

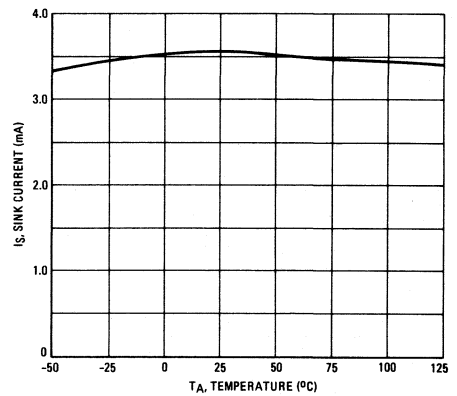
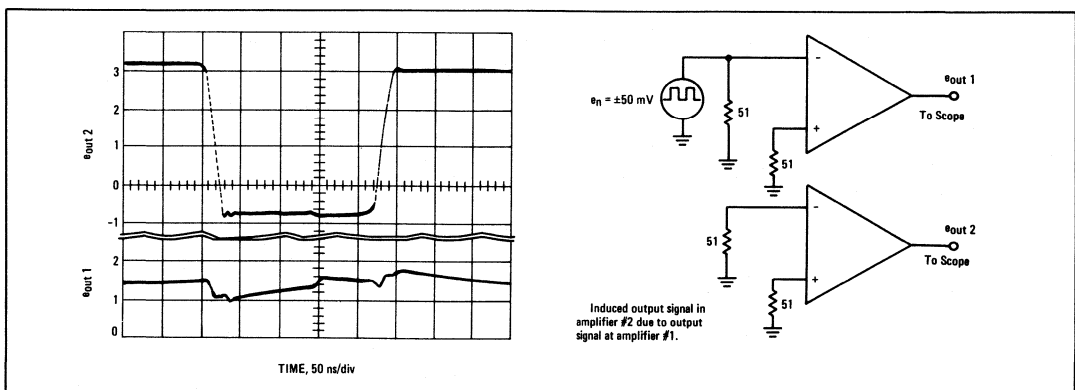


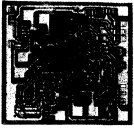
FIGURE 11 – CROSSTALK†



†Worst case condition shown -- no load.

**MC1520
MC1420**

MONOLITHIC DIFFERENTIAL OUTPUT OPERATIONAL AMPLIFIER

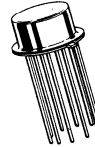


... designed for use in general-purpose or wide-band differential amplifier applications, especially those requiring differential outputs.

Typical Characteristics

- Differential Input and Differential Output
- Wide Closed-Loop Bandwidth; 10 MHz
- Differential Gain; 70 dB
- High Input Impedance; 2.0 megohms:
- Low Output Impedance; 50 ohms

**OPERATIONAL AMPLIFIER
MONOLITHIC SILICON
INTEGRATED
CIRCUIT**



Pin 3 connected to case

**G SUFFIX
METAL PACKAGE
CASE 602A**



**F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91**

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|------------------|-------------------------|----------------------|
| Power Supply Voltage | V^+ V^- | +8.0 -8.0 | Vdc |
| Differential Input Signal | V_{in} | ± 8.0 | Vdc |
| Load Current | I_{L1}, I_{L2} | 15 | mA |
| Power Dissipation (Package Limitation) | P_D | | |
| Metal Package | | 680 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 4.6 | mW/ $^\circ\text{C}$ |
| Flat Package | | 500 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 3.3 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | MC1520 MC1420 | T_A | $^\circ\text{C}$ |
| | | -55 to +125 0 to +75 | |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

CIRCUIT SCHEMATICS

FIGURE 1 - CIRCUIT SCHEMATIC

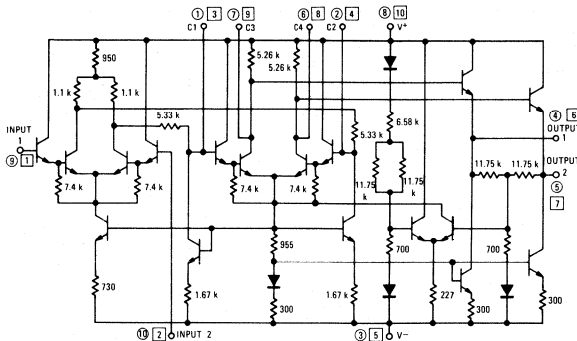
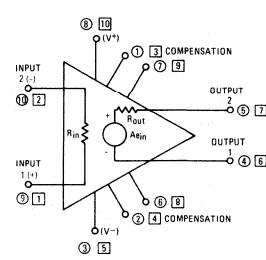


FIGURE 2 - EQUIVALENT CIRCUIT



○ contains pin number for metal can package
□ contains pin number for flat package

See Packaging Information Section for outline dimensions.

MC1520, MC1420 (continued)

SINGLE-ENDED ELECTRICAL CHARACTERISTICS

($V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MC1520 | | | MC1420 | | | Unit |
|--|--|------------|------------|-----|-----------|------------|-----|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Open Loop Voltage Gain ($T_{\text{low}} \textcircled{2} \leq T_A \leq T_{\text{high}} \textcircled{2}$) | A_{VOL} | 1000 60 | 1500 64 | — | 750 — | 1500 64 | — | V/V dB |
| Output Impedance ($f = 20$ Hz) | Z_{out} | — | 50 | 100 | — | 50 | — | ohms |
| Input Impedance ($f = 20$ Hz) | Z_{in} | 0.5 | 2.0 | — | — | 2.0 | — | megohms |
| Output Voltage Swing ($R_L = 7.0$ k Ω [Figure 8]) | V_o | ± 3.5 | ± 4.0 | — | ± 3.0 | ± 4.0 | — | V_{peak} |
| Input Common-Mode Voltage Swing | CMV_{in} | ± 2.0 | ± 3.0 | — | — | ± 3.0 | — | V_{peak} |
| Common-Mode Rejection Ratio | CM_{rej} | 75 | 90 | — | 60 | 90 | — | dB |
| Input Bias Current ($I_{\text{b}} = \frac{I_1 + I_2}{2}$, $T_A = +25^\circ\text{C}$) | I_{b} | — | 0.8 | 2.0 | — | 2.0 | 40 | μA |
| Input Offset Current ($I_{\text{io}} = I_1 - I_2$) ($I_{\text{io}} = I_1 - I_2$, $T_A = T_{\text{low}}$) ($I_{\text{io}} = I_1 - I_2$, $T_A = T_{\text{high}}$) | $ I_{\text{io}} $ | — | 30 | 100 | — | 30 | 200 | nA |
| Input Offset Voltage ($T_A = +25^\circ\text{C}$) | $ V_{\text{io}} $ | — | 5.0 | 10 | — | 5.0 | 15 | mV |
| Step Response Gain = 1.0, 10% Overshoot $R_1 = 10$ k Ω $R_2 = 10$ k Ω $R_3 = 5.0$ k Ω $C_s = 39$ pF | t_f t_{pd} $dV_{\text{out}}/dt \textcircled{1}$ | — | 80 | — | — | 80 | — | ns ns V/ μs |
| Gain = 10, 10% Overshoot $R_1 = 10$ k Ω $R_2 = 100$ k Ω $R_3 = 10$ k Ω $C_s = 10$ pF | t_f t_{pd} $dV_{\text{out}}/dt \textcircled{1}$ | — | 80 | — | — | 80 | — | ns ns V/ μs |
| Gain = 100, No Overshoot $R_1 = 1.0$ k Ω $R_2 = 100$ k Ω $R_3 = 1.0$ k Ω $C_s = 1.0$ pF | t_f t_{pd} $dV_{\text{out}}/dt \textcircled{1}$ | — | 80 | — | — | 80 | — | ns ns V/ μs |
| Open Loop, No Overshoot $R_1 = 50$ Ω $R_2 = \infty$ $R_3 = 50$ Ω $C_s = 0$ | t_f t_{pd} $dV_{\text{out}}/dt \textcircled{1}$ | — | 180 | — | — | 180 | — | ns ns V/ μs |
| Bandwidth: (Open Loop [Figure 4]) (Closed Loop [Unity Gain]) (Figure 5) | — | — | 2.0 | — | — | 2.0 | — | MHz |
| Input Noise Voltage (Open Loop) (5.0 Hz - 5.0 MHz) | $V_{\text{n(in)}}$ | — | 11 | 15 | — | 11 | — | $\mu\text{V(rms)}$ |
| Average Temperature Coefficient of Input Offset Voltage ($R_S = 50$ Ω , $T_A = T_{\text{low}}$ to T_{high}) | $ \text{TCV}_{\text{io}} $ | — | 2.0 | — | — | 2.0 | — | $\mu\text{V}/^\circ\text{C}$ |
| DC Power Dissipation ($V_o = 0$) | P_D | — | 120 | 240 | — | 120 | 240 | mW |
| Power Supply Sensitivity (V^\pm Constant) | S^\pm | — | 250 | 450 | — | 250 | — | $\mu\text{V}/\text{V}$ |

$\textcircled{1}$ $dV_{\text{out}}/dt = \text{Slew Rate}$

$\textcircled{2}$ $T_{\text{low}} = 0^\circ\text{C}$ for MC1420, -55°C for MC1520 $T_{\text{high}} = +75^\circ\text{C}$ for MC1420 $+125^\circ\text{C}$ for MC1520

MC1520, MC1420 (continued)

DIFFERENTIAL ELECTRICAL CHARACTERISTICS

($V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MC1520 | | | MC1420 | | | Unit |
|---|------------|------------|------------|------|------------|------------|-----|-------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Gain (Open Loop) | A_{VOL} | 2000 66 | 3000 70 | — | 1500 64 | 3000 70 | — | V/V dB |
| Input Impedance (f = 20 Hz) | Z_{in} | 0.5 | 2.0 | — | — | 2.0 | — | megohms |
| Output Impedance (f = 20 Hz) | Z_{out} | — | 100 | 200 | — | 100 | — | ohms |
| Common-Mode Output Voltage | V_O (CM) | -0.5 | 0 | +0.5 | — | 0 | — | Vdc |
| Output Voltage Swing ($R_L = 7.0$ k Ω) | V_o | ± 7.0 | ± 8.0 | — | ± 6.0 | ± 8.0 | — | V _{peak} |

TYPICAL CHARACTERISTICS

($V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

FIGURE 3 — LARGE SIGNAL SWING versus FREQUENCY

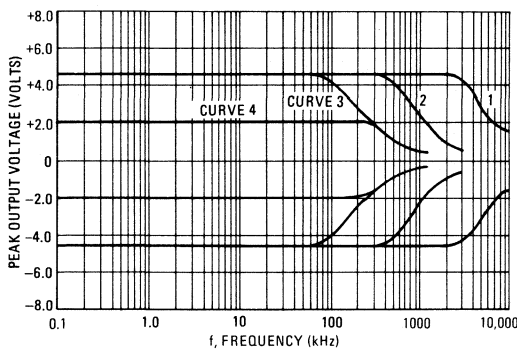
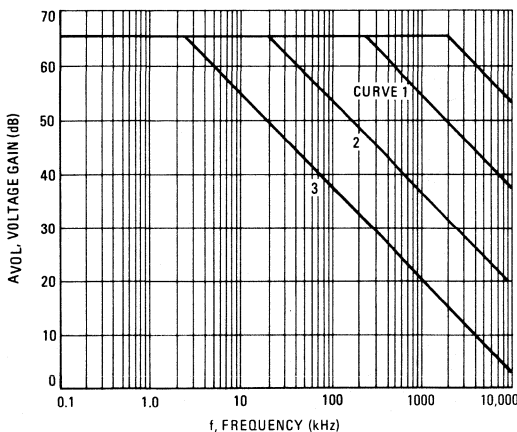
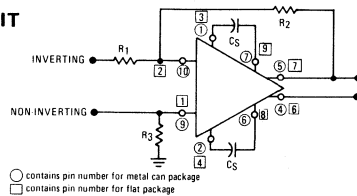


FIGURE 4 — OPEN LOOP VOLTAGE GAIN

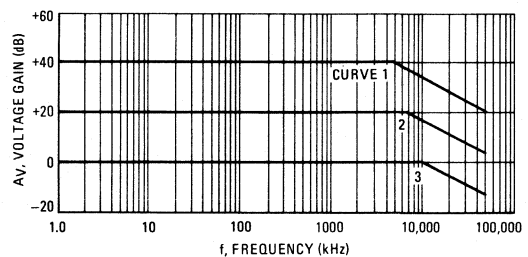


TEST CIRCUIT



| FIGURE NO. | CURVE NO. | MODE | VOLTAGE GAIN | TEST CONDITIONS | | | | NOISE OUTPUT mV (rms) |
|------------|-----------|---------------|--------------|--------------------|--------------------|--------------------|------------|-----------------------|
| | | | | R_1 (Ω) | R_2 (Ω) | R_3 (Ω) | C_S (pF) | |
| 3 | 1 | INVERTING | 100 | 1.0 k | 100 k | 1.0 k | 1.0 | 2.0 |
| | 2 | INVERTING | 10 | 10 k | 100 k | 10 k | 10 | 0.55 |
| | 3 | INVERTING | 1.0 | 10 k | 10 k | 5.0 k | 39 | 0.17 |
| | 4 | NON-INVERTING | 1.0 | ∞ | 10 k | 10 k | 39 | 0.17 |
| 4 | 1 | NON-INVERTING | A_{VOL} | 0 | ∞ | 50 | 1.0 | 1.0 |
| | 2 | NON-INVERTING | A_{VOL} | 0 | ∞ | 50 | 10 | 2.0 |
| | 3 | NON-INVERTING | A_{VOL} | 0 | ∞ | 50 | 39 | 5.2 |
| 5 | 1 | NON-INVERTING | 100 | 100 | 10 k | 100 | 1.0 | 2.0 |
| | 2 | NON-INVERTING | 10 | 1.0 k | 9.1 k | 910 | 10 | 0.55 |
| | 3 | NON-INVERTING | 1.0 | ∞ | 10 k | 10 k | 39 | 0.17 |

FIGURE 5 — CLOSED LOOP VOLTAGE GAIN versus FREQUENCY



TYPICAL OUTPUT CHARACTERISTICS
 ($V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, unless otherwise noted.)

FIGURE 6 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

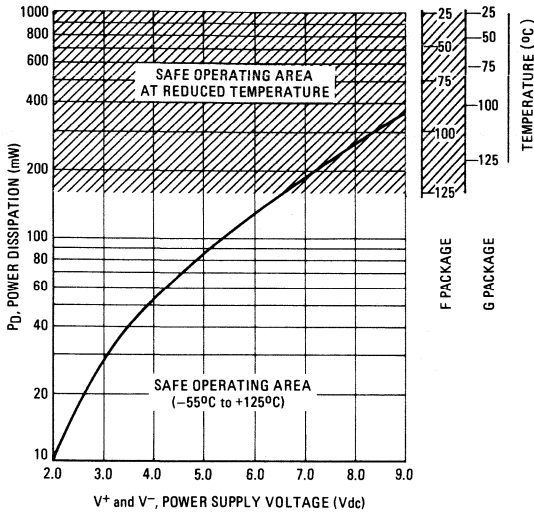


FIGURE 7 – OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

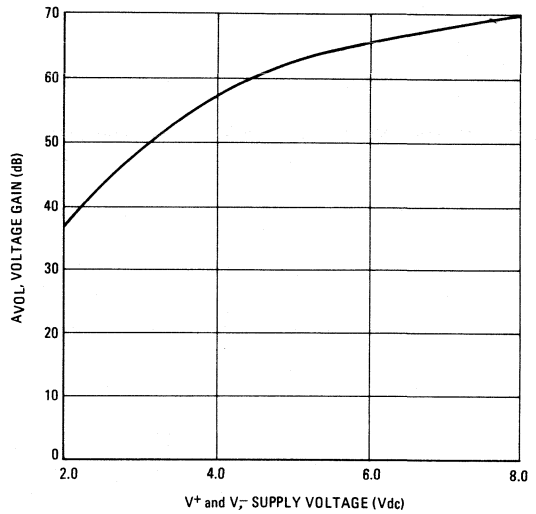


FIGURE 8 – SINGLE ENDED OUTPUT VOLTAGE versus LOAD RESISTANCE

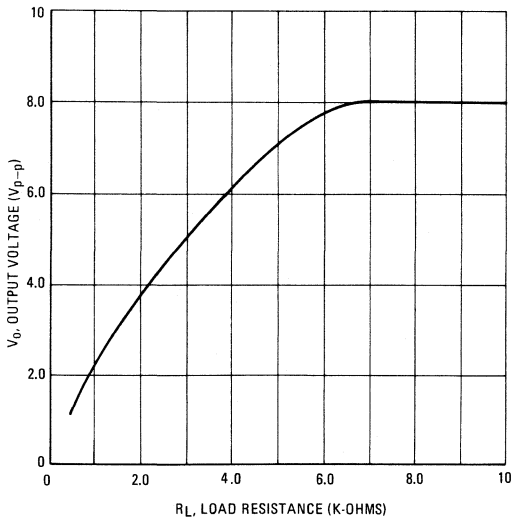
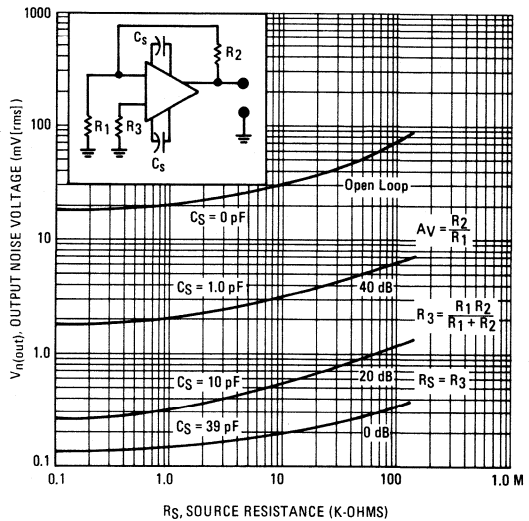


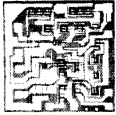
FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE



OPERATIONAL AMPLIFIERS

MC1530, MC1430 MC1531, MC1431

MONOLITHIC OPERATIONAL AMPLIFIER



... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MC1531 (MC1431) is provided with Darlington inputs to increase input impedance; otherwise the MC1531 (MC1431) circuit is identical with the MC1530 (MC1430) circuit.

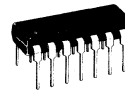
- High Open Loop Voltage Gain – 4500 min (MC1530) – 2500 min (MC1531)
- High Input Impedance – 10 Kiloohms min (MC1530) – 1.0 Megohm min (MC1531)
- Low Output Impedance – 50 Ohms max
- High Slew Rate – 6.0 V/ μ s typ @ $A_{vs} = 10$
- High Open Loop Bandwidth – 2.0 MHz typ (MC1530) 0.4 MHz typ (MC1531)

OPERATIONAL AMPLIFIERS INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 602B

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



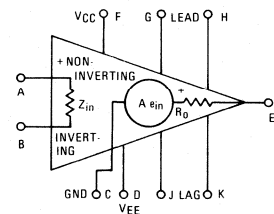
P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116
(MC1430P/MC1431P only)

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|--------------------------------------|----------------------------|----------------------|
| Power Supply Voltage MC1530, MC1531 MC1430, MC1431 | V_{CC}, V_{EE} V_{CC}, V_{EE} | +9.0, -9.0 +8.0, -8.0 | Vdc |
| Differential Input Signal | $V_{ID}(\text{max})$ | ± 5.0 | Volts |
| Load Current | I_L | 10 | mA |
| Power Dissipation (Package Limitation) | P_D | | |
| Metal Package | | 680 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 4.6 | mW/ $^\circ\text{C}$ |
| Flat Package | | 500 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 3.3 | mW/ $^\circ\text{C}$ |
| Dual In-Line Plastic Package MC1430, MC1431 | | 400 | mW |
| Derate above $+25^\circ\text{C}$ | | 3.3 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range MC1530, MC1531 MC1430, MC1431 | T_A | -55 to +125 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range Metal and Ceramic Package Plastic Package MC1430, MC1431 | T_{stg} | -65 to +175 -55 to +150 | $^\circ\text{C}$ |

CIRCUIT SCHEMATICS

FIGURE 1 – EQUIVALENT CIRCUIT
BOTH TYPES



| PIN CONNECTIONS | | | | | | | | | | |
|-----------------|---|---|---|---|----|----|----|----|---|----|
| Schematic | A | B | C | D | E | F | G | H | J | K |
| "F" & "G" Pkgs. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| "P" Package | 4 | 6 | 8 | 7 | 11 | 12 | 13 | 14 | 1 | 2 |

FIGURE 2 – MC1530/MC1430
(STANDARD INPUT)

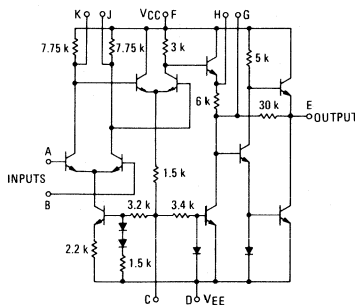
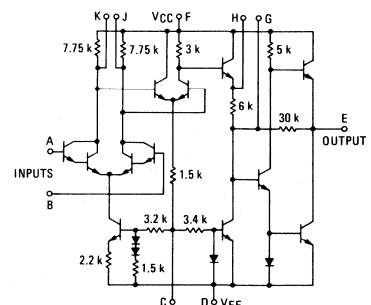


FIGURE 3 – MC1531/MC1431
(DARLINGTON INPUT)



See Packaging Information Section for outline dimensions.

MC1530, MC1531, MC1430, MC1431 (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = +6.0$ Vdc, $V_{EE} = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

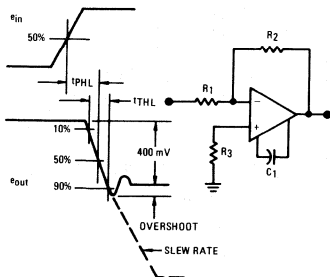
| Characteristic | Symbol* | MC1530 | | | MC1430 | | | Unit |
|--|----------------|-----------|-----------|--------|-----------|-----------|------|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | I_{IB} | — | 3.0 | 10 | — | 5.0 | 15 | μAdc |
| Input Offset Current | I_{IO} | — | 0.2 | 2.0 | — | 0.4 | 4.0 | μAdc |
| Input Offset Voltage $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ ① $T_A = T_{high}$ ① | V_{IO} | — | 1.0 | 5.0 | — | 2.0 | 10 | mVdc |
| | | — | — | 6.0 | — | — | 11 | |
| | | — | — | 6.0 | — | — | 12 | |
| Single-Ended Input Impedance (Open-Loop, $f = 30$ Hz) | z_{is} | 10 | 20 | — | 5.0 | 15 | — | k Ω |
| Common-Mode Input Voltage Swing | V_{ICR} | ± 2.0 | ± 2.7 | — | ± 2.0 | ± 2.5 | — | V _{pk} |
| Equivalent Input Noise Voltage (Open-Loop, $R_s = 50$ ohms, BW = 5.0 MHz) | e_N | — | 10 | — | — | 10 | — | $\mu\text{V(rms)}$ |
| Common-Mode Rejection Ratio ($f = 100$ Hz) | CMRR | 70 | 75 | — | 65 | 75 | — | dB |
| Open-Loop Voltage Gain, $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high} | A_{vol} | — | — | — | 3000 | 5000 | — | V/V |
| | | 4500 | 5000 | 12,500 | — | — | — | |
| Bandwidth (Open-Loop, -3.0 dB, no roll-off capacitance) | BW | 1.0 | 2.0 | — | 1.0 | 2.0 | — | MHz |
| Output Impedance ($f = 100$ Hz) | z_o | — | 25 | 50 | — | 25 | 50 | ohms |
| Output Voltage Swing ($R_L = 1.0$ k ohms) | V_O | ± 4.5 | ± 5.2 | — | ± 4.0 | ± 5.0 | — | V _{pk} |
| Power Supply Sensitivity ($R_s \leq 10$ k Ω) | PSRR | — | 100 | — | — | 100 | — | $\mu\text{V/V}$ |
| Power Supply Current | I_D^+, I_D^- | — | 9.2 | 12.5 | — | 9.2 | 12.5 | mAdc |
| DC Quiescent Power Dissipation ($V_O = 0$) | P_D | — | 110 | 150 | — | 110 | 150 | mW |

ELECTRICAL CHARACTERISTICS ($V_{CC} = +6.0$ Vdc, $V_{EE} = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol* | MC1531 | | | MC1431 | | | Unit |
|--|----------------|-----------|-----------|-------|-----------|-----------|------|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | I_{IB} | — | 0.025 | 0.150 | — | 0.1 | 0.3 | μAdc |
| Input Offset Current | I_{IO} | — | 0.003 | 0.025 | — | 0.01 | 0.1 | μAdc |
| Input Offset Voltage $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ ① $T_A = T_{high}$ ① | V_{io} | — | 3.0 | 10 | — | 5.0 | 15 | mVdc |
| | | — | — | — | — | — | 18 | |
| | | — | — | — | — | — | 16.5 | |
| Single-Ended Input Impedance (Open-Loop, $f = 30$ Hz) | z_{is} | 1000 | 2000 | — | 300 | 600 | — | k Ω |
| Common-Mode Input Voltage Swing | V_{ICR} | ± 2.0 | ± 2.4 | — | ± 2.0 | ± 2.2 | — | V _{pk} |
| Equivalent Input Noise Voltage (Open-Loop, $R_s = 50$ ohms, BW = 5.0 MHz) | e_N | — | 20 | — | — | 20 | — | $\mu\text{V(rms)}$ |
| Common-Mode Rejection Ratio ($f = 100$ Hz) | CMRR | 65 | 65 | — | 60 | 75 | — | dB |
| Open-Loop Voltage Gain $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high} | A_{vol} | — | — | — | 1500 | 3500 | — | V/V |
| | | 2500 | 3500 | 7000 | — | — | — | |
| Bandwidth (Open-Loop, -3.0 dB, no roll-off capacitance) | BW | — | 0.4 | — | — | 0.4 | — | MHz |
| Output Impedance ($f = 30$ Hz) | z_o | — | 25 | 50 | — | 25 | 50 | ohms |
| Output Voltage Swing ($R_L = 1.0$ k ohms) | V_O | ± 4.5 | ± 5.2 | — | ± 4.0 | ± 5.0 | — | V _{pk} |
| Power Supply Sensitivity ($R_s \leq 10$ k Ω) | PSRR | — | 100 | — | — | 100 | — | $\mu\text{V/V}$ |
| Power Supply Current | I_D^+, I_D^- | — | 9.2 | 12.5 | — | 9.2 | 12.5 | mAdc |
| DC Quiescent Power Dissipation ($V_O = 0$) | P_D | — | 110 | 150 | — | 110 | 150 | mW |

STEP RESPONSE, TYPICAL CHARACTERISTICS

($V_{CC} = +6.0$ Vdc, $V_{EE} = -6.0$ Vdc, $V_O = 400$ mVdc, $T_A = +25^\circ\text{C}$)



| Step Response | Symbol* | MC1530 | MC1430 | MC1531 | MC1431 | Unit |
|---|------------------|--------|--------|--------|--------|------------------|
| | | | | | | |
| Gain = 100, 0% overshoot, $R_1 = 1.0$ k ohm, $R_2 = 100$ k ohms, $R_3 = 1.0$ k ohm, $C_1 = 750$ pF | t _{THL} | 0.13 | 0.36 | 0.36 | 0.21 | μs |
| | t _{PHL} | 0.11 | 0.21 | 0.21 | 0.16 | μs |
| | SR | 33 | 16 | 16 | 16 | V/ μs |
| Gain = 10, 10% overshoot, $R_1 = 10$ k ohms, $R_2 = 100$ k ohms, $R_3 = 10$ k ohms, $C_1 = 6800$ pF | t _{THL} | 0.34 | 0.30 | 0.30 | 0.28 | μs |
| | t _{PHL} | 0.25 | 0.28 | 0.28 | 0.28 | μs |
| | SR | 6.0 | 5.5 | 5.5 | 5.5 | V/ μs |
| Gain = 1.0, 5.0% overshoot, $R_1 = 10$ k ohms, $R_2 = 10$ k ohms, $R_3 = 5.0$ k ohms, $C_1 = 33,000$ pF | t _{THL} | 0.28 | 0.37 | 0.37 | 0.17 | μs |
| | t _{PHL} | 0.16 | 0.17 | 0.17 | 0.17 | μs |
| | SR | 1.7 | 1.4 | 1.4 | 1.4 | V/ μs |

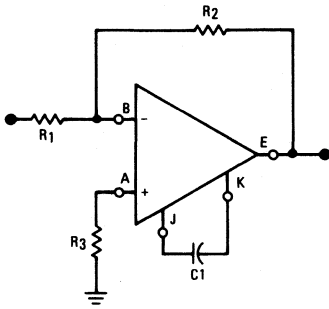
① T_{low} : 0°C for MC1430
 -55°C for MC1530
 T_{high} : $+75^\circ\text{C}$ for MC1430
 $+125^\circ\text{C}$ for MC1530

T_{low} : 0°C for MC1431
 -55°C for MC1531
 T_{high} : $+75^\circ\text{C}$ for MC1431
 $+125^\circ\text{C}$ for MC1531

*Symbols used conform to JEDEC Engineering Bulletin No. 1 where applicable.

MC1530, MC1531, MC1430, MC1431 (continued)

FIGURE 4 – TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS

($V_{CC} = +6.0$ Vdc, $V_{EE} = -6.0$ Vdc, $T_A = +25^\circ\text{C}$)

| FIG. NO. | CURVE NO. | VOLTAGE GAIN | DEVICE NO. | TEST CONDITIONS | | | |
|----------|-----------|--------------|------------------------------|------------------------------|------------------------------|-----------------------------|---------------------|
| | | | | R ₁ (k Ω) | R ₂ (k Ω) | R ₃ (Ω) | C ₁ (pF) |
| 5 | 1,2 | 100 | MC1530/MC1430, MC1531/MC1431 | 1.0 | 100 | 1.0 k | 750 |
| | 3 | 10 | MC1530/MC1430, MC1531/MC1431 | 10 | 100 | 10 k | 6800 |
| | 4 | 1 | MC1530/MC1430, MC1531/MC1431 | 10 | 10 | 5.0 k | 33,000 |
| 6 | 1 | 100 | MC1530/MC1430 | 1.0 | 100 | 1.0 k | 750 |
| | 2 | 10 | MC1530/MC1430 | 10 | 100 | 10 k | 6800 |
| | 3 | 10 | MC1530/MC1430 | 1.0 | 10 | 1.0 k | 6800 |
| | 4 | 1 | MC1530/MC1430 | 10 | 10 | 5.0 k | 33,000 |
| | 5 | 1 | MC1530/MC1430 | 1.0 | 1.0 | 500 | 33,000 |
| 7 | 1 | 100 | MC1531/MC1431 | 1.0 | 100 | 1.0 k | 750 |
| | 2 | 10 | MC1531/MC1431 | 10 | 100 | 10 k | 6800 |
| | 3 | 1 | MC1531/MC1431 | 10 | 10 | 5.0 k | 33,000 |
| 8 | 1 | AVOL | MC1530/MC1430 | 0 | = | 0 | 0 |
| | 2 | AVOL | MC1530/MC1430 | 0 | = | 0 | 750 |
| | 3 | AVOL | MC1530/MC1430 | 0 | = | 0 | 6800 |
| | 4 | AVOL | MC1530/MC1430 | 0 | = | 0 | 33,000 |
| 9 | 1 | AVOL | MC1531/MC1431 | 0 | = | 0 | 0 |
| | 2 | AVOL | MC1531/MC1431 | 0 | = | 0 | 750 |
| | 3 | AVOL | MC1531/MC1431 | 0 | = | 0 | 6800 |
| | 4 | AVOL | MC1531/MC1431 | 0 | = | 0 | 33,000 |

FIGURE 5 – LARGE SIGNAL SWING versus FREQUENCY

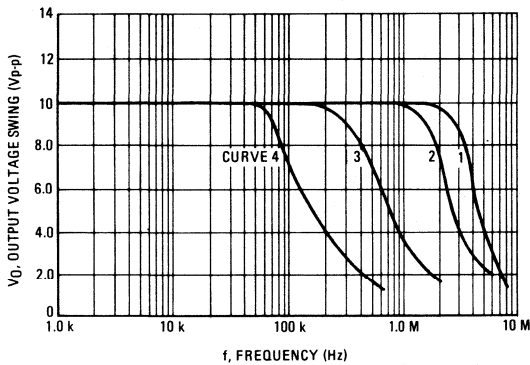


FIGURE 6 – MC1530/MC1430 VOLTAGE GAIN versus FREQUENCY

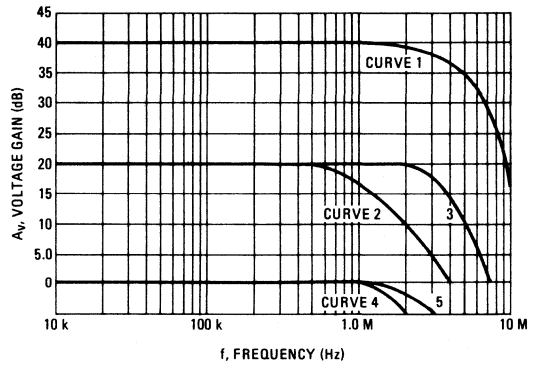


FIGURE 7 – MC1531/MC1431 VOLTAGE GAIN versus FREQUENCY

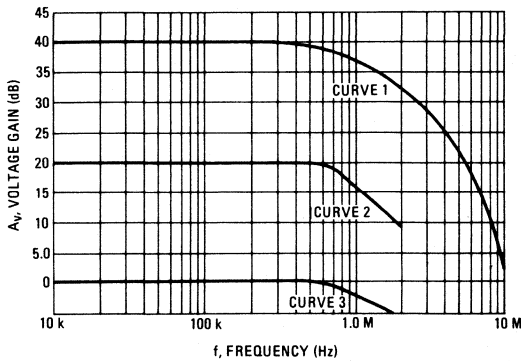
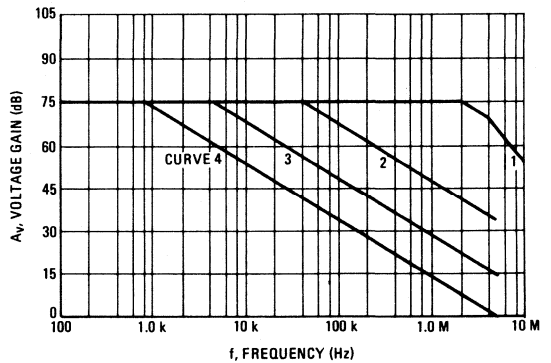


FIGURE 8 – MC1530/MC1430 OPEN LOOP VOLTAGE GAIN versus FREQUENCY



7

MC1530, MC1531, MC1430, MC1431 (continued)

FIGURE 9 – MC1531/MC1431 OPEN LOOP VOLTAGE GAIN versus FREQUENCY

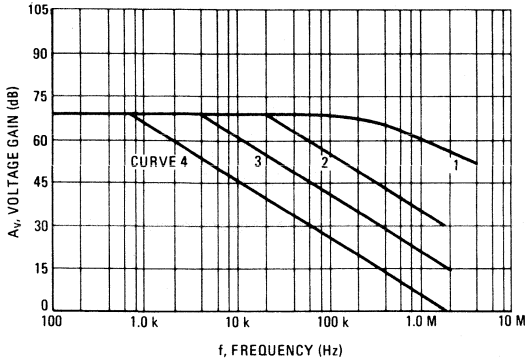


FIGURE 10 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

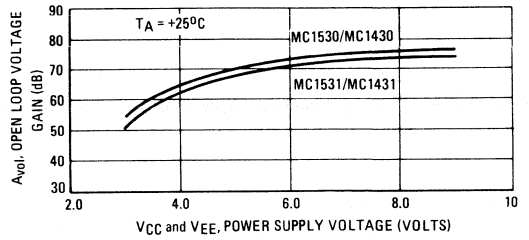


FIGURE 11 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

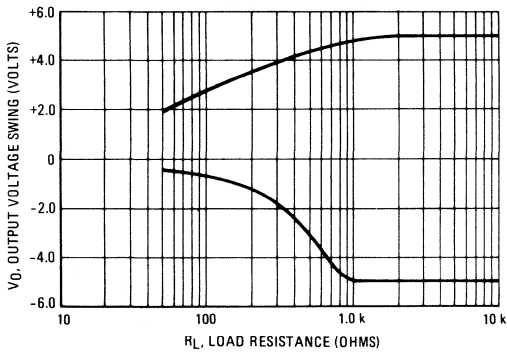


FIGURE 12 – COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

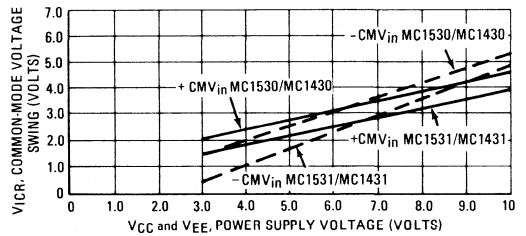
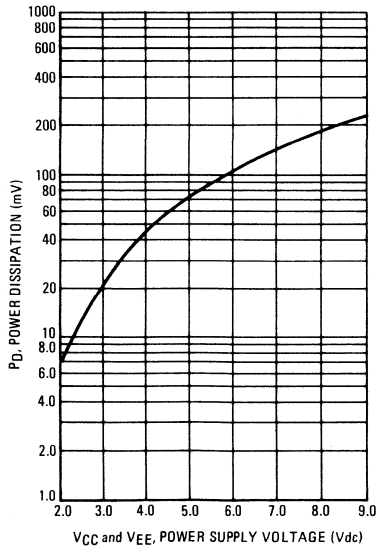
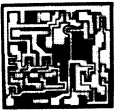


FIGURE 13 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



**MC1533
MC1433**

**MONOLITHIC OPERATIONAL
AMPLIFIER**



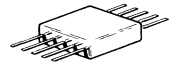
... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics
AVOL = 60,000 typical
- Low Temperature Drift – $\pm 5 \mu\text{V}/^\circ\text{C}$
- Large Output Voltage Swing –
 $\pm 13 \text{ V}$ typical @ $\pm 15 \text{ V}$ Supply
- Low Output Impedance – $Z_{\text{out}} = 100 \text{ ohms}$ typical

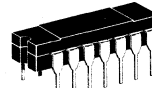
**OPERATIONAL AMPLIFIER
MONOLITHIC SILICON
INTEGRATED CIRCUIT**



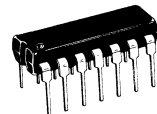
G SUFFIX
METAL PACKAGE
CASE 602B



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116

(MC1433P Only)

FIGURE 1 – CIRCUIT SCHEMATIC

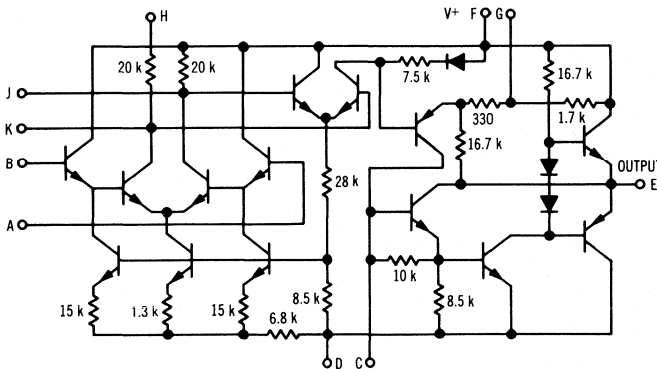
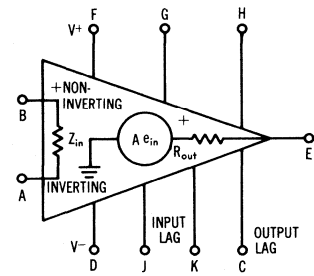


FIGURE 2 – EQUIVALENT CIRCUIT



PIN CONNECTIONS

| Schematic | A | B | C | D | E | F | G | H | J | K |
|--------------------|----|---|---|---|----|----|----|----|---|----|
| "G" Package | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| "F" Package | 10 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| "L" & "P" Packages | 4 | 5 | 6 | 7 | 11 | 12 | 13 | 14 | 2 | 3 |

See Packaging Information Section for outline dimensions.

MC1533, MC1433 (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MC1533 | | | MC1433 | | | Unit |
|---|--------------------------------------|----------------------|----------------------|--------------------|----------------------|----------------------|----------------------|--|
| | | Min | Typ | Max | Min | Typ | Max | |
| Open Loop Voltage Gain ($T_A = +25^\circ\text{C}$) ($T_A = T_{low}$ ① to T_{high} ①) | A_{VOL} | 40,000 35,000 | 60,000 50,000 | — — | 30,000 20,000 | 60,000 50,000 | — — | — |
| Output Impedance ($f = 20$ Hz) | Z_{out} | — | 100 | 150 | — | 100 | 150 | Ω |
| Input Impedance ($f = 20$ Hz) | Z_{in} | 500 | 1000 | — | 300 | 600 | — | k Ω |
| Output Voltage Swing ($R_L = 10$ k Ω) ($R_L = 2$ k Ω) | V_o | ± 12 ± 11 | ± 13 ± 12 | — — | ± 12 ± 10 | ± 13 ± 12 | — — | V_{peak} |
| Input Common Mode Voltage Swing | CMV_{in} | +9.0 -8.0 | +10 -9.0 | — — | +8.0 -8.0 | +9.0 -9.0 | — — | V_{peak} |
| Common Mode Rejection Ratio | CM_{rej} | 90 | 100 | — | 80 | 100 | — | dB |
| Input Bias Current ($T_A = +25^\circ\text{C}$) ($T_A = T_{low}$) | I_b | — — | 0.5 — | 1.0 3.0 | — — | 0.5 — | 2.0 4.0 | μA |
| Input Offset Current ($T_A = +25^\circ\text{C}$) ($T_A = T_{low}$) ($T_A = T_{high}$) | $ I_{io} $ | — — — | 0.03 — — | 0.15 0.5 0.2 | — — — | 0.1 — — | 0.50 0.75 0.75 | μA |
| Input Offset Voltage ② ($T_A = +25^\circ\text{C}$) ($T_A = T_{low}, T_{high}$) | $ V_{io} $ | — — | 1.0 — | 5.0 6.0 | — — | 1.0 — | 7.5 10 | mV |
| Step Response ($C_2 = 10$ pF) { Gain = 100, 10% overshoot, $R_1 = 10$ k Ω , $R_2 = 1.0$ M Ω , $R_3 = 100$ Ω , $C_1 = 0.01$ μF } | t_f t_{pd} dV_{out}/dt ③ | — — — | 0.25 0.1 6.2 | — — — | — — — | 0.25 0.1 6.2 | — — — | μs μs V/ μs |
| { Gain = 10, no overshoot, $R_1 = 10$ k Ω , $R_2 = 100$ k Ω , $R_3 = 10$ Ω , $C_1 = 0.1$ μF } | t_f t_{pd} dV_{out}/dt ③ | — — — | 0.3 0.1 2.9 | — — — | — — — | 0.3 0.1 2.9 | — — — | μs μs V/ μs |
| { Gain = 1, 5% overshoot, $R_1 = 10$ k Ω , $R_2 = 10$ k Ω , $R_3 = 10$ Ω , $C_1 = 1.0$ μF } | t_f t_{pd} dV_{out}/dt ③ | — — — | 0.2 0.1 2.0 | — — — | — — — | 0.2 0.1 2.0 | — — — | μs μs V/ μs |
| Average Temperature Coefficient of Input Offset Voltage ($T_A = T_{low}$ to $+25^\circ\text{C}$) ($T_A = +25^\circ\text{C}$ to T_{high}) | $ TC_{V_{io}} $ | — — | 8.0 5.0 | — — | — — | 10 8.0 | — — | $\mu\text{V}/^\circ\text{C}$ |
| Average Temperature Coefficient of Input Offset Current ($T_A = T_{low}$ to T_{high}) ($T_A = +25^\circ\text{C}$ to T_{high}) | $ TC_{I_{io}} $ | — — | 0.1 0.05 | — — | — — | 0.1 0.05 | — — | nA/ $^\circ\text{C}$ |
| DC Power Dissipation (Power Supply = ± 15 V, $V_o = 0$) | P_D | — | 125 | 170 | — | 125 | 240 | mW |
| Positive Supply Sensitivity (V^- constant) | S^+ | — | 50 | 150 | — | 50 | 200 | $\mu\text{V}/\text{V}$ |
| Negative Supply Sensitivity (V^+ constant) | S^- | — | 50 | 150 | — | 50 | 200 | $\mu\text{V}/\text{V}$ |

① $T_{high} = +75^\circ\text{C}$ for MC1433,
+125 $^\circ\text{C}$ for MC1533

$T_{low} = 0$ for MC1433
-55 $^\circ\text{C}$ for MC1533

② Input offset voltage (V_{io}) may be adjusted to zero.
③ $dV_{out}/dt =$ Slew Rate

MC1533, MC1433 (continued)

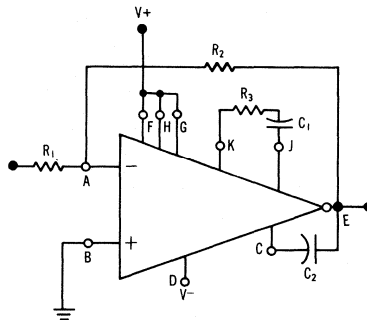
MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit | |
|--|----------------|----------------------|----------------------|-----|
| Power Supply Voltage | MC1533, MC1433 | V^+ | +20, +18 | Vdc |
| | MC1533, MC1433 | V^- | -20, -18 | Vdc |
| Differential Input Signal | V_{in} | ± 10 | Volts | |
| Common Mode Input Swing | CMV_{in} | $\pm V^+$ | Volts | |
| Load Current | I_L | 10 | mA | |
| Output Short Circuit Duration | t_S | 1.0 | s | |
| Power Dissipation (Package Limitation) | P_D | | | |
| Metal Package | | 680 | mW | |
| Derate above $T_A = +25^\circ\text{C}$ | | 4.6 | mW/ $^\circ\text{C}$ | |
| Flat Package | | 500 | mW | |
| Derate above $T_A = +25^\circ\text{C}$ | | 3.3 | mW/ $^\circ\text{C}$ | |
| Dual In-Line Ceramic Package | | 625 | mW | |
| Derate above $T_A = +25^\circ\text{C}$ | 5.0 | mW/ $^\circ\text{C}$ | | |
| Dual In-Line Plastic Package | 400 | mW | | |
| Derate above $T_A = +25^\circ\text{C}$ | 3.3 | mW/ $^\circ\text{C}$ | | |
| Operating Temperature Range | T_A | | $^\circ\text{C}$ | |
| MC1533 | | -55 to +125 | | |
| MC1433 | 0 to +75 | | | |
| Storage Temperature Range | T_{stg} | | $^\circ\text{C}$ | |
| Metal and Ceramic Packages | | -65 to +150 | | |
| Plastic Package | -65 to +125 | | | |

TYPICAL CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT

$V^+ = +15\text{ Vdc}$, $V^- = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$



| Fig. No. | Curve No. | Test Conditions | | | | |
|----------|-----------|--------------------|--------------------|--------------------|-------------------------|-------------------------|
| | | R_1 (Ω) | R_2 (Ω) | R_3 (Ω) | C_1 (μF) | C_2 (μF) |
| 4 | 1 | 10 k | 10 k | 10 | 1.0 | 10 |
| | 2 | 10 k | 100 k | 10 | 0.1 | 10 |
| | 3 | 10 k | 1.0 M | 100 | 0.01 | 10 |
| | 3 | 1.0 k | 1.0 M | 390 | 0.002 | 10 |
| 5 | 1 | 10 k | 10 k | 10 | 1.0 | 10 |
| | 2 | 10 k | 100 k | 10 | 0.1 | 10 |
| | 3 | 10 k | 1.0 M | 100 | 0.01 | 10 |
| | 4 | 1.0 k | 1.0 M | 390 | 0.002 | 10 |
| 6 | 1 | 0 | ∞ | 10 | 1.0 | 10 |
| | 2 | 0 | ∞ | 10 | 0.1 | 10 |
| | 3 | 0 | ∞ | 100 | 0.01 | 10 |
| | 4 | 0 | ∞ | 390 | 0.002 | 10 |

TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 4 – LARGE-SIGNAL SWING versus FREQUENCY

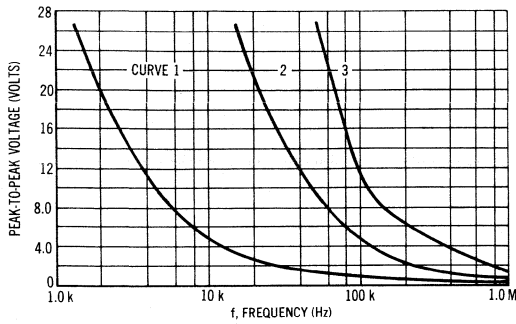


FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

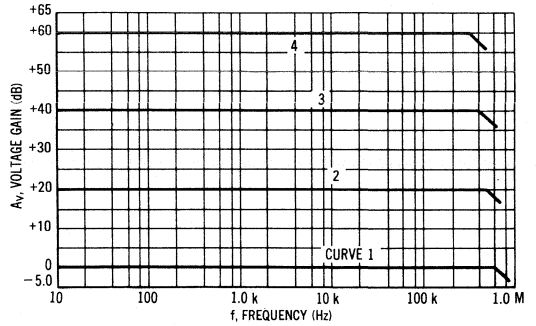


FIGURE 6 – OFFSET ADJUST CIRCUIT

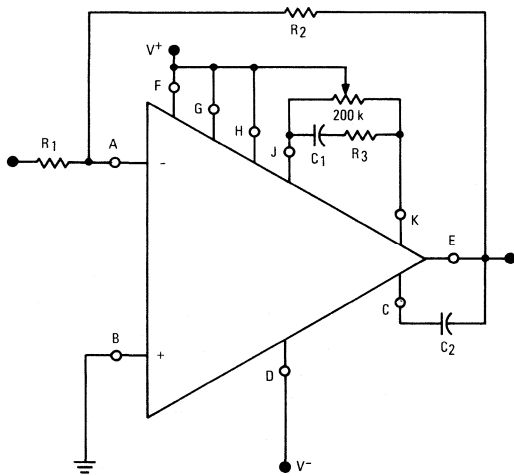
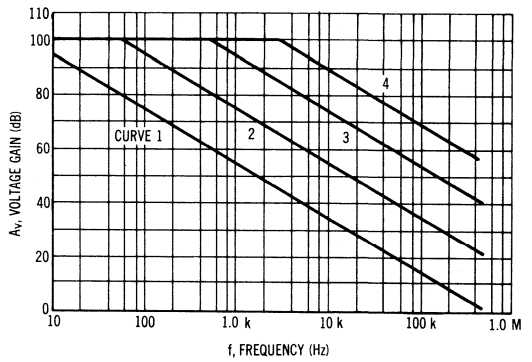


FIGURE 7 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY (HIGH GAIN CONFIGURATION)



PIN CONNECTIONS

| Schematic | A | B | C | D | E | F | G | H | J | K |
|--------------------|----|---|---|---|----|----|----|----|---|----|
| "G" Package | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| "F" Package | 10 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| "L" & "P" Packages | 4 | 5 | 6 | 7 | 11 | 12 | 13 | 14 | 2 | 3 |

TYPICAL CHARACTERISTICS (continued)

FIGURE 8 — POWER DISSIPATION versus POWER SUPPLY VOLTAGE

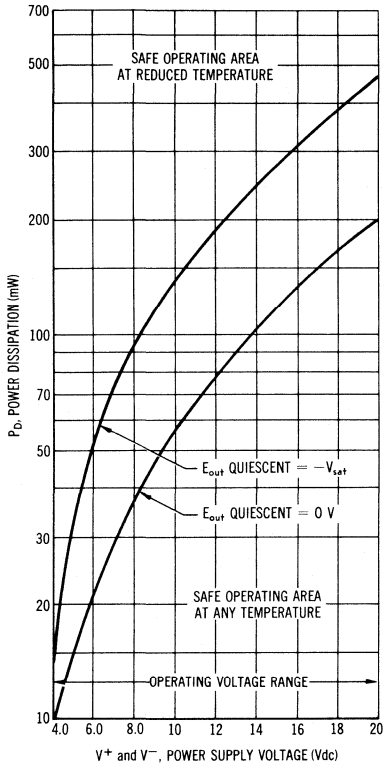


FIGURE 9 — VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

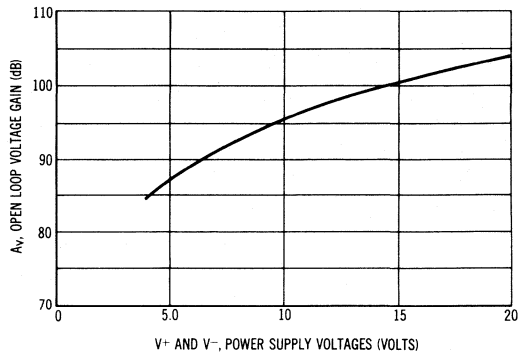


FIGURE 10 — COMMON MODE SWING versus POWER SUPPLY VOLTAGE

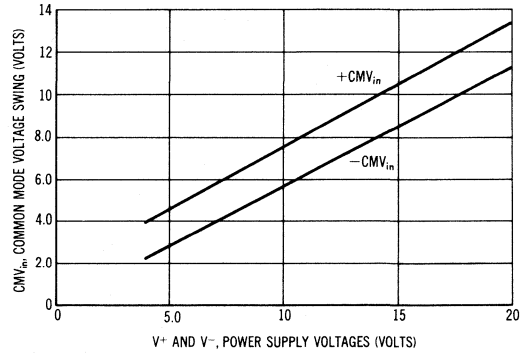
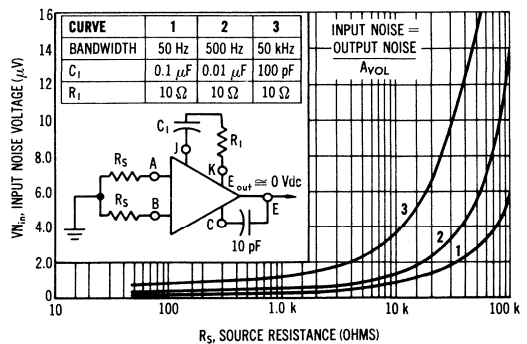


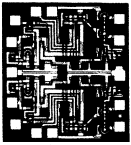
FIGURE 11 — INPUT NOISE VOLTAGE versus SOURCE RESISTANCE



MC1535 MC1435

OPERATIONAL AMPLIFIERS

MONOLITHIC DUAL OPERATIONAL AMPLIFIERS

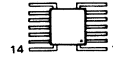


... designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

- High Open Loop Gain Characteristics — $A_{VOL} = 7,000$
- Low Temperature Drift — $\pm 10 \mu\text{V}/^\circ\text{C}$
- Low Input Offset Voltage — 1.0mV
- Low Input Noise Voltage — $0.5\mu\text{V}$

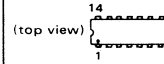
MONOLITHIC DUAL OPERATIONAL AMPLIFIERS INTEGRATED CIRCUIT EPITAXIAL PASSIVATED



F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86



(bottom view)



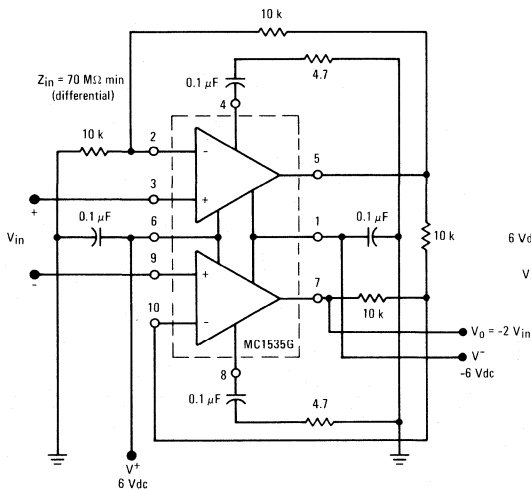
(top view)

G SUFFIX
METAL PACKAGE
CASE 602B

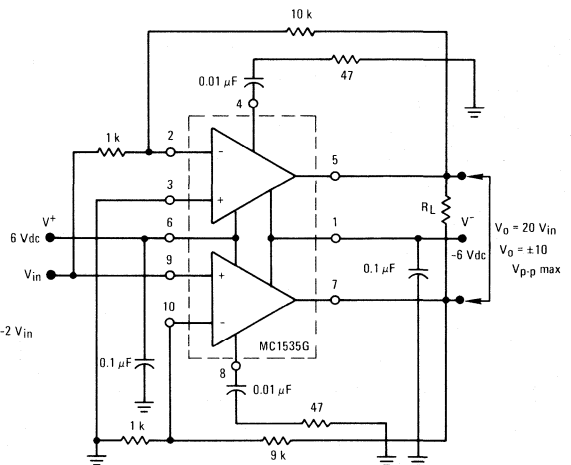


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

HIGH Z_{in} , DIFFERENTIAL TO SINGLE-ENDED AMPLIFIER

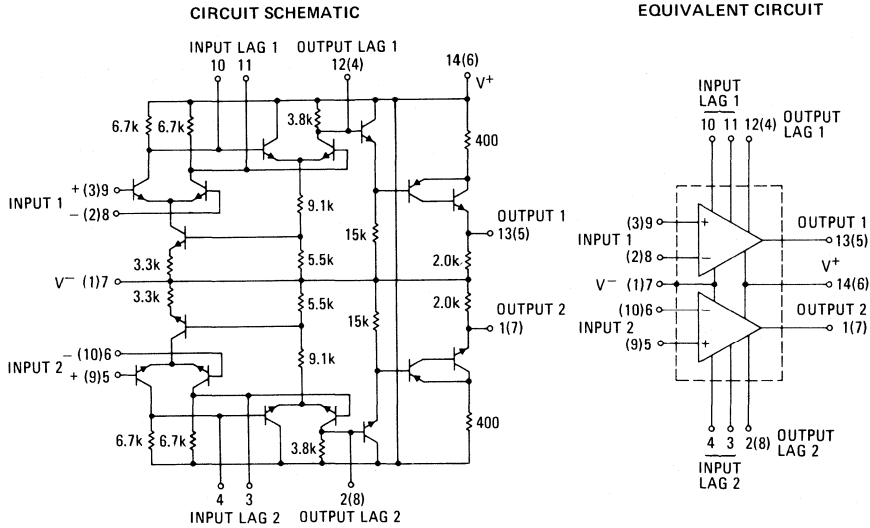


LARGE OUTPUT SWING CONFIGURATION (FLOATING LOAD)



See Packaging Information Section for outline dimensions.

MC1535, MC1435 (continued)



Number at end of terminal is pin number for ceramic packages.
 Number in parenthesis is pin number for metal package. Input Lag available only in ceramic packages.

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | MC1535 | MC1435 | Unit |
|--|------------------|-------------|--------------|----------------------------|
| Power Supply Voltage | V^+ V^- | +10 -10 | +9.0 -9.0 | Vdc |
| Differential Input Signal | V_{in} | ± 5.0 | ± 5.0 | Volts |
| Common-Mode Input Swing | CMV_{in} | +5.0 -4.0 | +5.0 -4.0 | Volts |
| Load Current | I_L | 20 | 20 | mA |
| Output Short Circuit Duration | T_{SC} | Continuous | | |
| Power Dissipation (Package Limitation) | P_D | | | |
| Flat Ceramic Package Derate above $T_A = +25^\circ\text{C}$ | MC1535F, MC1435F | 500 | 3.3 | mW mW/ $^\circ\text{C}$ |
| Metal Package Derate above $T_A = +25^\circ\text{C}$ | MC1535G, MC1435G | 680 | 4.6 | mW mW/ $^\circ\text{C}$ |
| Ceramic Dual In-Line Package Derate above $T_A = +25^\circ\text{C}$ | MC1435L | 625 | 5.0 | mW mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | -65 to +150 | $^\circ\text{C}$ |

MC1535, MC1435 (continued)

ELECTRICAL CHARACTERISTICS (Each Amplifier) ($V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristics | Symbol | MC1535 | | | MC1435 | | | Unit |
|--|--|--------------|---|--------------|--------------|---|----------|--|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current $I_b = \frac{I_1 + I_2}{2}$, $T_A = +25^\circ\text{C}$ $I_b = T_{low}$ to T_{high} ① | I_b | — | 1.2 | 3.0 | — | 1.2 | 5.0 | μAdc |
| Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = +25^\circ\text{C}$ to T_{high} $T_A = T_{low}$ to $+25^\circ\text{C}$ | $ I_{io} $ | — | 50 | 300 | — | 50 | 500 | nAdc |
| Input Offset Voltage $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high} | $ V_{io} $ | — | 1.0 | 3.0 | — | 1.0 | 5.0 | mVdc |
| Differential Input Impedance (Open-Loop, $f = 20$ Hz) Parallel Input Resistance Parallel Input Capacitance | R_p C_p | 10 | 45 | — | 10 | 45 | — | kohms pF |
| Common-Mode Input Impedance ($f = 20$ Hz) | Z_{in} | — | 250 | — | — | 250 | — | Meg ohms |
| Common-Mode Input Voltage Swing | CMV_{in} | +3.0 -2.0 | +3.9 -2.7 | — | +3.0 -2.0 | +3.9 -2.7 | — | Vpk |
| Equivalent Input Noise Voltage ($A_V = 100$, $R_s = 10$ kohms, $f = 1.0$ kHz, $BW = 1.0$ Hz) | e_n | — | 45 | — | — | 45 | — | $nV/(\text{Hz})^{1/2}$ |
| Common-Mode Rejection Ratio ($f = 100$ Hz) | CM_{rej} | -70 | -90 | — | -70 | -90 | — | dB |
| Open Loop Voltage Gain ($T_A = T_{low}$ to T_{high}) | A_{VOL} | 4,000 | 7,000 | 10,000 | 3,500 | 7,000 | — | V/V |
| Power Bandwidth ($A_V = 1$, $R_L = 2.0$ kohms, $\text{THD} \leq 5\%$, $V_O = 20$ Vp-p) | P_{BW} | — | 40 | — | — | 40 | — | kHz |
| Unity Gain Crossover Frequency (open-loop) | | — | 1.0 | — | — | 1.0 | — | MHz |
| Phase Margin (open-loop, unity gain) | | — | 75 | — | — | 75 | — | degrees |
| Gain Margin | | — | 18 | — | — | 18 | — | dB |
| Step Response { Gain = 100, 30% overshoot, R1 = 4.7 k Ω , R2 = 470 k Ω , R3 = 150 Ω , C1 = 1,000 pF Gain = 10, 10% overshoot, R1 = 47 k Ω , R2 = 470 k Ω , R3 = 47 Ω , C1 = 0.01 μF Gain = 1, 5% overshoot, R1 = 47 k Ω , R2 = 47 k Ω , R3 = 4.7 Ω , C1 = 0.1 μF | t_f t_{pd} dV_{out}/dt ② t_f t_{pd} dV_{out}/dt ② t_f t_{pd} dV_{out}/dt ② | — | 0.3 0.1 0.167 1.9 0.3 0.111 27 0.25 0.013 | — | — | 0.3 0.1 0.167 1.9 0.3 0.111 27 0.25 0.013 | — | μs μs V/ μs μs μs V/ μs μs μs V/ μs |
| Output Impedance ($f = 20$ Hz) | Z_{out} | — | 1.7 | — | — | 1.7 | — | kohms |
| Short-Circuit Output Current | I_{SC} | — | ± 17 | — | — | ± 17 | — | mAdc |
| Output Voltage Swing ($R_L = 2.0$ kohms) | V_O | ± 2.5 | ± 2.8 | — | ± 2.3 | ± 2.7 | — | Vp |
| Power Supply Sensitivity $V^- = \text{constant}$, $R_s \leq 10$ kohms $V^+ = \text{constant}$, $R_s \leq 10$ kohms | S+ S- | — | 50 100 | — | — | 50 100 | — | $\mu\text{V/V}$ |
| Power Supply Current (Total) | I_{D^+} I_{D^-} | — | 8.3 8.3 | 12.5 12.5 | — | 8.3 8.3 | 15 15 | mAdc |
| DC Quiescent Power Dissipation (Total) ($V_O = 0$) | P_D | — | 100 | 150 | — | 100 | 180 | mW |

MATCHING CHARACTERISTICS

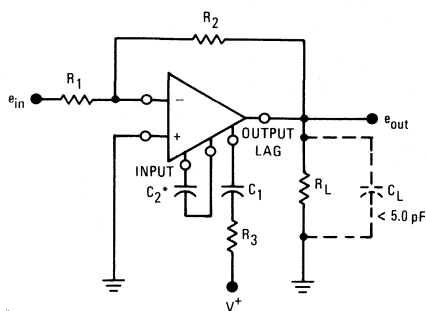
| | | | | | | | | |
|---|-------------------------------|---|------------|---|---|------------|---|------------------------------|
| Open Loop Voltage Gain | $A_{VOL1} - A_{VOL2}$ | — | ± 1.0 | — | — | ± 1.0 | — | dB |
| Input Bias Current | $I_{b1} - I_{b2}$ | — | ± 0.15 | — | — | ± 0.15 | — | μA |
| Input Offset Current | $I_{io1} - I_{io2}$ | — | ± 0.02 | — | — | ± 0.02 | — | μA |
| Average Temperature Coefficient | $TC_{I_{io1}} - TC_{I_{io2}}$ | — | ± 0.1 | — | — | ± 0.1 | — | nA/ $^\circ\text{C}$ |
| Input Offset Voltage | $V_{io1} - V_{io2}$ | — | ± 0.1 | — | — | ± 0.1 | — | mV |
| Average Temperature Coefficient | $TC_{V_{io1}} - TC_{V_{io2}}$ | — | ± 0.5 | — | — | ± 0.5 | — | $\mu\text{V}/^\circ\text{C}$ |
| Channel Separation (See Fig. 10) ($f = 10$ kHz) | e_{out1} e_{out2} | — | -60 | — | — | -60 | — | dB |

① T_{low} : 0°C for MC1435
 -55°C for MC1535
 T_{high} : $+75^\circ\text{C}$ for MC1435
 $+125^\circ\text{C}$ for MC1535

② $dV_{out}/dt = \text{Slew Rate}$

TYPICAL OUTPUT CHARACTERISTICS
 ($V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = +25^\circ\text{C}$)

FIGURE 1 – TEST CIRCUIT



*Ceramic packages only.

| FIGURE NO. | CURVE NO. | VOLTAGE GAIN | TEST CONDITIONS | | | | | OUTPUT NOISE (mV rms) |
|------------|-----------|----------------|-----------------|---------------|------------------|---------------|------------------|-----------------------|
| | | | $R_1(\Omega)$ | $R_2(\Omega)$ | $C_1(\text{pF})$ | $R_3(\Omega)$ | $C_2(\text{pF})$ | |
| 2 | 3 | 1 or 1 | 47 k | 47 k | 100,000 | 4.7 | 0 | 0.12 |
| | | | 47 k | 47 k | 0 | ∞ | 50,000 | 0.46 |
| 3 | 1 | 100 or 100 | 4.7 k | 470 k | 1,000 | 150 | 0 | 1.7 |
| | | | 4.7 k | 470 k | 0 | ∞ | 510 | 2.1 |
| | 2 | 10 or 10 | 47 k | 470 k | 10,000 | 47 | 0 | 1.0 |
| | | | 47 k | 470 k | 0 | ∞ | 5,000 | 2.1 |
| | 3 | 1 or 1 | 47 k | 47 k | 100,000 | 4.7 | 0 | 0.12 |
| | | | 47 k | 47 k | 0 | ∞ | 50,000 | 0.46 |
| 4 | 1 | AVOL or 100 | 100 | ∞ | 1,000 | 150 | 0 | 8.1 |
| | | | 100 | ∞ | 0 | ∞ | 510 | 8.1 |
| | 2 | AVOL or 100 | 100 | ∞ | 10,000 | 47 | 0 | 5.5 |
| | | | 100 | ∞ | 0 | ∞ | 5,000 | 5.5 |
| | 3 | AVOL or 100 | 100 | ∞ | 100,000 | 4.7 | 0 | 4.4 |
| | | | 100 | ∞ | 0 | ∞ | 50,000 | 4.4 |

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY

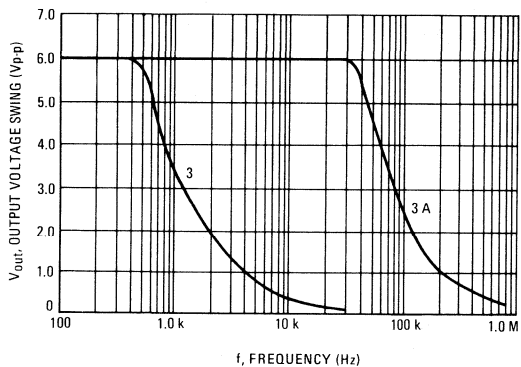


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

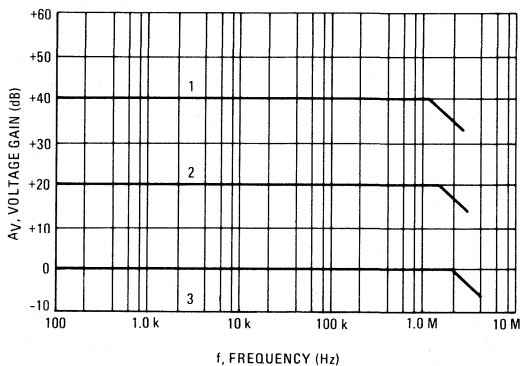


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

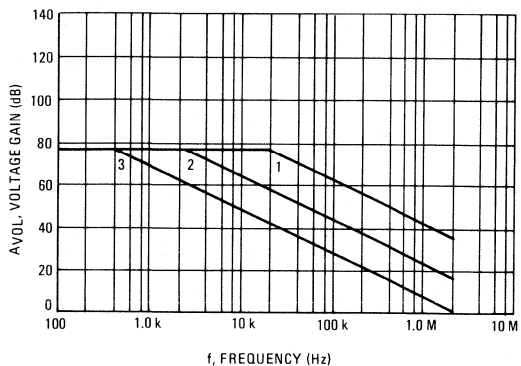
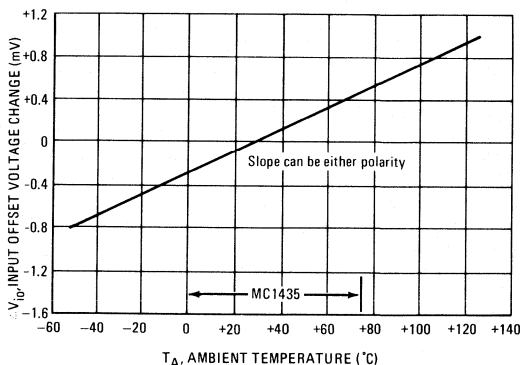


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE



7

FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

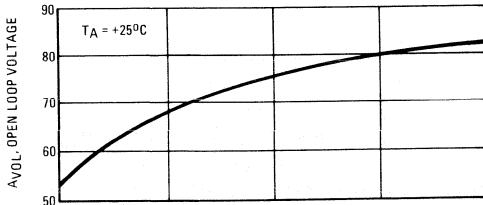


FIGURE 7 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

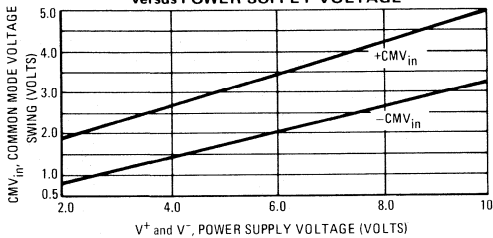


FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

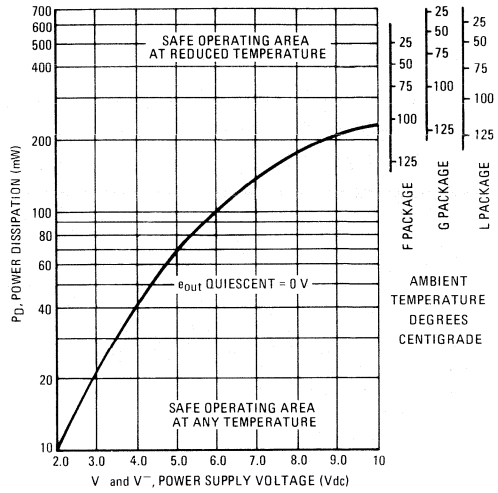


FIGURE 9 – OUTPUT WIDEBAND NOISE VOLTAGE versus SOURCE RESISTANCE

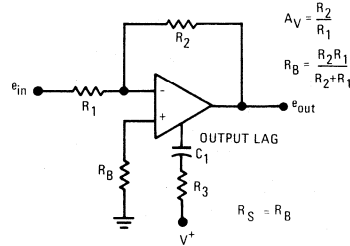
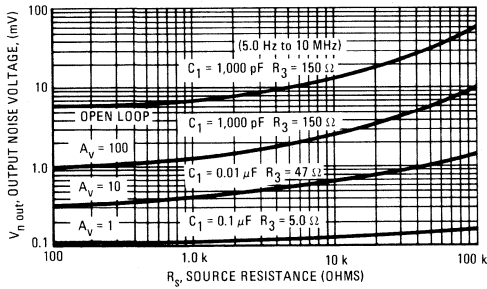
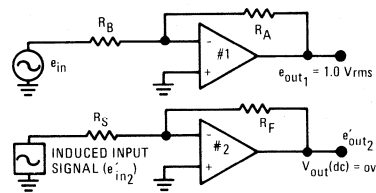
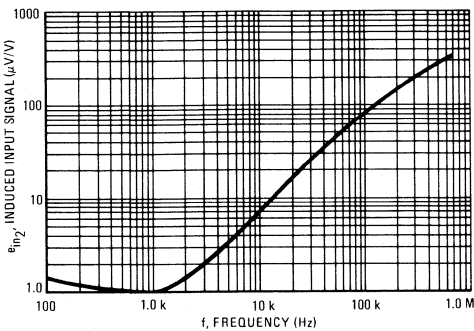


FIGURE 10 – INDUCED INPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY



Induced input signal (μV of induced input signal in amplifier #2 per volt of output signal at amplifier #1)

$e'_{out2} = e'_{in2} \left(\frac{R_F}{R_S} \right)$, where e_{out2} is the component of e_{out2} due only to lack of perfect separation between the two amplifiers.

MC1536G MC1436G MC1436CG

OPERATIONAL AMPLIFIER

HIGH VOLTAGE, INTERNALLY COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Maximum Supply Voltage – ± 40 Vdc (MC1536G)
- Output Voltage Swing –
 ± 30 V_{pk}(min) ($V^+ = +36$ V, $V^- = -36$ V) (MC1536G)
 ± 22 V_{pk}(min) ($V^+ = +28$ V, $V^- = -28$ V)
- Input Bias Current – 20 nA max (MC1536G)
- Input Offset Current – 3.0 nA max (MC1536G)
- Fast Slew Rate – 2.0 V/ μ s typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Over-Voltage Protection
- AVOL – 500,000 typ
- Characteristics Independent of Power Supply Voltages –
 $(\pm 5.0$ Vdc to ± 36 Vdc)

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED

METAL PACKAGE

CASE 601

TO-99



(bottom view)

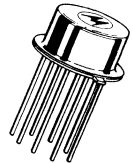


FIGURE 1 – DIFFERENTIAL AMPLIFIER WITH ± 20 V
COMMON-MODE INPUT VOLTAGE RANGE

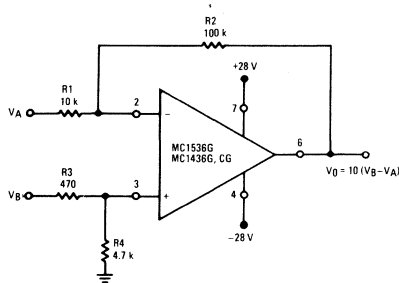


FIGURE 2 – VOLTAGE CONTROLLED CURRENT
SOURCE or TRANSCONDUCTANCE AMPLIFIER
WITH 0 TO 40 V COMPLIANCE

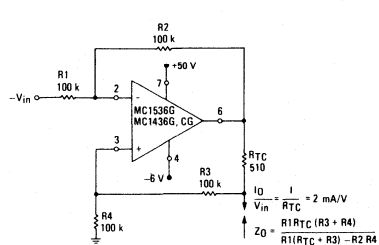


FIGURE 3 – TYPICAL NON-INVERTING X10
VOLTAGE AMPLIFIER

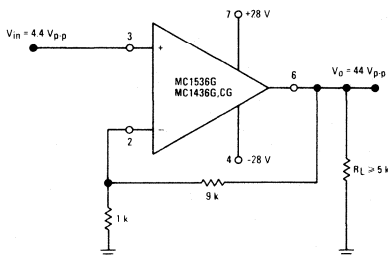
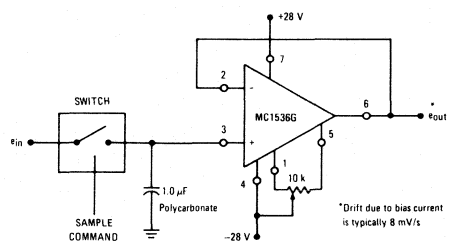


FIGURE 4 – LOW-DRIFT SAMPLE AND HOLD



*Drift due to bias current is typically 8 mV/s

See Packaging Information Section for outline dimensions.
See current MCC1536/1436 data sheet for standard linear chip information.

MC1536G, MC1436G, MC1436CG (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | MC1536G | MC1436G | MC1436CG | Unit |
|---|-------------------|---|----------|----------|-------|
| Power Supply Voltage | V ⁺ | +40 | +34 | +30 | Vdc |
| | V ⁻ | -40 | -34 | -30 | |
| Differential Input Signal | V _{in} | ±(V ⁺ + V ⁻ -3) | | | Volts |
| Common-Mode Input Swing | CMV _{in} | +V ⁺ , -(V ⁻ -3) | | | Volts |
| Output Short Circuit Duration (V ⁺ = V ⁻ = 28 Vdc, V _O = 0) | T _{SC} | 5.0 | | | s |
| Power Dissipation (Package Limitation) Derate above T _A = +25°C | P _D | 680 | | | mW |
| | | 4.6 | | | |
| Operating Temperature Range | T _A | -55 to +150 | 0 to +75 | | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | | | °C |

ELECTRICAL CHARACTERISTICS (V⁺ = +28 Vdc, V⁻ = -28 Vdc, T_A = +25°C unless otherwise noted)

| Characteristics | Symbol | MC1536G | | | MC1436G | | | MC1436CG | | | Unit |
|--|--|---------|---------|-----|---------|---------|-----|----------|---------|-----|------------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current T _A = +25°C T _A = T _{low} to T _{high} (See Note 1) | I _b | — | 8.0 | 20 | — | 15 | 40 | — | 25 | 90 | nAdc |
| | | — | — | 35 | — | — | 55 | — | — | — | |
| Input Offset Current T _A = +25°C T _A = +25°C to T _{high} T _A = T _{low} to +25°C | I _{io} | — | 1.0 | 3.0 | — | 5.0 | 10 | — | 10 | 25 | nAdc |
| | | — | — | 4.5 | — | — | 14 | — | — | — | |
| | | — | — | 7.0 | — | — | 14 | — | — | — | |
| Input Offset Voltage T _A = +25°C T _A = T _{low} to T _{high} | V _{io} | — | 2.0 | 5.0 | — | 5.0 | 10 | — | 5.0 | 12 | mVdc |
| | | — | — | 7.0 | — | — | 14 | — | — | — | |
| Differential Input Impedance (Open-Loop, f ≤ 5.0 Hz) Parallel Input Resistance Parallel Input Capacitance | R _p C _p | — | 10 | — | — | 10 | — | — | 10 | — | Meg ohms pF |
| | | — | 2.0 | — | — | 2.0 | — | — | 2.0 | — | |
| Common-Mode Input Impedance (f ≤ 5.0 Hz) | Z _(in) | — | 250 | — | — | 250 | — | — | 250 | — | Meg ohms |
| Common-Mode Input Voltage Swing | CMV _{in} | ±24 | ±25 | — | ±22 | ±25 | — | ±18 | ±20 | — | V _{pk} |
| Equivalent Input Noise Voltage (A _V = 100, R _s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz) | e _n | — | 50 | — | — | 50 | — | — | 50 | — | nV/(Hz) ^{1/2} |
| Common-Mode Rejection Ratio (dc) | CM _{rej} | 80 | 110 | — | 70 | 110 | — | 50 | 90 | — | dB |
| Large Signal dc Open Loop Voltage Gain (V _O = ±10 V, R _L = 100 k ohms) { T _A = +25°C T _A = T _{low} to T _{high} (V _O = ±10 V, R _L = 10 k ohms, T _A = +25°C) | A _{VOL} | 100,000 | 500,000 | — | 70,000 | 500,000 | — | 50,000 | 500,000 | — | V/V |
| | | 50,000 | — | — | 50,000 | — | — | — | — | — | |
| Power Bandwidth (Voltage Follower) (A _V = 1, R _L = 5.0 k ohms, THD ≤ 5%, V _O = 40 V _{p-p}) | P _{BW} | — | 23 | — | — | 23 | — | — | 23 | — | kHz |
| Unity Gain Crossover Frequency (open-loop) | f _c | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | MHz |
| Phase Margin (open-loop, unity gain) | φ | — | 50 | — | — | 50 | — | — | 50 | — | degrees |
| Gain Margin | A _{GM} | — | 18 | — | — | 18 | — | — | 18 | — | dB |
| Slew Rate (Unity Gain) | dV _{out} /dt | — | 2.0 | — | — | 2.0 | — | — | 2.0 | — | V/μs |
| Output Impedance (f ≤ 5.0 Hz) | Z _{out} | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | k ohms |
| Short-Circuit Output Current | I _{SC} | — | ±17 | — | — | ±17 | — | — | ±19 | — | mAdc |
| Output Voltage Swing (R _L = 5.0 k ohms) V ⁺ = +28 Vdc, V ⁻ = -28 Vdc V ⁺ = +36 Vdc, V ⁻ = -36 Vdc | V _O | ±22 | ±23 | — | ±20 | ±22 | — | ±20 | ±22 | — | V _{pk} |
| | | ±30 | ±32 | — | — | — | — | — | — | — | |
| Power Supply Sensitivity (dc) V ⁻ = constant, R _s ≤ 10 k ohms V ⁺ = constant, R _s ≤ 10 k ohms | S ⁺ S ⁻ | — | 15 | 100 | — | 35 | 200 | — | 50 | — | μV/V |
| | | — | 15 | 100 | — | 35 | 200 | — | 50 | — | |
| Power Supply Current (See Note 2) | I _D ⁺ I _D ⁻ | — | 2.2 | 4.0 | — | 2.6 | 5.0 | — | 2.6 | 5.0 | mAdc |
| | | — | 2.2 | 4.0 | — | 2.6 | 5.0 | — | 2.6 | 5.0 | |
| DC Quiescent Power Dissipation (V _O = 0) | P _D | — | — | — | — | — | — | — | — | — | mW |
| | | — | 124 | 224 | — | 146 | 280 | — | 146 | 280 | |

Note 1: T_{low}: 0°C for MC1436G,CG
-55°C for MC1536G
T_{high}: +75°C for MC1436G,CG
+15°C for MC1536G

Note 2: V⁺ = |V⁻| = 5.0 Vdc to 36 Vdc for MC1536G
V⁺ = |V⁻| = 5.0 Vdc to 30 Vdc for MC1436G
V⁺ = |V⁻| = 5.0 Vdc to 28 Vdc for MC1436CG



FIGURE 5 – POWER BANDWIDTH

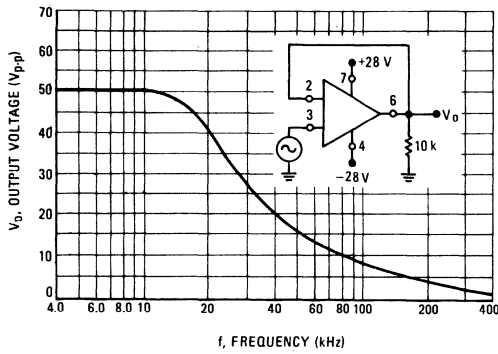


FIGURE 6 – PEAK OUTPUT VOLTAGE SWING versus POWER SUPPLY VOLTAGE

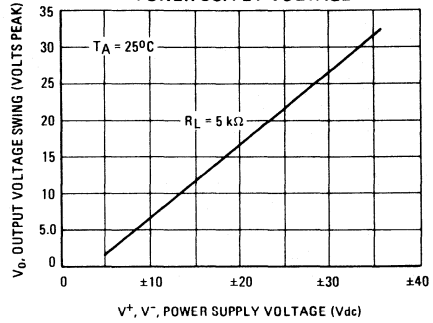


FIGURE 7 – OPEN-LOOP FREQUENCY RESPONSE

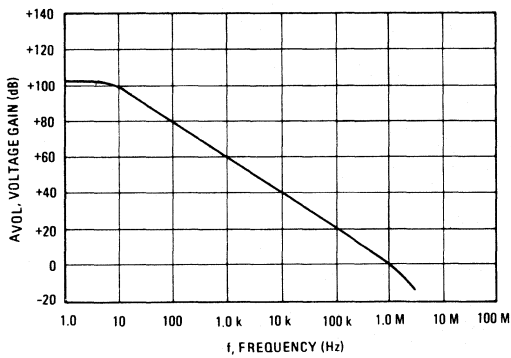


FIGURE 8 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

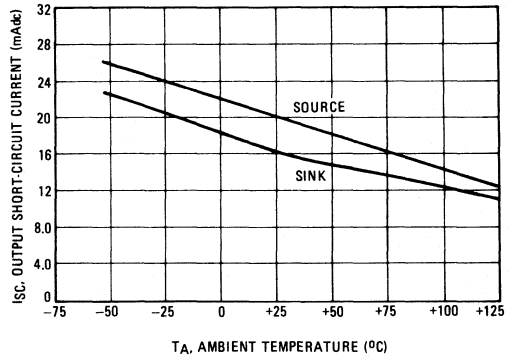


FIGURE 9 – INPUT BIAS CURRENT versus TEMPERATURE

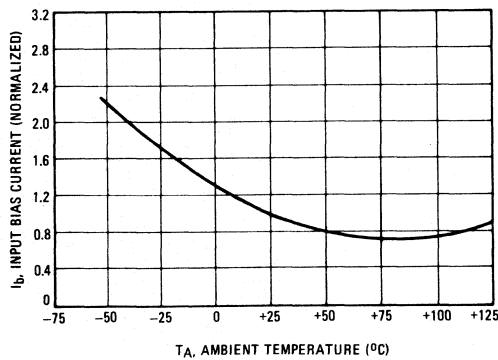


FIGURE 10 — INVERTING FEEDBACK MODEL

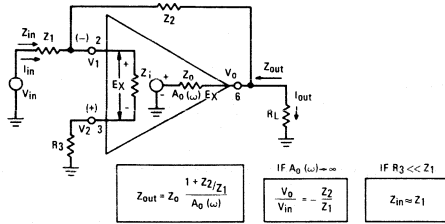


FIGURE 11 — NON-INVERTING FEEDBACK MODEL

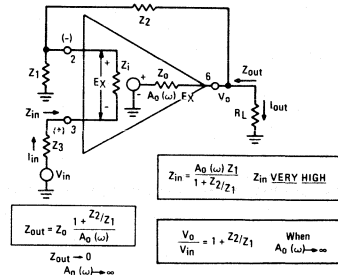


FIGURE 12 — AUDIO AMPLIFIER

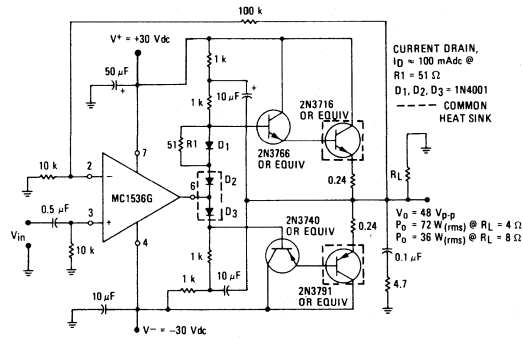


FIGURE 13 — CIRCUIT SCHEMATIC

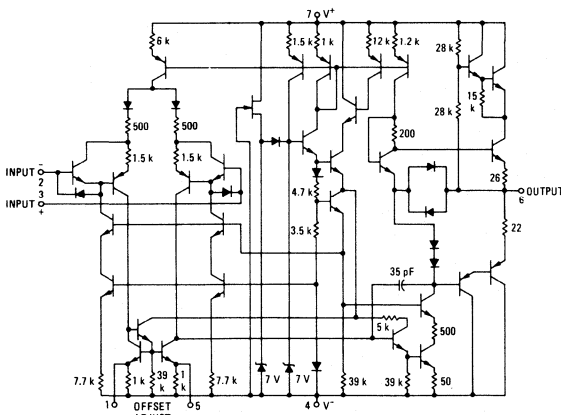
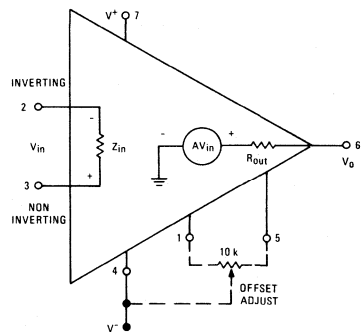


FIGURE 14 — EQUIVALENT CIRCUIT



MC1537 MC1437

HIGHLY MATCHED MONOLITHIC DUAL OPERATIONAL AMPLIFIERS

... designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics – $A_{VOL} = 45,000$ typical
- Low Temperature Drift – $\pm 3 \mu V/^\circ C$
- Large Output Voltage Swing – $\pm 14 V$ typical @ $\pm 15 V$ Supply

MAXIMUM RATINGS ($T_A = +25^\circ C$)

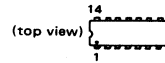
| Rating | Symbol | Value | Unit | |
|--|------------|----------------------------------|-------------|----------------|
| Power Supply Voltage | V^+ | +18 | Vdc | |
| | V^- | -18 | Vdc | |
| Differential Input Signal | V_{in} | ± 5.0 | Volts | |
| Common Mode Input Swing | CMV_{in} | $\pm V^+$ | Volts | |
| Output Short Circuit Duration | t_S | 5.0 | s | |
| Power Dissipation (Package Limitation) | P_D | Ceramic Package | 750 | mW |
| | | Derate above $T_A = +25^\circ C$ | 6.0 | mW/ $^\circ C$ |
| | | Plastic Package | 625 | mW |
| | | Derate above $T_A = +25^\circ C$ | 5.0 | mW/ $^\circ C$ |
| Operating Temperature Range | T_A | MC1537 | -55 to +125 | $^\circ C$ |
| | | MC1437 | 0 to +75 | $^\circ C$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ C$ | |

DUAL MC1709 MONOLITHIC SILICON OPERATIONAL AMPLIFIERS INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116



(MC1437 only)



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



FIGURE 1 – CIRCUIT SCHEMATIC

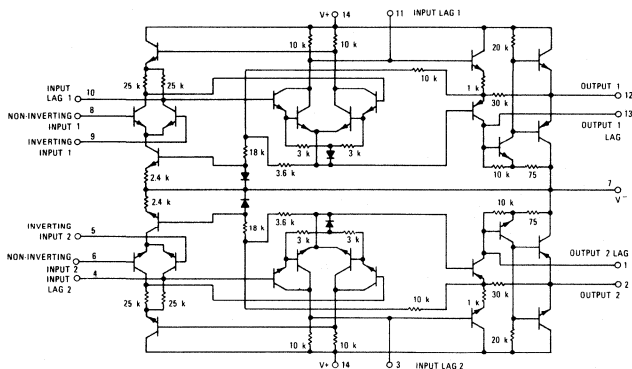
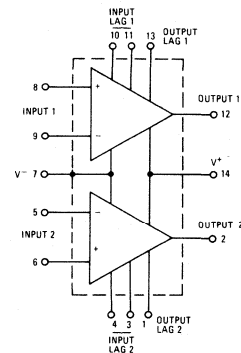


FIGURE 2 – EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

MC1537, MC1437 (continued)

ELECTRICAL CHARACTERISTICS — Each Amplifier ($V^+ = +15 \text{ Vdc}$, $V^- = -15 \text{ Vdc}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MC1537 | | | MC1437 | | | Unit |
|--|---|----------------------|---|-------------------|---------------|---|---------------------|--|
| | | Min | Typ | Max | Min | Typ | Max | |
| Open Loop Voltage Gain ($R_L = 5.0 \text{ k}\Omega$, $V_O = \pm 10 \text{ V}$, $T_A = T_{\text{low}} \text{ ①}$ to $T_{\text{high}} \text{ ②}$) | AVOL | 25,000 | 45,000 | 70,000 | 15,000 | 45,000 | — | — |
| Output Impedance ($f = 20 \text{ Hz}$) | Z_o | — | 30 | — | — | 30 | — | Ω |
| Input Impedance ($f = 20 \text{ Hz}$) | Z_{in} | 150 | 400 | — | 50 | 150 | — | $\text{k}\Omega$ |
| Output Voltage Swing ($R_L = 10 \text{ k}\Omega$) ($R_L = 2.0 \text{ k}\Omega$) | V_o | ± 12 ± 10 | ± 14 ± 13 | — | ± 12 — | ± 14 — | — | V_{peak} |
| Input Common-Mode Voltage Swing | CMV _{in} | ± 8.0 | ± 10 | — | ± 8.0 | ± 10 | — | V_{peak} |
| Common-Mode Rejection Ratio | CM _{rej} | 70 | 100 | — | 65 | 100 | — | dB |
| Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2} \right)$, ($T_A = +25^\circ\text{C}$) ($T_A = T_{\text{low}} \text{ ①}$) | I_b | — | 0.2 0.5 | 0.5 1.5 | — | 0.4 — | 1.5 2.0 | μA |
| Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, $T_A = T_{\text{low}} \text{ ①}$) ($I_{io} = I_1 - I_2$, $T_A = T_{\text{high}} \text{ ②}$) | $ I_{io} $ | — | 0.05 — | 0.2 0.6 0.2 | — | 0.05 — | 0.5 0.75 0.75 | μA |
| Input Offset Voltage ($T_A = +25^\circ\text{C}$) ($T_A = T_{\text{low}} \text{ ①}$ to $T_{\text{high}} \text{ ②}$) | $ V_{io} $ | — | 1.0 — | 5.0 6.0 | — | 1.0 — | 7.5 10 | mV |
| Step Response { Gain = 100, 5% overshoot, R ₁ = 1 k Ω , R ₂ = 100 k Ω , R ₃ = 1.5 k Ω , C ₁ = 100 pF, C ₂ = 3.0 pF } { Gain = 10, 10% overshoot, R ₁ = 1 k Ω , R ₂ = 10 k Ω , R ₃ = 1.5 k Ω , C ₁ = 500 pF, C ₂ = 20 pF } { Gain = 1, 5% overshoot, R ₁ = 10 k Ω , R ₂ = 10 k Ω , R ₃ = 1.5 k Ω , C ₁ = 5000 pF, C ₂ = 200 pF } | t_f t_{pd} dV_{out}/dt ③ t_f t_{pd} dV_{out}/dt ③ t_f t_{pd} dV_{out}/dt ③ | — | 0.8 0.38 12 0.6 0.34 1.7 2.2 1.3 0.25 | — | — | 0.8 0.38 12 0.6 0.34 1.7 2.2 1.3 0.25 | — | μs μs $\text{V}/\mu\text{s}$ μs μs $\text{V}/\mu\text{s}$ μs μs $\text{V}/\mu\text{s}$ |
| Average Temperature Coefficient of Input Offset Voltage ($R_S = 50 \Omega$, $T_A = T_{\text{low}} \text{ ①}$ to $T_{\text{high}} \text{ ②}$) ($R_S \leq 10 \text{ k}\Omega$, $T_A = T_{\text{low}} \text{ ①}$ to $T_{\text{high}} \text{ ②}$) | $ TC_{V_{io}} $ | — | 1.5 3.0 | — | — | 1.5 3.0 | — | $\mu\text{V}/^\circ\text{C}$ |
| Average Temperature Coefficient of Input Offset Current ($T_A = T_{\text{low}} \text{ ①}$ to $+25^\circ\text{C}$) ($T_A = +25^\circ\text{C}$ to $T_{\text{high}} \text{ ②}$) | $ TC_{I_{io}} $ | — | 0.7 0.7 | — | — | 0.7 0.7 | — | $\text{nA}/^\circ\text{C}$ |
| DC Power Dissipation (Total) (Power Supply = $\pm 15 \text{ V}$, $V_O = 0$) | P_D | — | 160 | 225 | — | 160 | 225 | mW |
| Positive Supply Sensitivity (V^- constant) | S^+ | — | 10 | 150 | — | 10 | 200 | $\mu\text{V}/\text{V}$ |
| Negative Supply Sensitivity (V^+ constant) | S^- | — | 10 | 150 | — | 10 | 200 | $\mu\text{V}/\text{V}$ |

① $T_{\text{low}} = 0^\circ\text{C}$ for MC1437
 $= -55^\circ\text{C}$ for MC1537

② $T_{\text{high}} = +75^\circ\text{C}$ for MC1437
 $= +125^\circ\text{C}$ for MC1537

③ $dV_{\text{out}}/dt = \text{Slew Rate}$

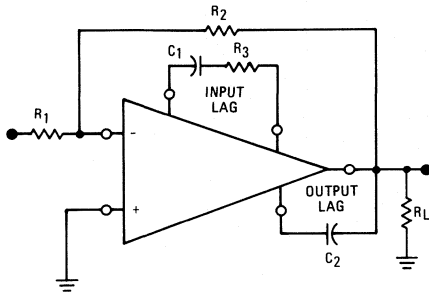
MATCHING CHARACTERISTICS

| | | | | | | | | |
|--|--|---|------------|---|---|------------|---|------------------------------|
| Open Loop Voltage Gain | AVOL1-AVOL2 | — | ± 1.0 | — | — | ± 1.0 | — | dB |
| Input Bias Current | $I_{b1}-I_{b2}$ | — | ± 0.15 | — | — | ± 0.15 | — | μA |
| Input Offset Current | $ I_{io1} - I_{io2} $ | — | ± 0.02 | — | — | ± 0.02 | — | μA |
| Average Temperature Coefficient | $ TC_{I_{io1}} - TC_{I_{io2}} $ | — | ± 0.2 | — | — | ± 0.2 | — | $\text{nA}/^\circ\text{C}$ |
| Input Offset Voltage | $ V_{io1} - V_{io2} $ | — | ± 0.2 | — | — | ± 0.2 | — | mV |
| Average Temperature Coefficient | $ TC_{V_{io1}} - TC_{V_{io2}} $ | — | ± 0.5 | — | — | ± 0.5 | — | $\mu\text{V}/^\circ\text{C}$ |
| Channel Separation ($f = 10 \text{ kHz}$) | $e_{\text{out } 1}$ $e_{\text{out } 2}$ | — | 90 | — | — | 90 | — | dB |

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT

$V^+ = +15\text{ Vdc}$, $V^- = 15\text{ Vdc}$, $T_A = 25^\circ\text{C}$



| FIGURE NO. | CURVE NO. | VOLTAGE GAIN | TEST CONDITIONS | | | | | OUTPUT NOISE (mV[rms]) |
|------------|-----------|--------------|-----------------|---------------|---------------|--------------------|--------------------|------------------------|
| | | | $R_1(\Omega)$ | $R_2(\Omega)$ | $R_3(\Omega)$ | $C_1(\mu\text{F})$ | $C_2(\mu\text{F})$ | |
| 4 | 1 | 1 | 10 k | 10 k | 1.5 k | 5.0 k | 200 | 0.10 |
| | 2 | 10 | 10 k | 100 k | 1.5 k | 500 | 20 | 0.14 |
| | 3 | 100 | 10 k | 1.0 M | 1.5 k | 100 | 3.0 | 0.7 |
| | 4 | 1000 | 1.0 k | 1.0 M | 0 | 10 | 3.0 | 5.2 |
| 5 | 1 | 1 | 10 k | 10 k | 1.5 k | 5.0 k | 200 | 0.10 |
| | 2 | 10 | 10 k | 100 k | 1.5 k | 500 | 20 | 0.14 |
| | 3 | 100 | 10 k | 1.0 M | 1.5 k | 100 | 3.0 | 0.7 |
| | 4 | 1000 | 1.0 k | 1.0 M | 0 | 10 | 3.0 | 5.2 |
| 6 | 1 | AVOL | 0 | ∞ | 1.5 k | 5.0 k | 200 | 5.5 |
| | 2 | AVOL | 0 | ∞ | 1.5 k | 500 | 20 | 10.5 |
| | 3 | AVOL | 0 | ∞ | 1.5 k | 100 | 3.0 | 21.0 |
| | 4 | AVOL | 0 | ∞ | 0 | 10 | 3.0 | 39.0 |
| | 5 | AVOL | 0 | ∞ | ∞ | 0 | 3.0 | — |

FIGURE 4 – LARGE SIGNAL SWING versus FREQUENCY

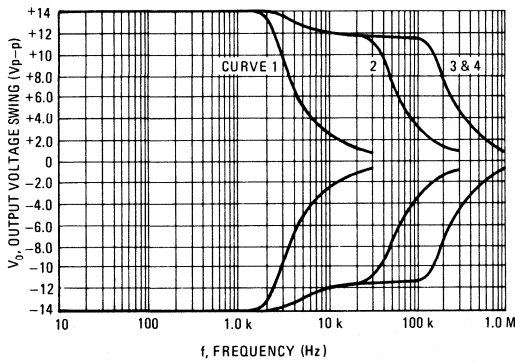


FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

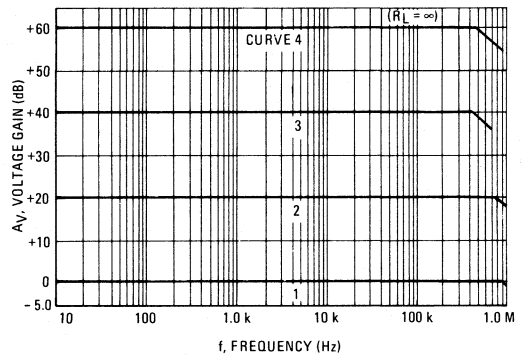


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

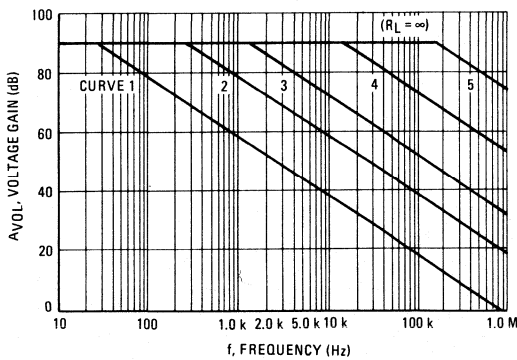
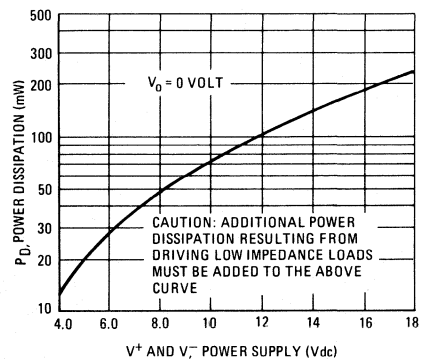


FIGURE 7 – TOTAL POWER DISSIPATION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

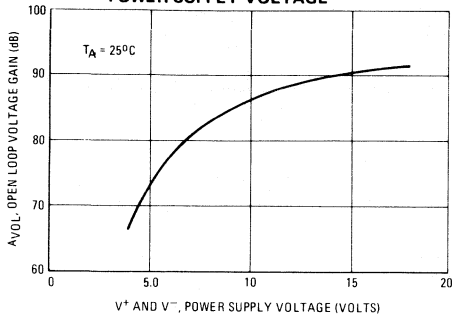


FIGURE 9 – COMMON INPUT SWING versus POWER SUPPLY VOLTAGE

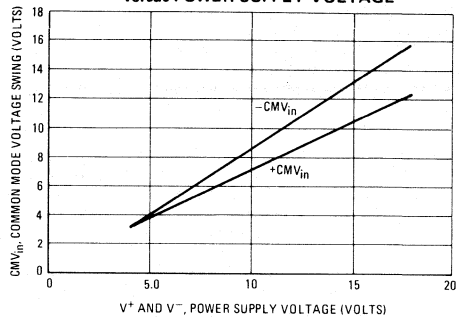


FIGURE 10 – INPUT OFFSET VOLTAGE versus TEMPERATURE

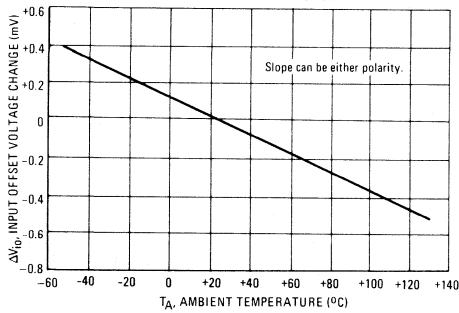


FIGURE 11 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE

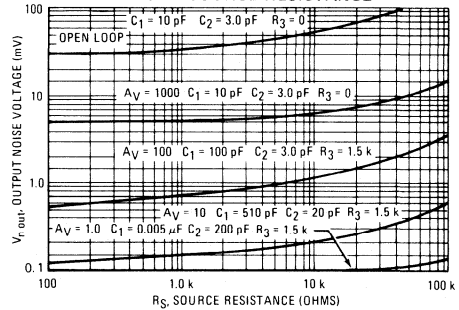
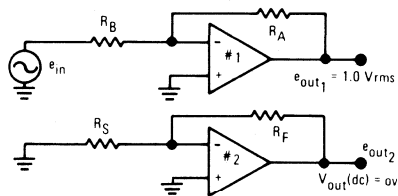
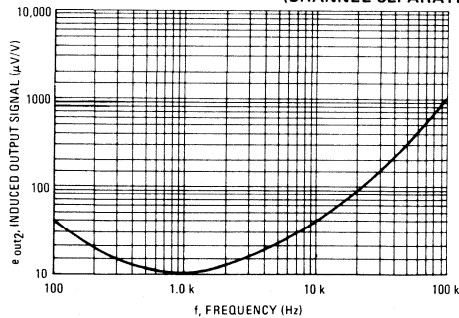


FIGURE 12 – INDUCED OUTPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY



Induced output signal (μV of induced output signal in amplifier #2 per volt of output signal at amplifier #1).

MC1538R MC1438R

POWER BOOSTER

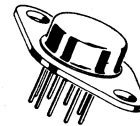
MONOLITHIC POWER BOOSTER

The MC1538/MC1438 is designed as a high current gain amplifier (70 dB), with unity voltage gain that can deliver load currents up to ± 300 mA dc. This device is ideally suited to follow an operational amplifier (such as MC1556/MC1456) for driving low impedance loads and improving the overall circuit performance.

- High Input Impedance – 0.4 Meg-Ohm typ – when driving the MC1538/MC1438, the gain of an operational amplifier will approach the unloaded open-loop gain. Internal power dissipation of the operational amplifier will be independent of output voltage and therefore thermal drift will be reduced.
- Large Power Bandwidth – 1.5 MHz typ – considerably better than present operational amplifiers. Bandwidth and slew rate will be limited by the operational amplifier, not the MC1538/MC1438.
- Low Output Impedance – 10 Ohms typ – allows the MC1538/MC1438 to drive a capacitive load with greatly reduced phase shift compared with an operational amplifier. Output voltage swing capability is much increased when driving small load impedances.
- Adjustable Current Limit – ± 5.0 mA dc to ± 300 mA dc
- Excellent Power-Supply Rejection – 1.0 mV/V typ
- Current Gain – 3000 typ

POWER BOOSTER INTEGRATED CIRCUIT FOR OPERATIONAL AMPLIFIERS EPITAXIAL PASSIVATED

CASE 614

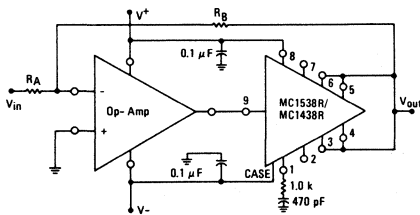


Weight ≈ 6.315 grams

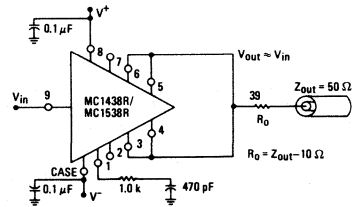
Case connected to V^-

TYPICAL APPLICATIONS

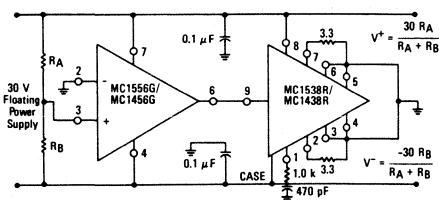
OPERATIONAL AMPLIFIER BOOST CIRCUIT



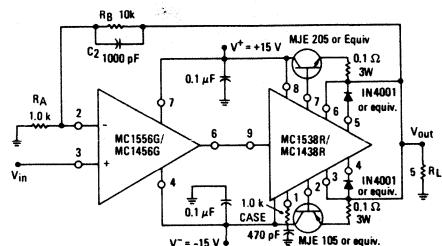
DIGITAL OR ANALOG LINE DRIVER



POWER SUPPLY SPLITTER



SERVO/POWER AMPLIFIER



See Packaging Information Section for outline dimensions.

MC1538R, MC1438R (continued)

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

| Rating | Symbol | MC1538R | MC1438R | Unit |
|--|------------------------------------|----------------------------------|------------|-------|
| Power Supply Voltage | V ⁺ V ⁻ | +22 -22 | +18 -18 | Vdc |
| Input-Output Voltage Differential | V _{in} - V _{out} | -14.5, +44 | -14, +36 | Vdc |
| Input Voltage Swing | V _{in} | V ⁺ or V ⁻ | | Vdc |
| Load Current | I _L | 350 | | mAdc |
| Power Dissipation and Thermal Characteristics | | | | |
| T _A = +25°C | P _D | 3.0 | | Watts |
| Derate above T _A = +25°C | 1/θ _{JA} | 24 | | mW/°C |
| Thermal Resistance, Junction to Air | θ _{JA} | 41.6 | | °C/W |
| T _C = +25°C | P _D | 17.5 | | Watts |
| Derate above T _C = +25°C | 1/θ _{JC} | 140 | | mW/°C |
| Thermal Resistance, Junction to Case | θ _{JC} | 7.15 | | °C/W |
| Operating and Storage Junction Temperature Range | T _J , T _{stg} | -65 to +150 | | °C |

OPERATING TEMPERATURE RANGE

| Ambient Temperature | MC1438R MC1538R | T _A | 0 to +75 -55 to +125 | °C |
|---------------------|--------------------|----------------|-------------------------|----|
|---------------------|--------------------|----------------|-------------------------|----|

ELECTRICAL CHARACTERISTICS

(R_L = 300 ohms, T_C = +25°C unless otherwise noted.)

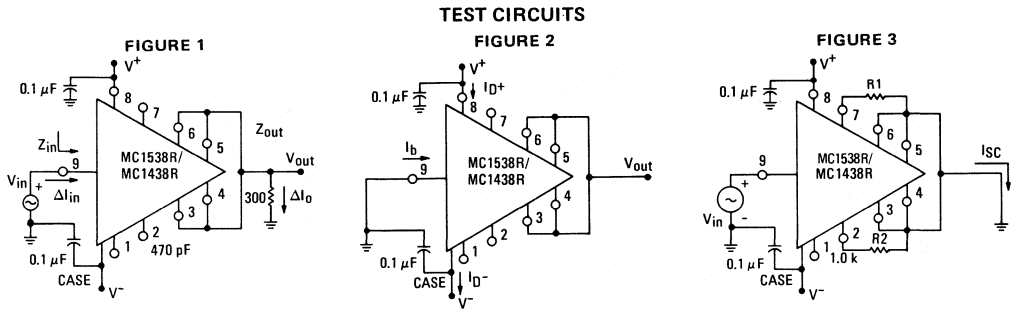
| Characteristic (Linear Operation) | Fig | Note | Symbol | MC1538R | | | MC1438R | | | Unit |
|---|---------------|------|------------------------------------|--|--|--|--------------|-------------------------|---------------|--------|
| | | | | V ⁺ = +5 V to +20 V, V ⁻ = -5 V to -20 V | V ⁺ = +15 V, V ⁻ = -15 V | V ⁺ = +15 V, V ⁻ = -15 V | Min | Typ | Max | |
| Voltage Gain (f = 1.0 kHz) | 1 | — | A _V | 0.9 | 0.95 | 1.0 | 0.85 | 0.95 | 1.0 | V/V |
| Current Gain (A _I = ΔI _O /ΔI _{in}) | 1 | — | A _I | — | 3000 | — | — | 3000 | — | A/A |
| Output Impedance (f = 1.0 kHz) | 1 | — | Z _{out} | — | 10 | — | — | 10 | — | Ohms |
| Input Impedance (f = 1.0 kHz) | 1 | — | Z _{in} | — | 400 | — | — | 400 | — | k ohms |
| Output Voltage Swing _i | 1 | 3 | V _{out} | ±12 | ±13 | — | ±11 | ±12 | — | Vdc |
| Input Bias Current | 2 | — | I _b | — | 60 | 200 | — | 60 | 300 | μAdc |
| Output Offset Voltage | 2 | 1 | V _{oo} | — | 25 | 150 | — | 25 | 200 | mVdc |
| Small Signal Bandwidth (R _L = 300 ohms) (V _{in} = 0 Vdc, V _{in} = 100 mV [rms]) | 1 | — | BW _{3 dB} | — | 8.0 | — | — | 8.0 | — | MHz |
| Power Bandwidth (V _{out} = 20 V _{p-p} , THD = 5%) | 1 | 3 | PBW | — | 1.5 | — | — | 1.5 | — | MHz |
| Total Harmonic Distortion (f = 1.0 kHz, V _{out} = 20 V _{p-p}) | 1 | 3 | THD | — | 0.5 | — | — | 0.5 | — | % |
| Short-Circuit Output Current (R ₁ = R ₂ = ∞) (R ₁ = R ₂ = 3.3 ohms) Adjustable Range | 3 3 4,5 | 2 | I _{SC} | 75 — — | 95 300 5.0 to 300 | 125 — — | 65 — — | 95 300 5.0 to 300 | 140 — — | mAdc |
| Power Supply Sensitivity (V ⁻ constant) (V ⁺ constant) | 2 | — | S ⁺ S ⁻ | — — | 1.0 1.0 | — — | — — | 1.0 1.0 | — — | mV/V |
| Power Supply Current (R _L = ∞, V _{in} = 0) | 2 | — | I _{D+} or I _{D-} | 4.5 | 6.0 | 10 | 2.5 | 6.0 | 15 | mAdc |
| Power Dissipation (R _L = ∞, V _{in} = 0). | 2 | 3 | P _D | 150 | 180 | 300 | 75 | 180 | 450 | mW |

Note 1. Output offset Voltage is the quiescent dc output voltage with the input grounded.

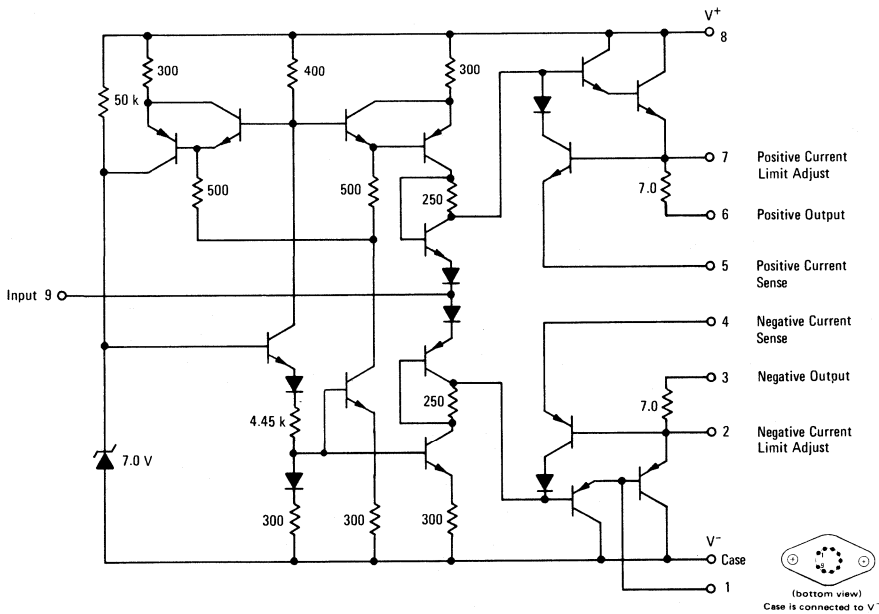
Note 2. Short-Circuit Current, I_{SC}, is adjustable by varying R₁, R₂, R₃ and R₄. The positive current limit is set by R₁ or R₃, and the negative current limit is set by R₂ or R₄. See Figures 4 and 5 for curves of short-circuit current versus R₁, R₂, R₃ and R₄.

Note 3. V⁺ = +15 V, V⁻ = -15 V.

MC1538R, MC1438R (continued)



CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 4 – SHORT-CIRCUIT CURRENT versus R1 OR R2 (100 mA to 300 mA)

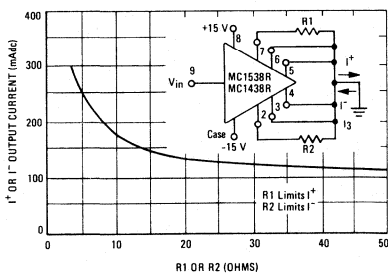
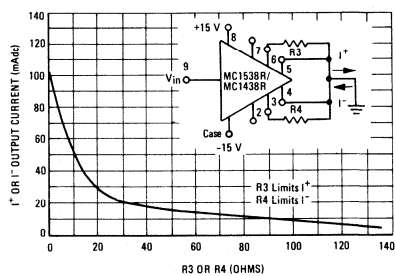


FIGURE 5 – SHORT-CIRCUIT CURRENT versus R3 OR R4 (5.0 mA to 100 mA)



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – POWER SUPPLY CURRENT versus SHUNT RESISTANCE

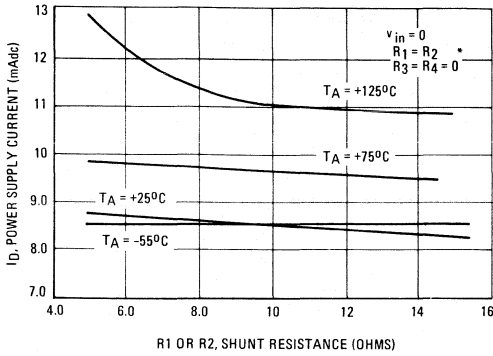


FIGURE 7 – SMALL SIGNAL GAIN AND PHASE RESPONSE

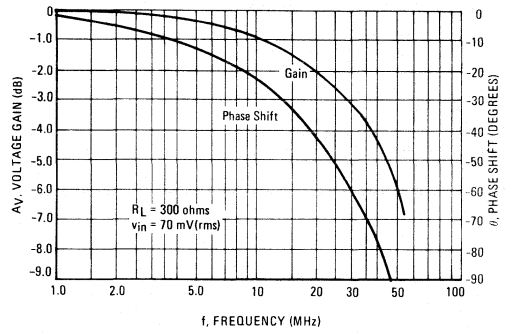


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD CURRENT

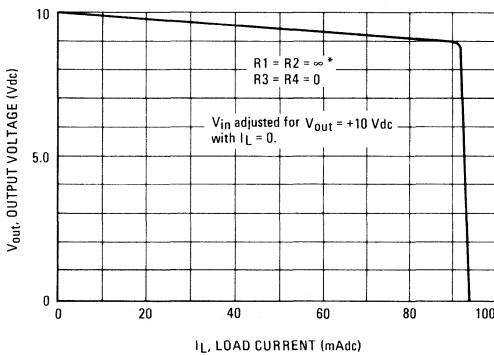


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD CURRENT

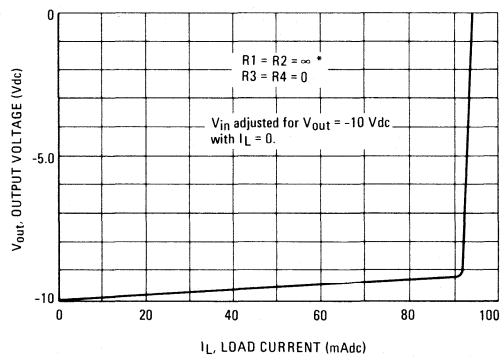


FIGURE 10 – OUTPUT OFFSET VOLTAGE versus TEMPERATURE

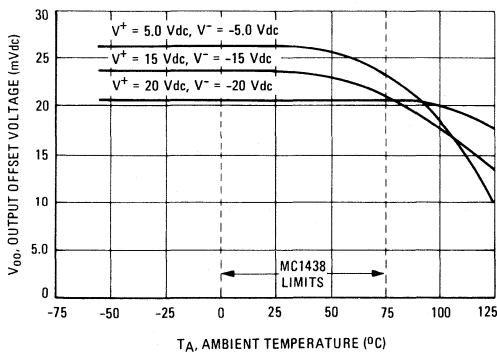
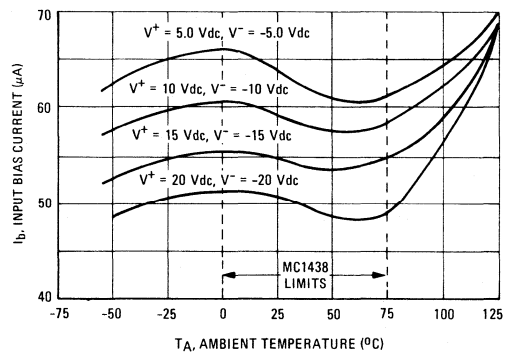


FIGURE 11 – INPUT BIAS CURRENT versus TEMPERATURE



*See figures 4 and 5 for definition of R1, R2, R3, and R4.

MC1538R, MC1438R (continued)

TYPICAL CHARACTERISTICS (continued) ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 12 – PULSE RESPONSE CHARACTERISTICS

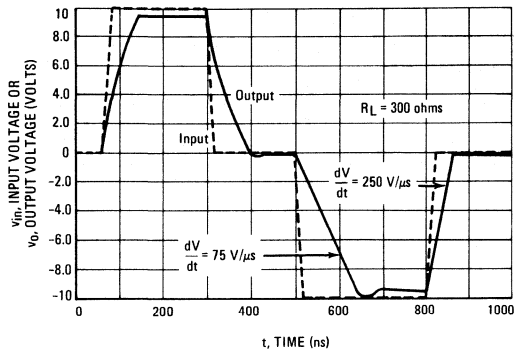
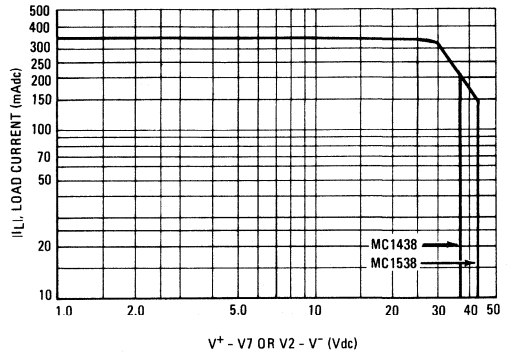


FIGURE 13 – DC SAFE OPERATING AREA



TYPICAL APPLICATIONS

FIGURE 14 – NON-INVERTING AC POWER AMPLIFIER

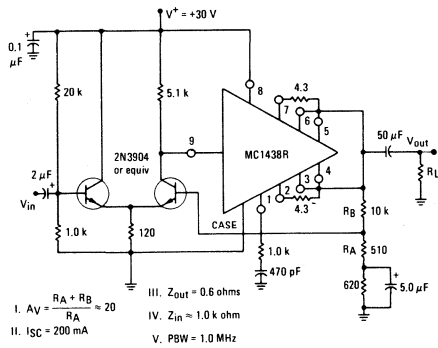


FIGURE 15 – NON-INVERTING POWER AMPLIFIER

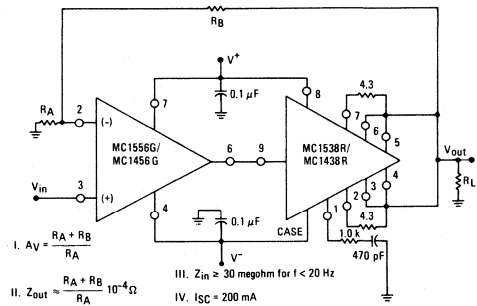


FIGURE 16 – NON-INVERTING VOLTAGE FOLLOWER

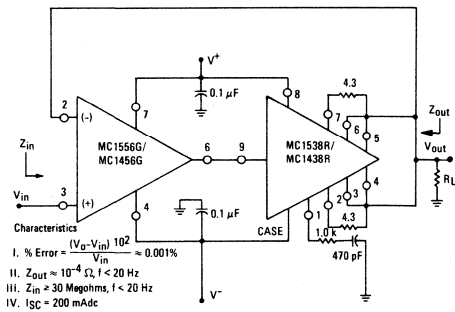
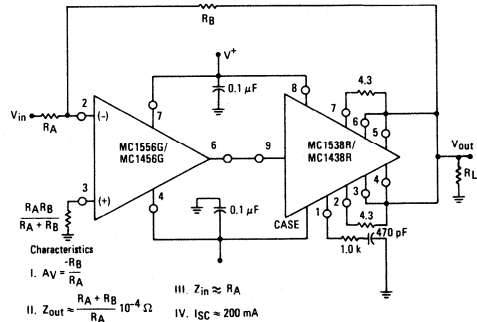


FIGURE 17 – INVERTING POWER AMPLIFIER



MC1538R, MC1438R (continued)

TYPICAL APPLICATIONS (continued)

FIGURE 18 – PROGRAMMABLE VOLTAGE SOURCE

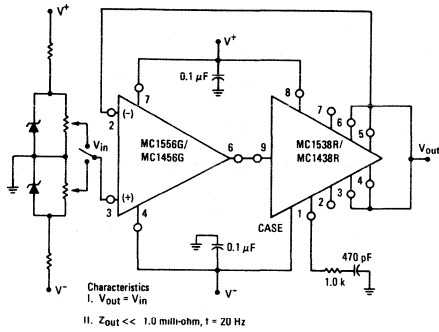


FIGURE 19 – CONSTANT CURRENT SOURCE OR TRANSCONDUCTANCE AMPLIFIER

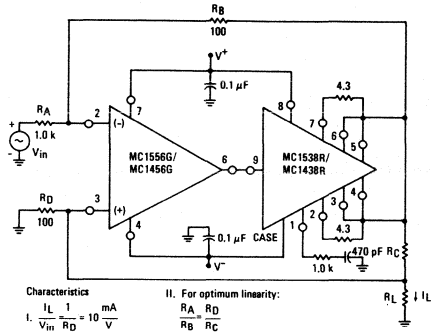


FIGURE 20 – SIGNAL DISTRIBUTION

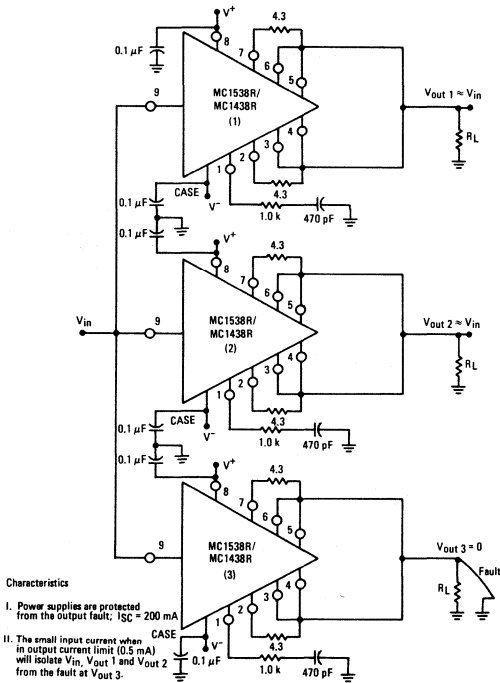


FIGURE 21 – ASTABLE MULTIVIBRATOR

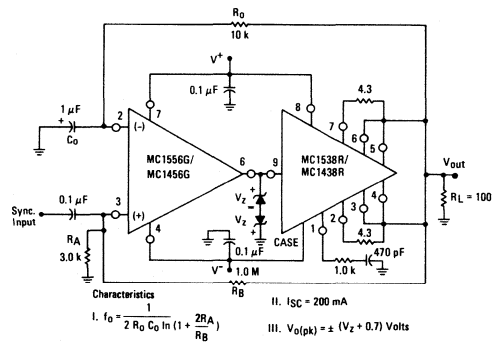
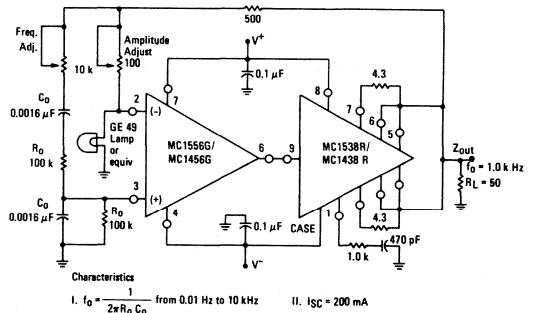


FIGURE 22 – WIEN BRIDGE OSCILLATOR



MC1539 MC1439

OPERATIONAL AMPLIFIERS

MONOLITHIC OPERATIONAL AMPLIFIER

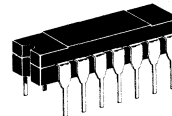
... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information see Motorola Application Note AN-439.

- Low Input Offset Voltage – 3.0 mV max
- Low Input Offset Current – 60 nA max
- Large Power-Bandwidth – 20 V_{p-p} Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- Slew Rate – 34 V/μs typ

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON

G SUFFIX
METAL PACKAGE
CASE 601
TO-99



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P2 SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116
(MC1439 only)

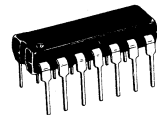
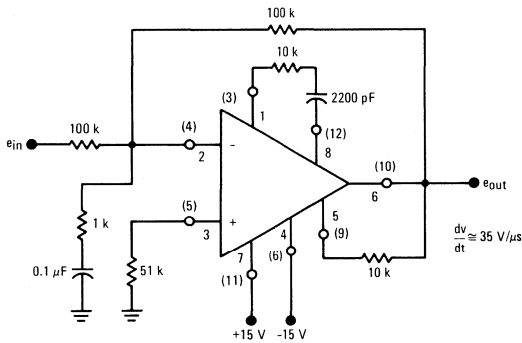


FIGURE 1 – HIGH SLEW RATE INVERTER



Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.

FIGURE 2 – OUTPUT NULLING CIRCUIT

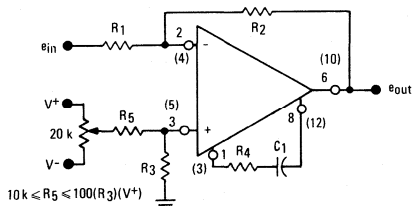
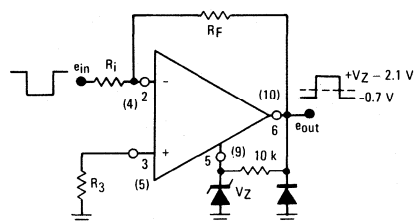


FIGURE 3 – OUTPUT LIMITING CIRCUIT



See Packaging Information Section for outline dimensions.

See current MCC1539/1439 data sheet for standard linear chip information.

MC1539, MC1439 (continued)

ELECTRICAL CHARACTERISTICS (V⁺ = +15 Vdc, V⁻ = -15 Vdc, T_A = +25°C unless otherwise noted)

| Characteristic | Symbol | MC1539 | | | MC1439 | | | Unit |
|--|--|------------------|--------------------|--------------|------------------|--------------------|------------|------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current (T _A = +25°C) (T _A = T _{low} ①) | I _b | — | 0.20 0.23 | 0.50 0.70 | — | 0.20 0.23 | 1.0 1.5 | μA |
| Input Offset Current (T _A = T _{low}) (T _A = +25°C) (T _A = T _{high} ①) | I _{io} | — | — | 75 | — | — | 150 | nA |
| Input Offset Voltage (T _A = +25°C) (T _A = T _{low} , T _{high}) | V _{io} | — | 1.0 | 3.0 | — | 2.0 | 7.5 | mV |
| Average Temperature Coefficient of Input Offset Voltage (T _A = T _{low} to T _{high}) (R _S = 50 Ω) (R _S ≤ 10 kΩ) | TC _{Vio} | — | 3.0 5.0 | — | — | 3.0 5.0 | — | μV/°C |
| Input Impedance (f = 20 Hz) | Z _{in} | 150 | 300 | — | 100 | 300 | — | kΩ |
| Input Common-Mode Voltage Swing | CMV _{in} | ±11 | ±12 | — | ±11 | ±12 | — | V _{pk} |
| Equivalent Input Noise Voltage (R _S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz) | e _n | — | 30 | — | — | 30 | — | nV/(Hz) ^{1/2} |
| Common-Mode Rejection Ratio (f = 1.0 kHz) | CM _{rej} | 80 | 110 | — | 80 | 110 | — | dB |
| Open-Loop Voltage Gain (V _O = ±10 V, R _L = 10 kΩ, R _S = ∞) (T _A = +25°C to T _{high}) (T _A = T _{low}) | A _{VOL} | 50,000 25,000 | 120,000 100,000 | — | 15,000 15,000 | 100,000 100,000 | — | — |
| Power Bandwidth (A _v = 1, THD ≤ 5%, V _O = 20 V _{p-p}) (R _L = 2.0 kΩ) (R _L = 1.0 kΩ) | PBW | — | — | — | 10 | 50 | — | kHz |
| Step Response { Gain = 1000, no overshoot, R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ, R4 = 30 kΩ, R5 = 10 kΩ, C1 = 1000 pF } dV _{out} /dt ② | t _f t _{pd} | — | 130 190 | — | — | 130 190 | — | ns |
| { Gain = 1000, 15% overshoot, R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ, R4 = 0, R5 = 10 kΩ, C1 = 10 pF } dV _{out} /dt | t _f t _{pd} | — | 80 100 | — | — | 80 100 | — | ns |
| { Gain = 100, no overshoot, R1 = 1.0 kΩ, R2 = 100 kΩ, R3 = 1.0 kΩ, R4 = 10 kΩ, R5 = 10 kΩ, C1 = 2200 pF } dV _{out} /dt | t _f t _{pd} | — | 60 100 | — | — | 60 100 | — | ns |
| { Gain = 10, 15% overshoot, R1 = 1.0 kΩ, R2 = 10 kΩ, R3 = 1.0 kΩ, R4 = 1.0 kΩ, R5 = 10 kΩ, C1 = 2200 pF } dV _{out} /dt | t _f t _{pd} | — | 120 80 | — | — | 120 80 | — | ns |
| { Gain = 1, 15% overshoot, R1 = 10 kΩ, R2 = 10 kΩ, R3 = 5.0 kΩ, R4 = 390 Ω, R5 = 10 kΩ, C1 = 2200 pF } dV _{out} /dt | t _f t _{pd} | — | 160 80 | — | — | 160 80 | — | ns |
| Output Impedance (f = 20 Hz) | Z _{out} | — | 4.0 | — | — | 4.0 | — | kΩ |
| Output Voltage Swing (R _L = 2.0 kΩ, f = 1.0 kHz) (R _L = 1.0 kΩ, f = 1.0 kHz) | V _{out} | — | — | — | ±10 | ±13 | — | V _{pk} |
| Positive Supply Sensitivity (V ⁻ constant) | S ⁺ | — | 50 | 150 | — | 50 | 200 | μV/V |
| Negative Supply Sensitivity (V ⁺ constant) | S ⁻ | — | 50 | 150 | — | 50 | 200 | μV/V |
| Power Supply Current (V _O = 0) | I _D ⁺ I _D ⁻ | — | 3.0 3.0 | 5.0 5.0 | — | 3.0 3.0 | 6.7 6.7 | mAdc |

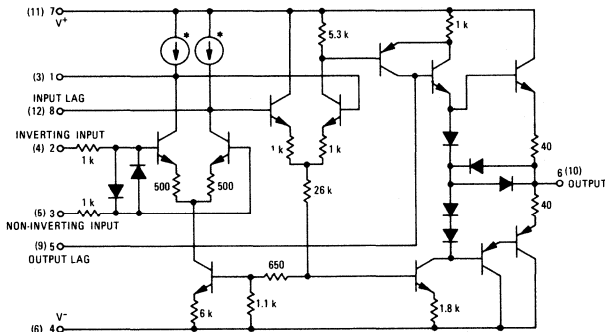
① T_{low} = 0°C for MC1439 T_{high} = +75°C for MC1439
-55°C for MC1539 +125°C for MC1539

② dV_{out}/dt = Slew Rate

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

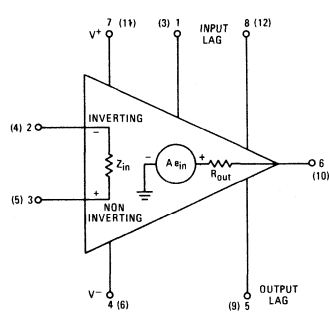
| Rating | Symbol | Value | Unit | |
|--|------------------|--|----------------------------|----------------------|
| Power Supply Voltage | V^+ | +18 | Vdc | |
| | V^- | -18 | Vdc | |
| Differential Input Signal | V_{in} | $\pm[V^+ + V^-]$ | Vdc | |
| Common Mode Input Swing | CMV_{in} | $+V^+, - V^- $ | Vdc | |
| Load Current | I_L | 15 | mA | |
| Output Short Circuit Duration | t_S | Continuous | | |
| Power Dissipation (Package Limitation) | P_D | | | |
| | | Metal Can | 680 | mW |
| | | Derate above $T_A = +25^\circ\text{C}$ | 4.6 | mW/ $^\circ\text{C}$ |
| | | Ceramic Dual In-Line Package | 750 | mW |
| | | Derate above $T_A = +25^\circ\text{C}$ | 6.0 | mW/ $^\circ\text{C}$ |
| Plastic Dual In-Line Package | | 625 | mW | |
| | | Derate above $T_A = +25^\circ\text{C}$ | 5.0 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | MC1539 MC1439 | T_A | -55 to +125 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | | T_{stg} | -65 to +150 -55 to +125 | $^\circ\text{C}$ |
| Metal and Ceramic Packages | | | | |
| Plastic Package | | | | |

FIGURE 4 - CIRCUIT SCHEMATIC



Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.
Pin 7 is electrically connected to the substrate and V^- for Case 646 (plastic package) only.
*Patent pending.

FIGURE 5 - EQUIVALENT CIRCUIT



TYPICAL CHARACTERISTICS

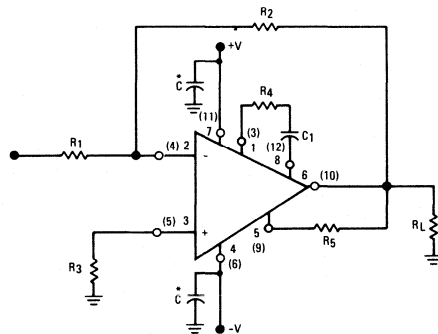
($V^+ = +15\text{ Vdc}$, $V^- = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$)

TYPICAL OUTPUT CHARACTERISTICS

($V^+ = +15\text{ Vdc}$, $V^- = -15\text{ Vdc}$, $T_A = 25^\circ\text{C}$)

| FIGURE NO. | CURVE NO. | VOLTAGE GAIN | TEST CONDITIONS (FIGURE 6) | | | | | | |
|------------|-----------|--------------|----------------------------|--------------------|--------------------|--------------------|--------------------|------------|------|
| | | | R_1 (Ω) | R_2 (Ω) | R_3 (Ω) | R_4 (Ω) | R_5 (Ω) | C_1 (pF) | |
| 7,8,10,12 | 1 | AVOL | 0 | ∞ | 0 | ∞ | ∞ | 0 | 2200 |
| | 2 | 10 | 10 k | 10 k | 5.0 k | 390 | 10 k | 10 k | 2200 |
| | 3 | 10 | 1.0 k | 10 k | 1.0 k | 1.0 k | 10 k | 10 k | 2200 |
| | 4 | 100 | 1.0 k | 100 k | 1.0 k | 1.0 k | 10 k | 10 k | 2200 |
| | 5 | 1000 | 1.0 k | 1.0 M | 1.0 k | 30 k | 10 k | 10 k | 1000 |
| | 6 | 1000 | 1.0 k | 1.0 M | 1.0 k | 0 | 10 k | 10 k | 10 |
| 13 | ALL | 1 | 10 k | 10 k | 5.0 k | 390 | 10 k | 10 k | 2200 |
| 14 | ALL | 10 | 1.0 k | 10 k | 1.0 k | 1.0 k | 10 k | 10 k | 2200 |
| 15 | ALL | 100 | 1.0 k | 100 k | 1.0 k | 10 k | 10 k | 10 k | 2200 |
| 16 | ALL | 1000 | 1.0 k | 1.0 M | 1.0 k | 30 k | 10 k | 10 k | 2200 |

FIGURE 6 - TEST CIRCUIT



TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25^\circ\text{C}$, unless otherwise noted)

FIGURE 7 – LARGE SIGNAL SWING versus FREQUENCY

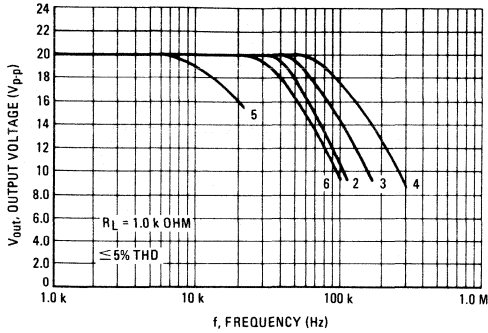


FIGURE 8 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

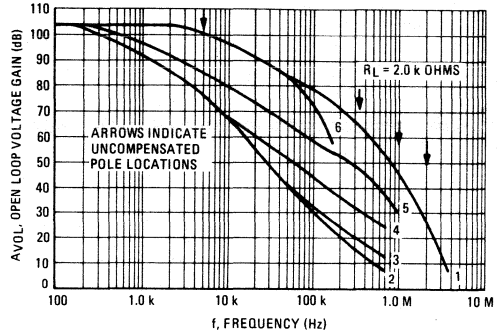


FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

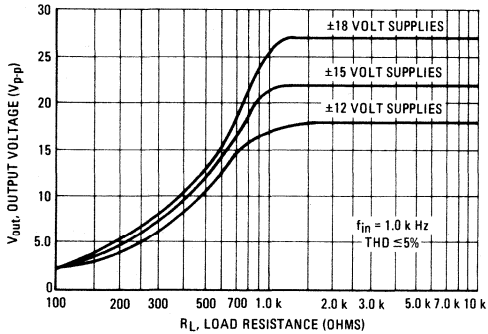


FIGURE 10 – OPEN LOOP PHASE SHIFT versus FREQUENCY

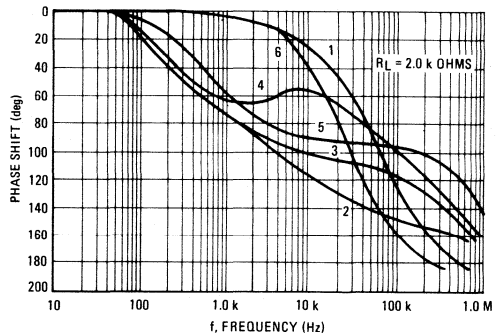


FIGURE 11 – OUTPUT VOLTAGE SWING (to clipping) versus SUPPLY

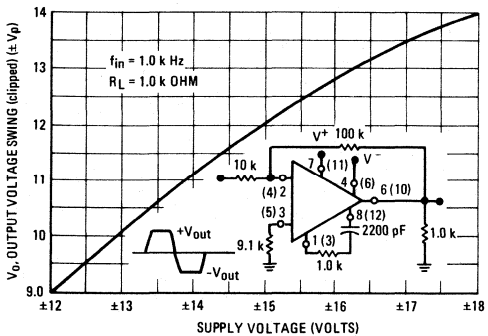
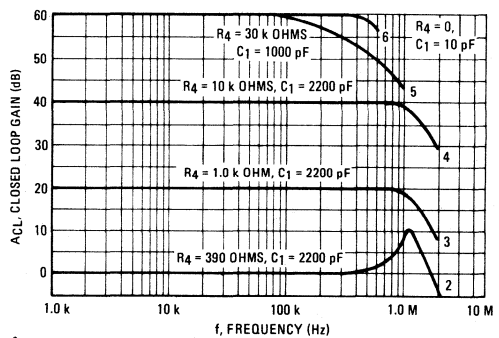


FIGURE 12 – CLOSED LOOP GAIN versus FREQUENCY



* A_{CL} = Closed Loop Gain

Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.

FIGURE 13 - $A_{CL}^* = 1$ RESPONSE versus TEMPERATURE

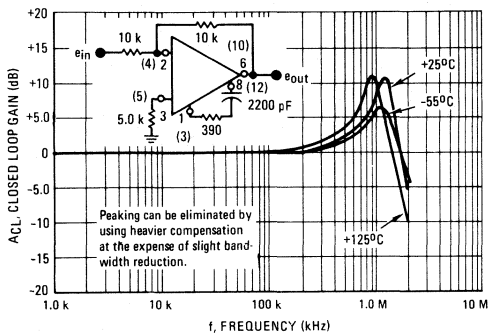


FIGURE 14 - $A_{CL} = 10$ RESPONSE versus TEMPERATURE

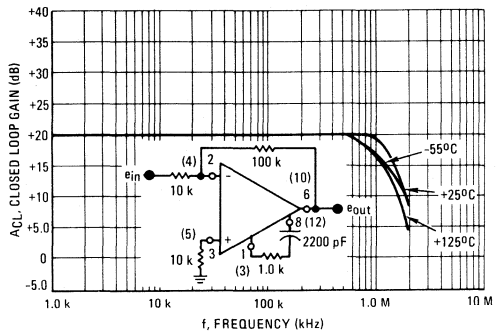


FIGURE 15 - $A_{CL} = 100$ RESPONSE versus TEMPERATURE

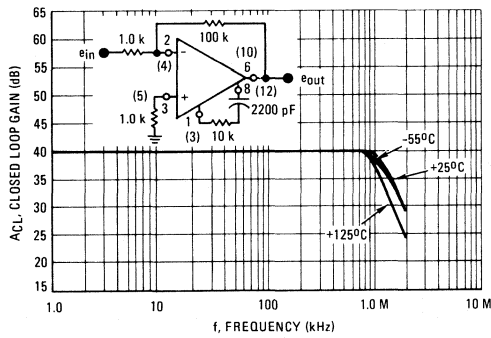


FIGURE 16 - $A_{CL} = 1000$ RESPONSE versus TEMPERATURE

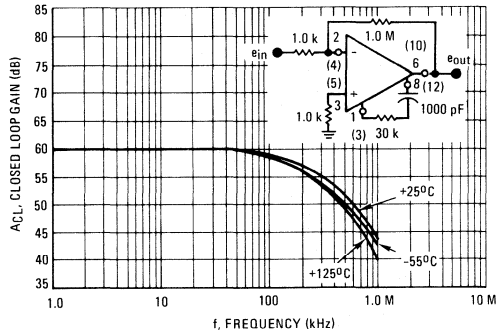
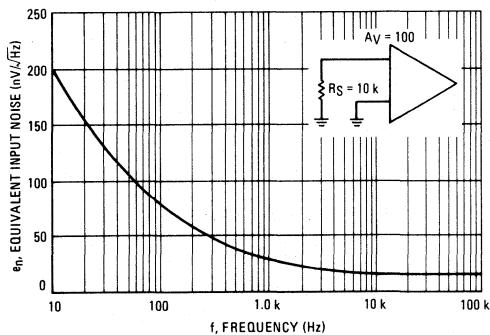


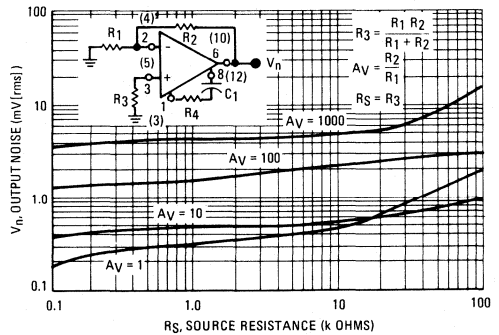
FIGURE 17 - SPECTRAL NOISE DENSITY



* A_{CL} = Closed Loop Gain

Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.

FIGURE 18 - OUTPUT NOISE versus SOURCE RESISTANCE



TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25^\circ\text{C}$, unless otherwise noted)

FIGURE 19 – POWER DISSIPATION versus TEMPERATURE

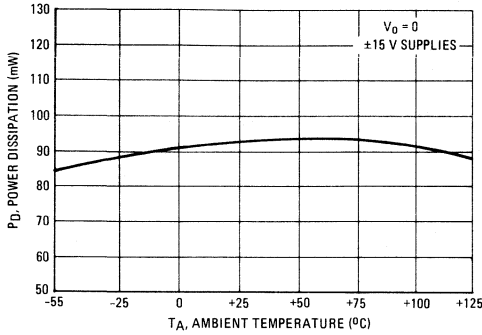


FIGURE 20 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

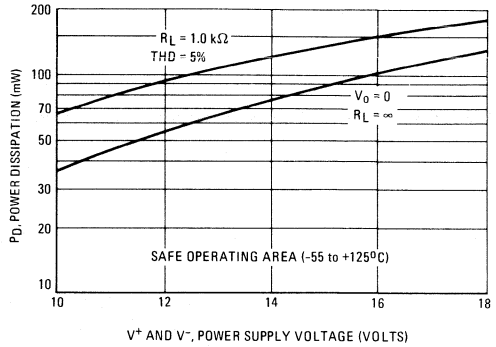


FIGURE 21 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

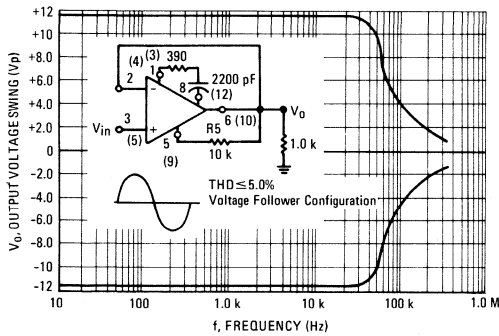


FIGURE 22 – COMMON-MODE INPUT VOLTAGE versus SUPPLY VOLTAGE

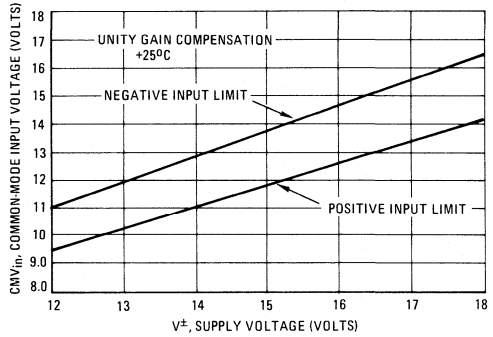


FIGURE 23 – COMMON-MODE REJECTION RATIO versus FREQUENCY

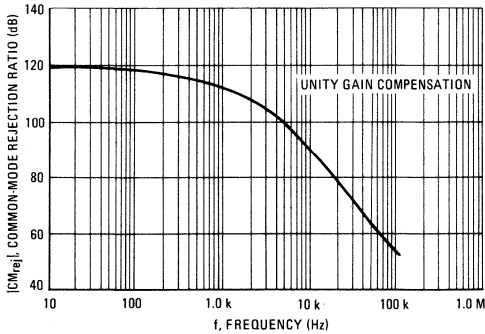
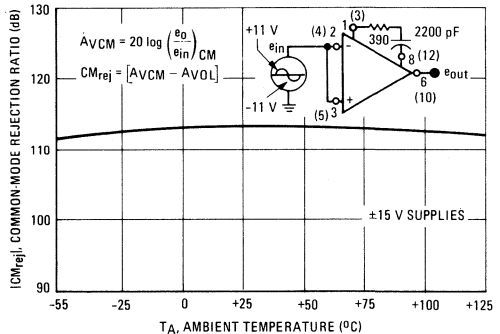
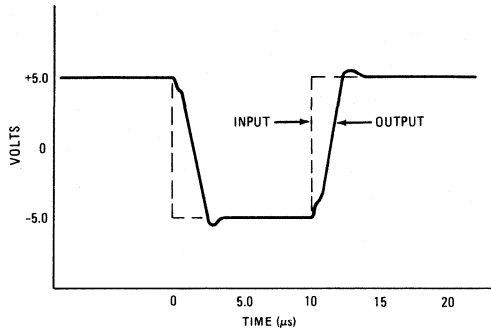


FIGURE 24 – COMMON-MODE REJECTION RATIO versus TEMPERATURE



Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.

FIGURE 25 - VOLTAGE-FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.

FIGURE 26 - VOLTAGE FOLLOWER

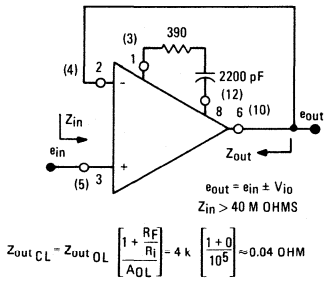


FIGURE 27 - DIFFERENTIAL AMPLIFIER

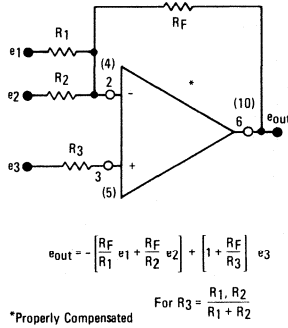


FIGURE 28 - SUMMING AMPLIFIER

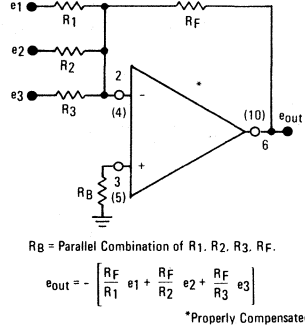
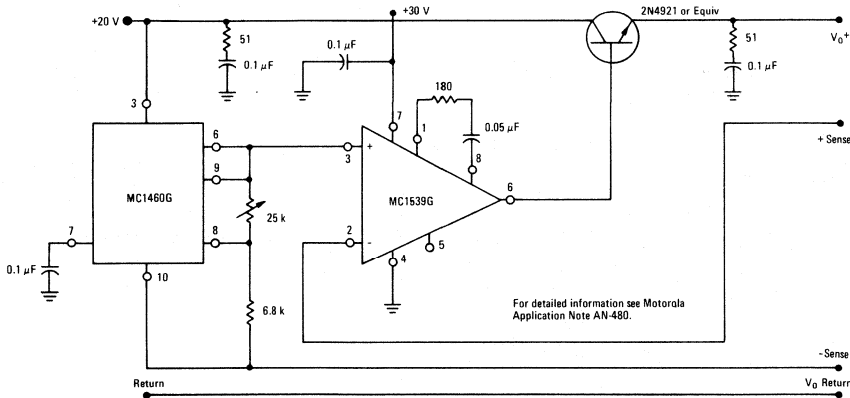


FIGURE 29 - +15 VOLT REGULATOR



TYPICAL APPLICATIONS (continued)

FIGURE 30 – LOAD REGULATION FOR
CIRCUIT OF FIGURE 29

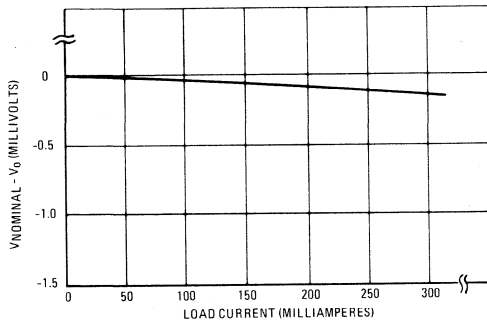
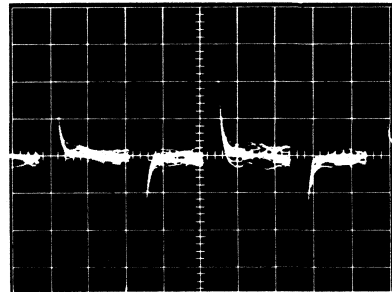


FIGURE 31 – REGULATOR OUTPUT VOLTAGE
(under pulsed load condition)



MC 1540 MC 1440

SENSE AMPLIFIERS

MONOLITHIC SENSE AMPLIFIER

... consisting of a wideband differential amplifier, a dc restoration circuit which also incorporates facilities to externally adjust the threshold, and an MDTL output gate which is strobed from saturated logic. It is designed to detect bipolar differential signals derived by a core memory with cycle times as low as 0.5 μ s.

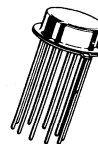
- Differential Threshold Characteristics:
Adjustable Threshold – 10-25 mV
Nominal Threshold – 17 mV @ $V_G = -6$ V
Input Offset Voltage – 1.0 mV typical
Threshold Drift – -10 μ V/ $^{\circ}$ C typical
- Fast Response Time – 20 ns typical
- Short Recovery Time:
50 ns max @ $e_{in} = 1.8$ V Common Mode
50 ns max @ $e_{in} = 400$ mV Differential Mode

CORE MEMORY SENSE AMPLIFIER INTEGRATED CIRCUIT

SILICON
EPITAXIAL PASSIVATED

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

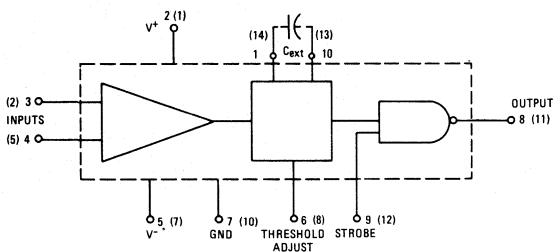
G SUFFIX
METAL PACKAGE
CASE 602B



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

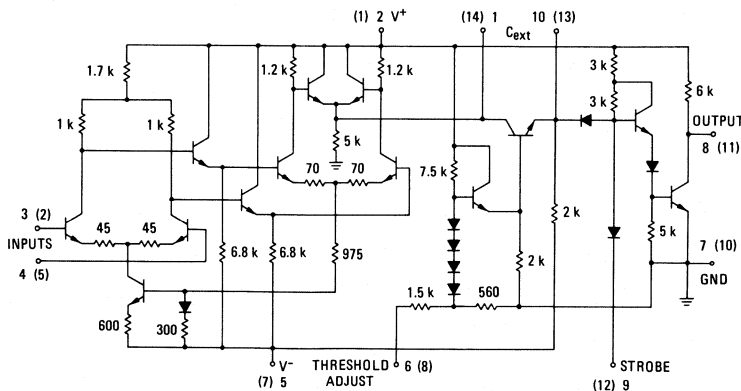


MC1540/MC1440 BLOCK DIAGRAM



Number at end of terminal represents pin number for devices in flat package and metal can. Number in parenthesis represents pin number for dual in-line package.

CIRCUIT SCHEMATIC



Number at end of terminal represents pin number for devices in flat package and metal can. Number in parenthesis represents pin number for ceramic dual in-line package.

See Packaging Information Section for outline dimensions.

MC1540, MC1440 (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|------------|--|--|
| Power Supply Voltage | V^+ | +10 | Vdc |
| | V^- | -10 | Vdc |
| Differential Input Signal | V_{in} | ± 5.0 | Vdc |
| Common Mode Input Voltage | CMV_{in} | ± 5.0 | Vdc |
| Load Current | I_L | 25 | mA |
| Power Dissipation (Package Limitation) | P_D | 680 4.6 500 3.3 625 5.0 | mW mW/ $^\circ\text{C}$ mW mW/ $^\circ\text{C}$ mW mW/ $^\circ\text{C}$ |
| Metal Can | | | |
| Derate above $T_A = +25^\circ\text{C}$ | | | |
| Flat Package | | | |
| Derate above $T_A = +25^\circ\text{C}$ | | | |
| Ceramic Dual In-Line Package | | | |
| Derate above $T_A = +25^\circ\text{C}$ | | | |
| Operating Temperature Range | T_A | 0 to +75 -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS

($V^+ = +6\text{ Vdc} \pm 1\%$, $V^- = -6\text{ Vdc} \pm 1\%$, $C_{ext} = 0.01\ \mu\text{F}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Pin number references are for devices in flat package and metal can.

See block diagram for dual in-line package pin numbers.

| Characteristic | Fig. No. | Symbol | MC1540 | | | MC1440 | | | Unit |
|--|----------|-------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Input Threshold Voltage ($V_G = -6.0\text{ Vdc}$, $T_A = 25^\circ\text{C}$) ($V_G = -6.0\text{ V}$, $T_A = T_{low}^*$) ($V_G = -6.0\text{ V}$, $T_A = T_{high}^*$) | 1 | V_{th} | 14 12 12 | 17 17 17 | 20 24 22 | 12 10 10 | 17 17 17 | 24 30 30 | mV |
| Input Offset Voltage | 1 | V_{io} | - | 1.0 | 5.0 | - | 1.0 | 6.0 | mV |
| Input Bias Current ($V_3 = V_4 = 0$, $T_A = 25^\circ\text{C}$) ($V_3 = V_4 = 0$, $T_A = T_{low}^*$) | 2 | I_b | - | 7.5 | 50 | - | 7.5 | 75 | μA |
| | | | - | - | 100 | - | - | 100 | |
| Input Offset Current | 2 | I_{io} | - | 2.0 | 10 | - | 2.0 | 15 | μA |
| Output Voltage High ($V_3 = V_4 = 0$) | 3 | V_{OH} | 5.9 | - | - | 5.8 | - | - | Vdc |
| Output Voltage Low ($V_3 = V_4 = 0$, $V_{10} = +6.0\text{ Vdc}$, $I_B = 6.0\text{ mAdc}$) ($V_{10} = +6.0\text{ Vdc}$, $I_B = 6.0\text{ mAdc}$, $T_A = T_{high}^*$) | 3 | V_{OL} | - | - | 350 | - | - | 400 | mVdc |
| | | | - | - | 400 | - | - | 450 | |
| Amplifier Voltage Gain ($V_3 = 15\text{ mV peak}$) | 4 | A_V | - | 85 | - | - | 85 | - | - |
| Strobe Load Current ($V_G = 0$) | - | I_S | - | - | 1.2 | - | - | 1.5 | mAdc |
| Strobe Reverse Current ($V_G = +5.0\text{ Vdc}$) ($V_G = +6.0\text{ Vdc}$, $T_A = T_{high}^*$) | - | I_R | - | - | 2.0 | - | - | 5.0 | μAdc |
| | | | - | - | 25 | - | - | 30 | |
| Propagation Delay Input to Amplifier Output ($V_3 = 25\text{ mV pulse}$, $V_G = +2.0\text{ Vdc}$) | 5 | t_{3+10+} | - | 10 | 15 | - | 10 | 20 | ns |
| Input to Gate Output ($V_3 = 25\text{ mV pulse}$, $V_G = +2.0\text{ Vdc}$) | 5 | t_{3+8-} | - | 20 | 30 | - | 20 | 50 | |
| Strobe to Gate Output ($V_3 = V_4 = 0$, $V_G = +2.0\text{ V pulse}$) | 6 | t_{9+8-} | - | 10 | 15 | - | 10 | 30 | |
| Recovery Time Differential Mode ($V_3 = 400\text{ mV pulse}$) | 7 | $t_R(dm)$ | - | 20 | 50 | - | 20 | 90 | ns |
| Common Mode ($V_3 = 1.8\text{ V pulse}$) | 8 | $t_R(cm)$ | - | 20 | 50 | - | 20 | 60 | |
| Power Dissipation | - | P_D | - | 120 | 180 | - | 120 | 250 | mW |

* $T_{low} = -55^\circ\text{C}$ for MC1540 or 0°C for MC1440, $T_{high} = +125^\circ\text{C}$ for MC1540 or $+75^\circ\text{C}$ for MC1440.

- A_V** Amplifier Voltage Gain — the ratio of output voltage at pin 1 to the input voltage at pin 3 or 4
- I_b** Input Bias Current — the average input current defined as $(I_3 + I_4)/2$
- I_{io}** Input Offset Current — the difference between input current values, $|I_3 - I_4|$
- I_R** Strobe Reverse Current — leakage current when the strobe input is high
- I_S** Strobe Load Current — amount of current drain from the circuit when the strobe pin is grounded
- P_D** Power Dissipation — amount of power dissipated in the unit as defined by $|I_2 \times V^+| + |I_5 \times V^-|$
- t_R** Recovery Time — The time that is required for the device to recover from the specified differential and common-mode overload inputs prior to strobe as reference to the 10% point

- t_{x±y±}** Propagation Delay — The time that is required for the output pulse at pin y to achieve 50% of its final value or the 1.5 V level referenced to 50% of the input pulse at pin x. (The + and - denote positive and negative-going pulse transition.)
- V_{OH}** Output Voltage High — high-level output voltage when the output gate is turned off
- V_{OL}** Output Voltage Low — low-level output voltage when the output gate is turned on
- V_{th}** Input Threshold — input pulse amplitude that causes the output to begin saturation
- V_{io}** Input Offset Voltage — the difference in V_{th} at each input

FIGURE 1 — INPUT THRESHOLD AT OUTPUT VOLTAGE SWING FROM V_{OL} TO V_{OH}

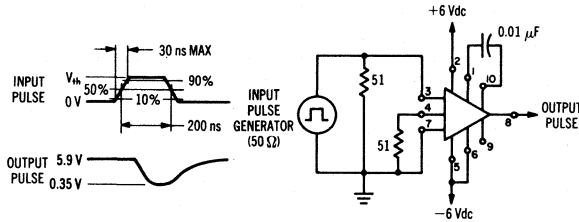


FIGURE 3 — OUTPUT VOLTAGE LEVELS

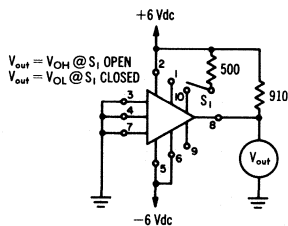


FIGURE 5 — PROPAGATION DELAY (STROBE HIGH)

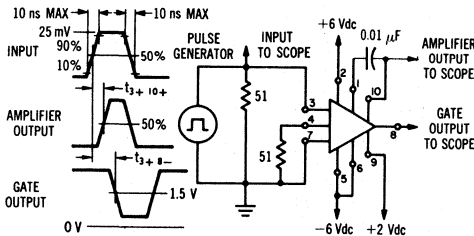


FIGURE 2 — INPUT BIAS CURRENT TEST CIRCUIT

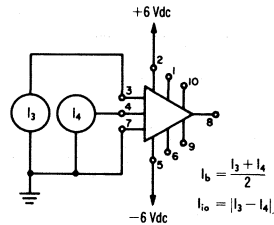


FIGURE 4 — AMPLIFIER VOLTAGE GAIN

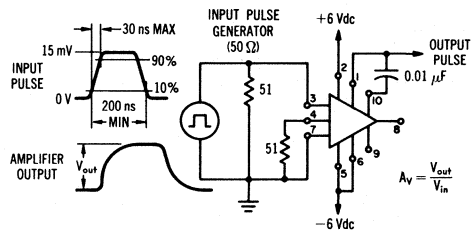


FIGURE 6 — PROPAGATION DELAY (STROBE INPUT)

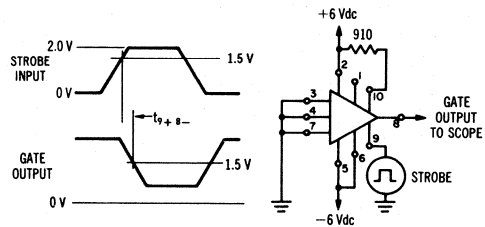


FIGURE 7 – DIFFERENTIAL MODE RECOVERY TIME TEST CIRCUIT

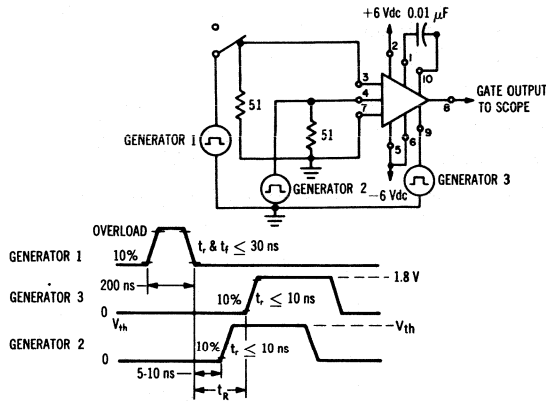


FIGURE 8 – COMMON MODE RECOVERY TIME TEST CIRCUIT

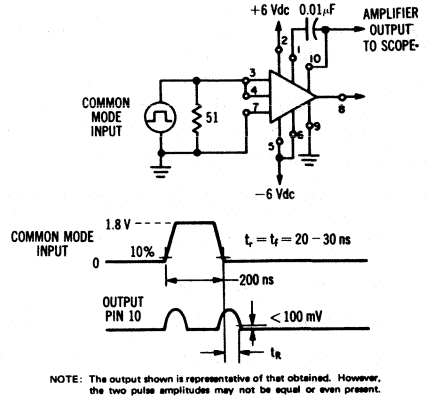


FIGURE 9 – TYPICAL TRANSFER CHARACTERISTICS

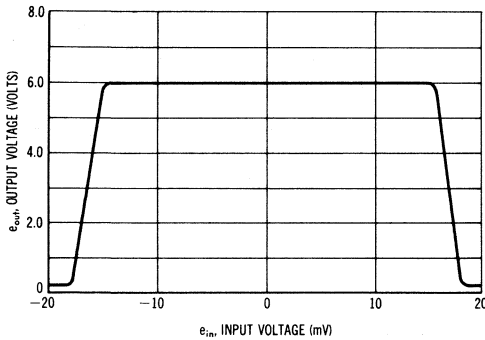


FIGURE 10 – TYPICAL THRESHOLD versus TEMPERATURE

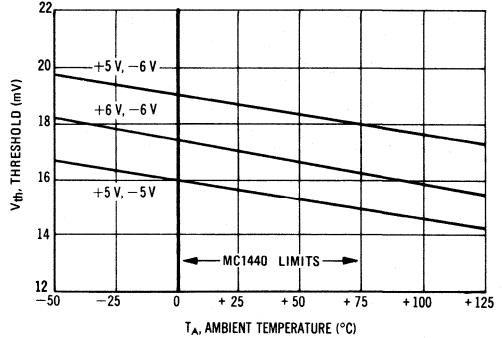


FIGURE 11 – TYPICAL THRESHOLD versus POWER SUPPLIES
 $T_A = +25^{\circ}$ C (Threshold Adjust Attached to V^-)

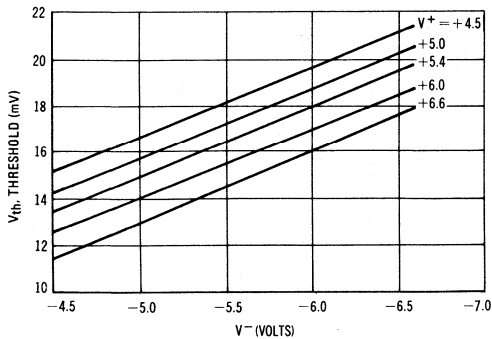
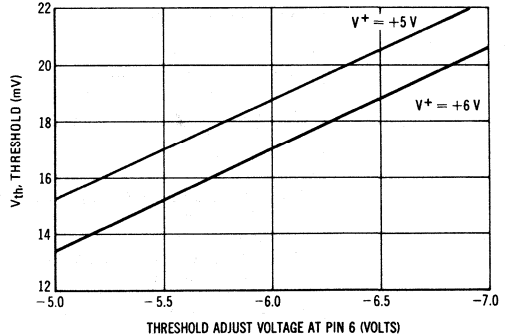


FIGURE 12 – TYPICAL THRESHOLD versus THRESHOLD VOLTAGE ADJUST FOR $V^+ = 6.0$ V



For a more detailed discussion regarding application of sense amplifiers, see Motorola Application Note AN-245, "The MC1540 – An Integrated Core Memory Sense Amplifier."

MC1541 MC1441

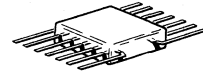
SENSE AMPLIFIERS

Dual-channel gated sense amplifier with separate wideband differential input amplifiers. Either input can be gated on from saturated logic levels. The sense amplifier features adjustable threshold, saturated logic output levels, and a strobe input that accommodates saturated logic levels. Designed to detect bipolar signals from either of two sense lines. Operates with core memory cycle times less than 0.5 μ s.

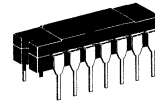
Typical Amplifier Features:

- Nominal Threshold – 17 mV
- Input Offset Voltage – 1.0 mV typical
- Propagation Delay
 - Input to Gate-Output – 20 ns
 - Input to Amplifier-Output – 10 ns
 - Gate Response Time – 15 ns
 - Strobe Response Time – 15 ns
- Common Mode Input Range – 1.5 Volts
- Differential Mode Input Range
 - With Gate On – 600 mV
 - With Gate Off – 1.5 Volts
- Power Dissipation – 140 mW typical

See Packaging Information Section for outline dimensions.



F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

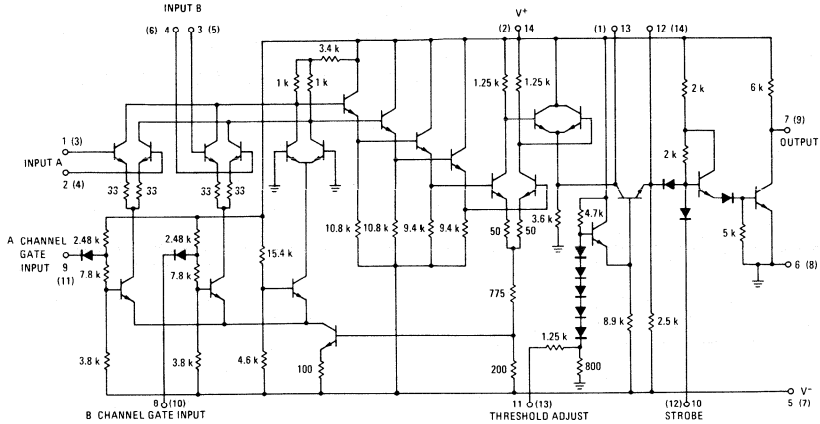


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS

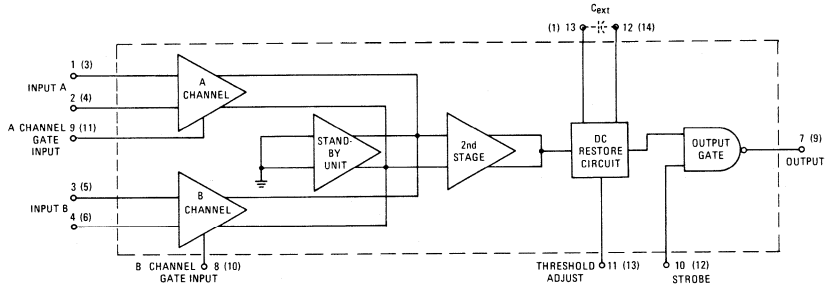
| Rating | Symbol | Value | Unit |
|--|-------------------|-------------|-------|
| Power Supply Voltage | V ⁺ | +10 | Vdc |
| | V ⁻ | -10 | Vdc |
| Differential Input Signal | V _{in} | ±5 | Vdc |
| Common Mode Input Voltage | CMV _{in} | ±5 | Vdc |
| Load Current | I _L | 25 | mA |
| Power Dissipation (Package Limitation) | P _D | 500 | mW |
| | | 3.3 | mW/°C |
| | | 600 | mW |
| | | 4.8 | mW/°C |
| Operating Temperature Range | T _A | -55 to +125 | °C |
| | | 0 to +75 | |
| | | | |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

CIRCUIT SCHEMATIC



Number at terminal end denotes pin number for flat (F) package.
 Number in parenthesis denotes pin number for dual in-line ceramic (L) package.

LOGIC DIAGRAM



Number at terminal end denotes pin number for flat package. Number in parenthesis denotes pin number for dual in-line package.

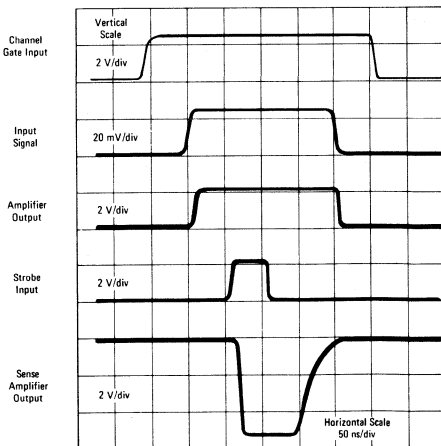


FIGURE 1 – TYPICAL OPERATION

MC1541, MC1441 (continued)

ELECTRICAL CHARACTERISTICS

(V⁺ = +5.0 Vdc ± 1%, V⁻ = -5.0 Vdc ± 1%, V_{in}(pin 11) = -5.0 Vdc ± 1%, C_{ext} = 0.01 μF, T_A = 25°C unless otherwise noted)
 (T_{low} = -55°C for MC1541 or 0°C for MC1441, T_{high} = +125°C for MC1541 or +75°C for MC1441. Pin numbers referenced in table denote flat package; to ascertain corresponding pin number for dual in-line package refer to the equivalent circuit.)

| Characteristic | Fig. No. | Symbol | Min | Typ | Max | Unit |
|---|----------|------------------------------------|----------------|---------------|----------------|-----------|
| Input Threshold Voltage (T _A = +25°C) (T _{low} ≤ T _A ≤ T _{high}) | 8 | V _{th} | 14 13 12 | 17 - 17 | 20 21 22 | mV |
| Input Offset Voltage | 8 | V _{io} | - | 1.0 | 6.0 | mV |
| Input Bias Current (V ₁ = V ₂ = V ₃ = V ₄ = 0) (V ₁ = V ₂ = V ₃ = V ₄ = 0, T _A = T _{low}) | 9 | I _b | - | 5.0 | 25 50 | μA |
| Input Offset Current | 9 | I _{io} | - | 1.0 | 2.0 | μA |
| Output Voltage High (V ₁ = V ₂ = V ₃ = V ₄ = 0, I _{OH} = 200 μA) | | V _{OH} | 3.0 | - | - | Vdc |
| Output Voltage Low (V ₁ = V ₂ = V ₃ = V ₄ = 0, V ₁₂ = +5.0 Vdc, I ₇ = 10 mAdc) (V ₁₂ = +5.0 Vdc, I ₇ = 10 mAdc, T _A = +T _{high}) | 10 | V _{OL} | - | - | 350 400 | mVdc |
| Strobe Load Current (V ₁₀ = 0) | | I _S | - | - | 1.5 | mAdc |
| Strobe Reverse Current (V ₁₀ = +5.0 Vdc) (V ₁₀ = +5.0 Vdc, T _A = T _{high}) | | I _{SR} | - | - | 2.0 25 | μA |
| Input Gate Voltage Low (V ₁ = V ₃ = 25 mVdc, V ₂ = V ₄ = 0) | 11 | V _{GL} | - | 0.7 | - | Vdc |
| Input Gate Voltage High (V ₁ = V ₃ = 25 mVdc, V ₂ = V ₄ = 0) | 11 | V _{GH} | - | 1.6 | - | Vdc |
| Input Gate Load Current (V ₈ or V ₉ = 0) | | I _G | - | - | 2.5 | mA |
| Input Gate Reverse Current (V ₈ or V ₉ = 5.0 Vdc) (T _A = 25°C) (T _A = T _{high}) | | I _{GR} | - | - | 2.0 25 | μA |
| Common Mode Range Input Gate High Input Gate Low | 13 | V _{CM} | - | ±1.5 ±1.5 | - | Vdc |
| Differential Mode Range Input Gate High Input Gate Low | 14 | V _{DH} V _{DL} | - | ±600 ±1.5 | - | mV Vdc |
| Power Dissipation | | P _D | - | 140 | 180 | mW |

SWITCHING CHARACTERISTICS

| Characteristic | Fig. No. | Symbol | Min | Typ | Max | Unit |
|---|----------|------------------|-----|----------|----------|------|
| Propagation Delay Input to Amplifier Output (V ₁ = 25 mV pulse, V ₁₀ = +2.0 Vdc) | 8 | t _{IA} | - | 10 | 15 | ns |
| Input to Output (V ₁ = 25 mV pulse, V ₁₀ = +2.0 Vdc) | 8 | t _{IO} | - | 20 | 30 | |
| Strobe to Output (V ₁ = V ₂ = V ₃ = V ₄ = 0, V ₁₀ = +2.0 V pulse) | 12 | t _{SO} | - | 15 | 20 | |
| Gate Input to Amplifier Input (V ₁ = 25 mV pulse, V ₉ = 2.0 V pulse) | 11 | t _{GI} | - | 10 | 15 | |
| Gate Input to Amplifier Output (V ₁ = 25 mVdc, V ₉ = 2.0 V pulse) | 11 | t _{GA} | - | 30 | 35 | |
| Recovery Time Differential Mode Input Gate High } V ₁ or V ₃ = 400 mV pulse Input Gate Low } | 14 | t _{DR} | - | 30 0 | - | ns |
| Common Mode Input Gate High } V ₁ or V ₃ = 1.5 V pulse Input Gate Low } | 13 | t _{CMR} | - | 15 15 | 30 30 | |

MC1541, MC1441 (continued)

FIGURE 2 – TYPICAL INPUT THRESHOLD versus TEMPERATURE

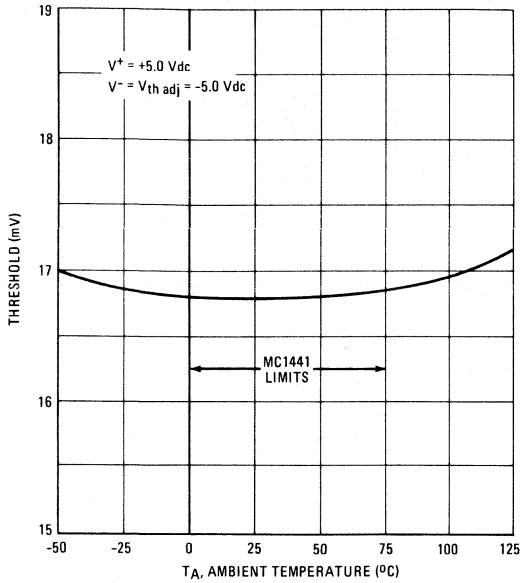


FIGURE 3 – TYPICAL THRESHOLD versus THRESHOLD VOLTAGE ADJUST

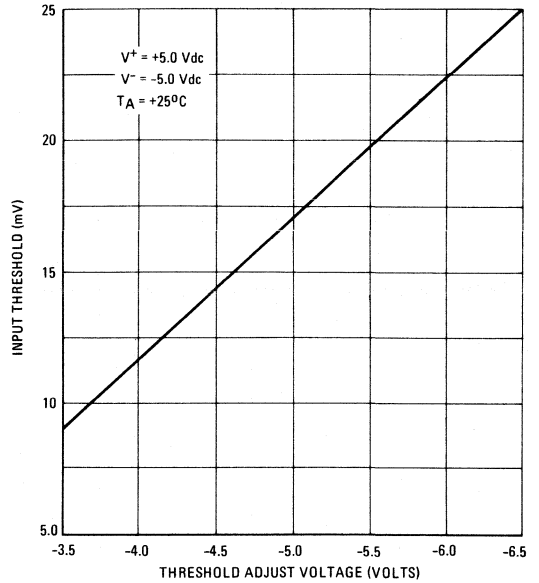


FIGURE 4 – TYPICAL INPUT THRESHOLD versus V^-

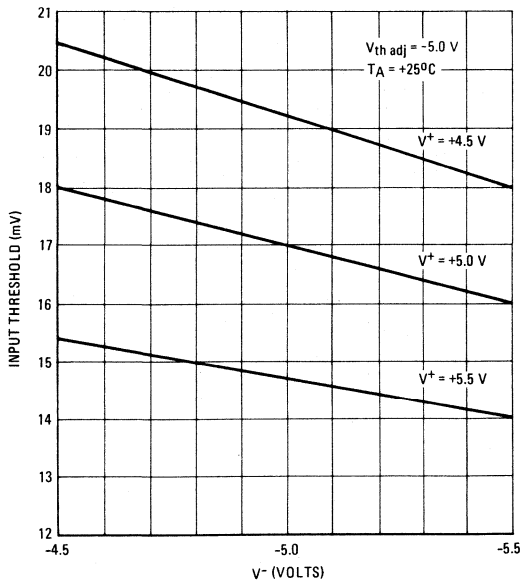


FIGURE 5 – TYPICAL INPUT THRESHOLD versus INPUT PULSE WIDTH

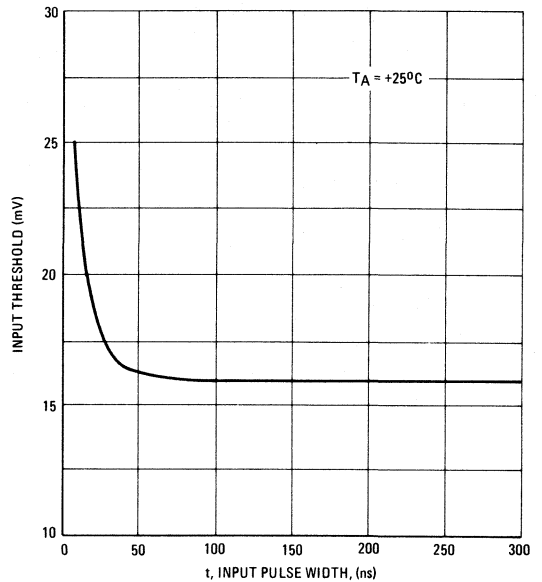


FIGURE 6 – INPUT-OUTPUT TRANSFER CHARACTERISTICS

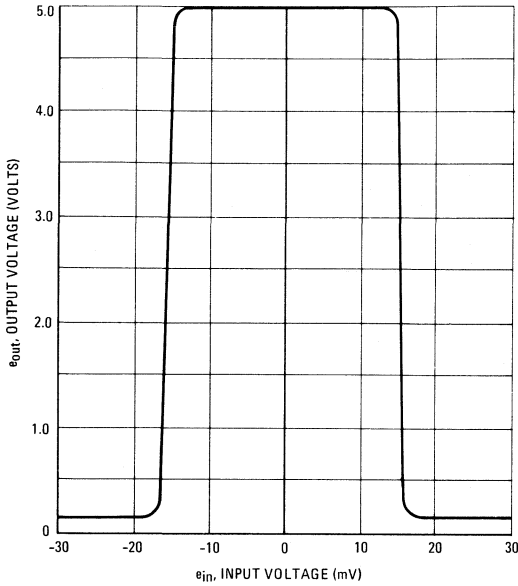


FIGURE 7 – CHANNEL GATE INPUT-AMPLIFIER OUTPUT TRANSFER CHARACTERISTICS

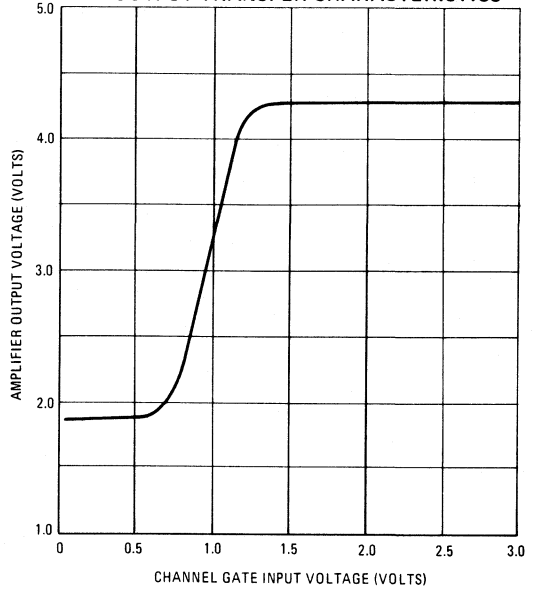
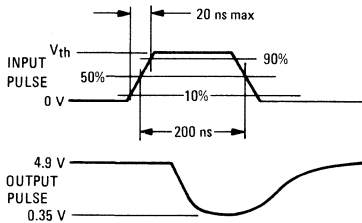
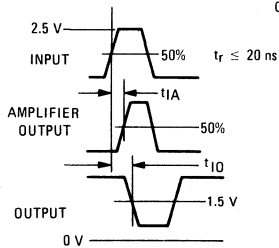


FIGURE 8 – INPUT THRESHOLD FOR OUTPUT VOLTAGE SWING FROM V_{OH} TO V_{OL} PROPAGATION DELAY FROM INPUT TO OUTPUT

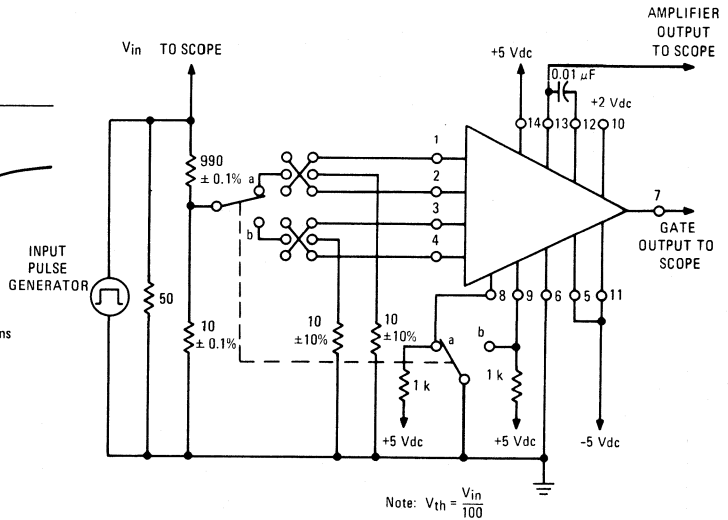
(a) Threshold Test Waveforms



(c) Waveforms for Propagation Delay Test

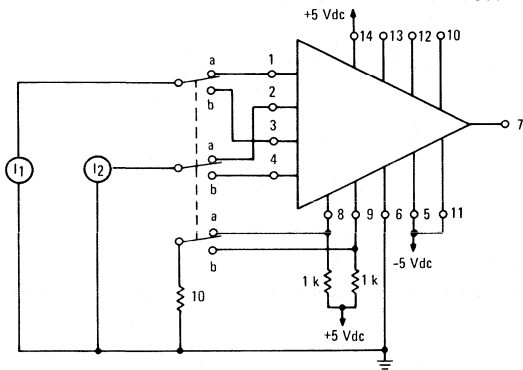


(b) Test Circuit



Number at terminal end denotes the pin number for flat package only; to ascertain the corresponding pin number for the dual in line packages refer to the circuit schematic on the second page.

FIGURE 9 – INPUT BIAS CURRENT TEST CIRCUIT



$$\frac{I_1 + I_2}{2} = I_b \text{ for "A" channel when switch is in "a" position}$$

$$= I_b \text{ for "B" channel when switch is in "b" position}$$

$$|I_1 - I_2| = I_{io}$$

FIGURE 10 – OUTPUT VOLTAGE LEVELS

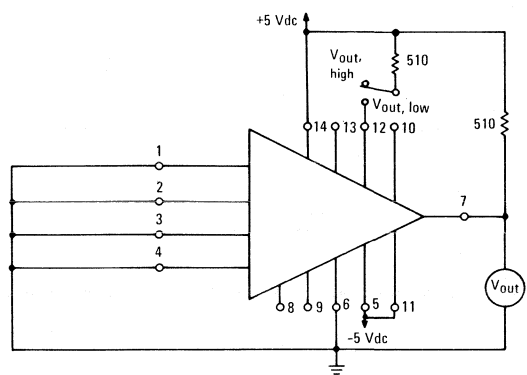
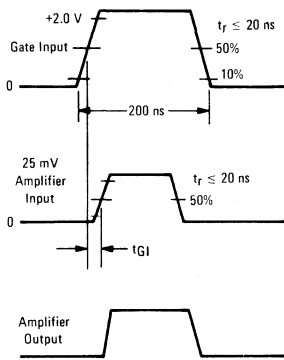
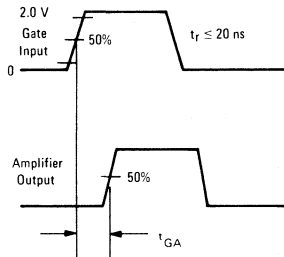


FIGURE 11 – MINIMUM TIME FROM CHANNEL GATE INPUT TO AMPLIFIER INPUT
PROPAGATION DELAY FROM CHANNEL GATE INPUT TO AMPLIFIER OUTPUT

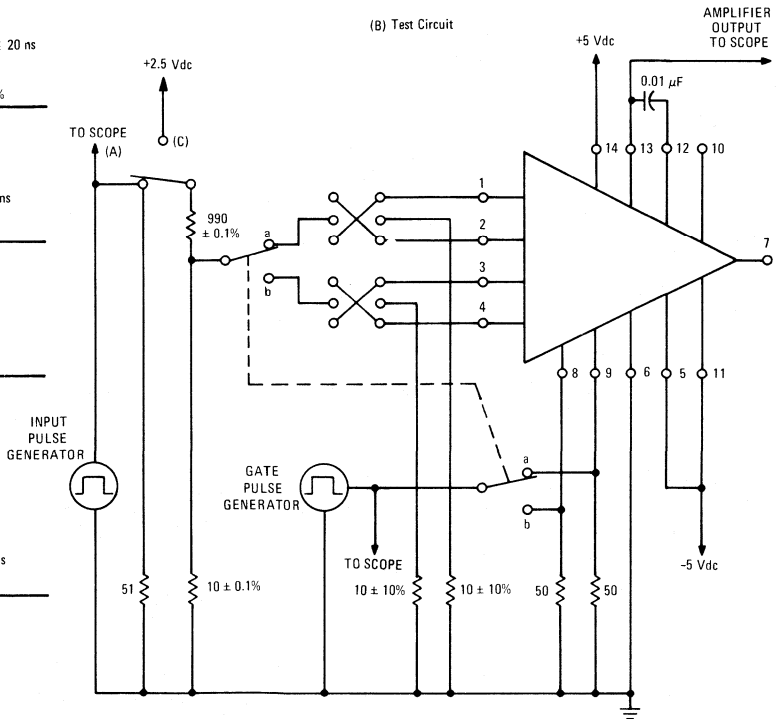
(A) Minimum Time from Gate Input to Amplifier Input - tGI
(See Definitions)



(C) Propagation Delay from Channel Gate Input to Amplifier Output



(B) Test Circuit



(Pin numbers shown on this page denote the pin numbers for the flat package only; to ascertain the corresponding pin numbers for the dual in-line package, refer to the circuit schematic on the second page.)

MC1541, MC1441 (continued)

FIGURE 12 – PROPAGATION DELAY FROM STROBE INPUT TO OUTPUT

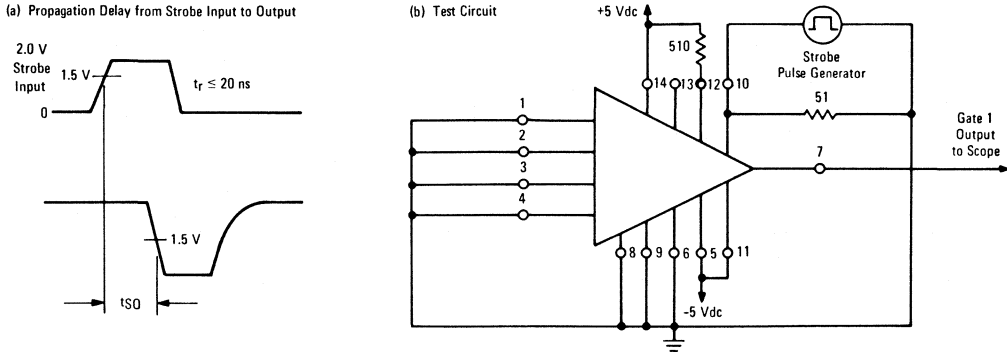


FIGURE 13 – COMMON-MODE RECOVERY AND COMMON-MODE RANGE

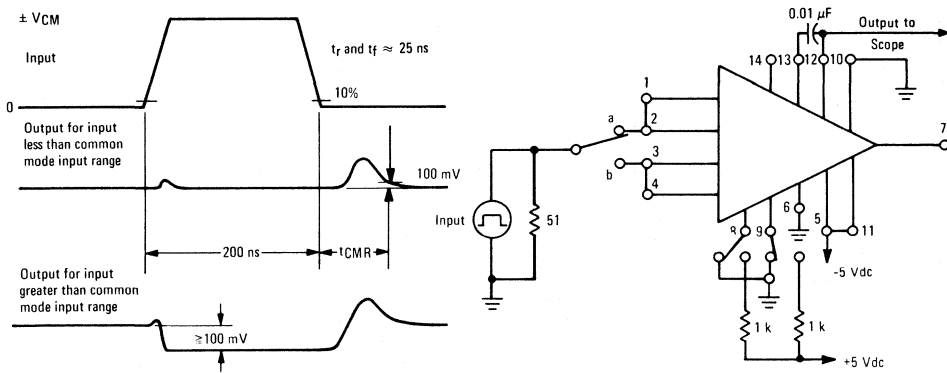
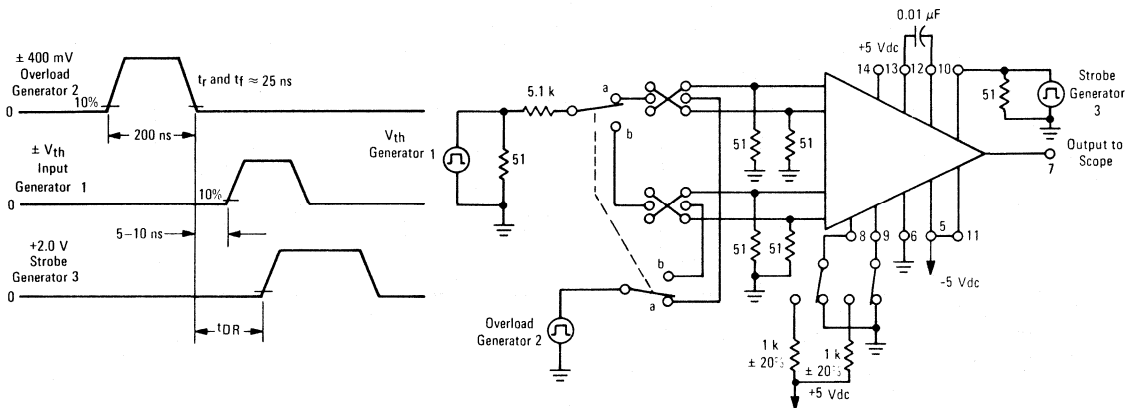


FIGURE 14 – DIFFERENTIAL RECOVERY AND DIFFERENTIAL RANGE



(Pin numbers shown on this page denote the pin numbers for the flat package only; to ascertain the corresponding pin numbers for the dual in-line package, refer to the circuit schematic on the second page.)

DEFINITIONS

Pin numbers referenced in the definitions below denote the flat package only; to ascertain the corresponding pin number for the dual in-line package refer to the circuit schematic.

| | |
|--|--|
| <p>I_B Input Bias Current – The average input current defined as $(I_1 + I_2 + I_3 + I_4)/4$.</p> <p>I_G Channel Gate Load Current – The amount of current drain from the circuit when the channel gate input (Pin 8 or 9) is grounded.</p> <p>I_{GR} Channel Gate Reverse Current – The leakage current when the channel gate input (Pin 8 or 9) is high.</p> <p>I_{io} Input Offset Current – The difference between amplifier input current values $I_1 - I_2$ or $I_3 - I_4$.</p> <p>I_S Strobe Load Current – The amount of current drain from the circuit when the strobe pin is grounded.</p> <p>I_{SR} Strobe Reverse Current – The leakage current when the strobe input is high.</p> <p>P_D Power Dissipation – The amount of power dissipated in the unit.</p> <p>t_{CMR} Common Mode Recovery Time – The time required for the voltage at pin 12 to be within 100 mV of the dc value (after overshoot or ringing) as referenced to the 10% point of the trailing edge of a common mode overload signal.</p> <p>t_{DR} Differential Recovery Time – The time required for the device to recover from the specified differential input prior to strobe enable as referenced to the 10% point of the trailing edge of an input pulse. The device is considered recovered when the threshold with the overload signal applied is within 1.0 mV of the threshold with no overload input.</p> <p>t_{GI} Minimum Time Between Channel Gate Input and Signal Input – The minimum time between 50% point of channel gate input (Pin 8 or 9) and 50% point of signal input (Pins 1, 2, 3, or 4) that still allows a full width signal at amplifier output.</p> <p>t_{GA} Propagation Delay, Channel Gate Input to Amplifier Output – The time required for the amplifier output at pin 13 to reach 50% of its final value as referenced to 50% of the input gate pulse at pin 8 or 9 (Amplifier input = 25 mVdc).</p> <p>t_{IA} Propagation Delay, Input to Amplifier Output – The time required for the amplifier output</p> | <p>pulse at pin 13 to achieve 50% of its final value referenced to 50% of the input pulse at pins 1 and 2 or 3 and 4.</p> <p>t_{IO} Propagation Delay, Input to Output – The time required for the gate output pulse at pin 7 to reach the 1.5 Volt level as referenced to 50% of the input pulse at pins 1 and 2 or 3 or 4.</p> <p>t_{SO} Strobe Propagation Delay to Output – The time required for the output pulse at pin 7 to reach the 1.5 Volt level as referenced to the 1.5 Volt level of the strobe input at pin 10.</p> <p>V_{CM} Maximum Common Mode Input Range – The common mode input voltage which causes the output voltage level of the amplifier to decrease by 100 mV. (This is independent of the channel gate input level.)</p> <p>V_{DH} Maximum Differential Input Range, Gate Input High – The differential input which causes the input stage to begin saturation.</p> <p>V_{DL} Maximum Differential Input Range, Gate Input Low – The differential input signal which causes the output voltage level of the amplifier to decrease by 100 mV.</p> <p>V_{GH} Channel Gate Input Voltage High – Gate pulse amplitude that allows the amplifier output pulse to just reach 100% of its final value. (Amplifier input is set at 25 mVdc).</p> <p>V_{GL} Channel Gate Input Voltage Low – Gate pulse amplitude that allows the amplifier output to just reach a 100 mV level. (Amplifier input is set at 25 mVdc).</p> <p>V_{io} Input Offset Voltage – The difference in V_{th} between inputs at pins 1 and 2 or 3 and 4.</p> <p>V_{OH} Output Voltage High – The high-level output voltage when the output gate is turned off.</p> <p>V_{OL} Output Voltage Low – The low-level output voltage when the output gate is saturated and the output sink current is 10 mA.</p> <p>V_{th} Input Threshold – Input pulse amplitude at pins 1, 2, 3 or 4 that causes the output gate to just reach V_{OL}.</p> |
|--|--|

MC1543L

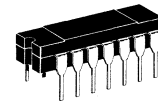
DUAL SENSE AMPLIFIER

DUAL MECL CORE-MEMORY SENSE AMPLIFIER

A dual dc coupled sense amplifier. Output levels are compatible with emitter coupled logic levels. MC1543L offers adjustable threshold and excellent threshold stability over a wide range of power-supply voltage variation.

Typical Amplifier Features:

- Input Threshold Adjustable from 10 to 40 mV (Positive or Negative Signals)
- Both OR and NOR Outputs Available
- Low Power Dissipation
- Threshold Insensitive to + or - Supply Variation
- Each Amplifier is Separately Strobed

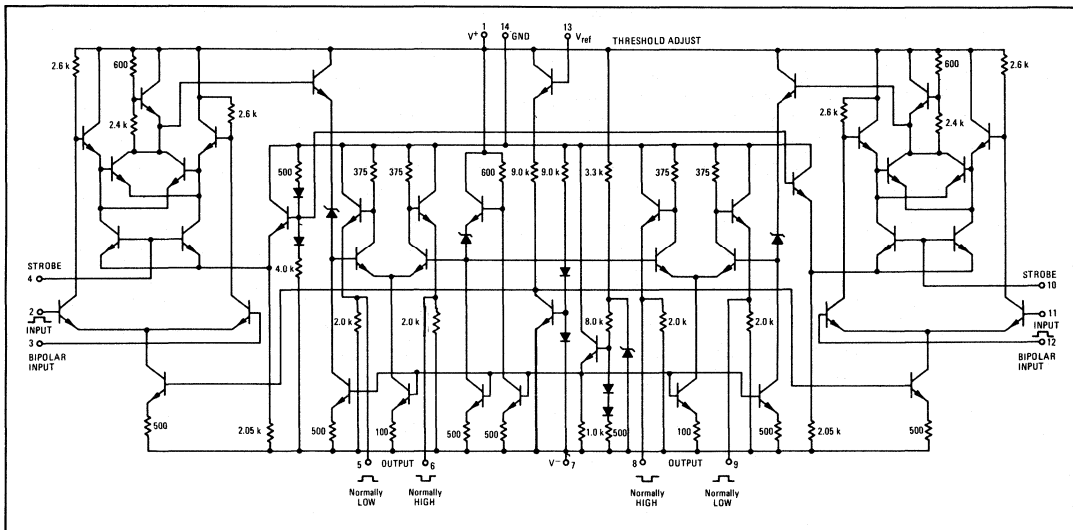


CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|----------------|-------------|----------------------------|
| Power Supply Voltage | V^+ V^- | +10 -10 | Vdc Vdc |
| Differential Input Signal | V_{in} | ± 5.0 | Vdc |
| Common Mode Input Voltage | CMV_{in} | ± 5.0 | Vdc |
| Load Current | I_L | 25 | mA |
| Power Dissipation (Package Limitation) | P_D | 1000 6.7 | mW mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

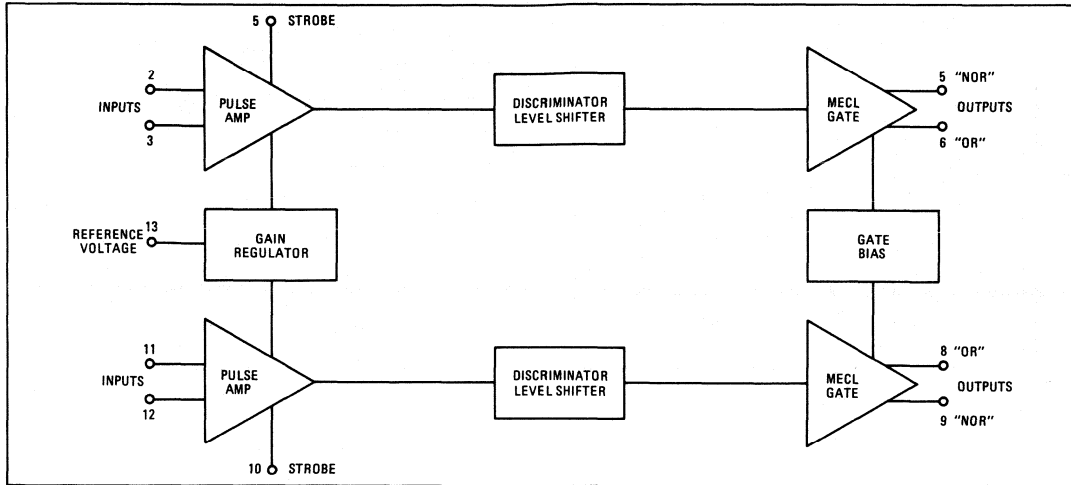
CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MC1543L (continued)

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (Each Amplifier)

($V^+ = +5.0 \text{ Vdc} \pm 5\%$, $V^- = -5.2 \text{ Vdc} \pm 5\%$, $V_{ref} = 0.54 \text{ V} \pm 1\%$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Fig. No. | Symbol | Min | Typ | Max | Unit |
|---|----------|-----------|-------|-------|-------|-----------------|
| Input Threshold Voltage | 8 | V_{th} | 17 | 20 | 23 | mV |
| Power Supply Currents ($V_2 = V_3 = V_{11} = V_{12} = V_{14} = 0$) | 6 | I_{CC} | — | 9.5 | 12 | mAdc |
| | 6 | I_{EE} | — | 26.5 | 33 | mAdc |
| Input Bias Current | 7 | I_b | — | 3.5 | 10 | μAdc |
| Input Offset Current | 7 | I_{io} | — | 0.05 | 0.5 | μAdc |
| Output Voltage High | 9 | V_{OH} | -0.85 | -0.8 | -0.67 | Vdc |
| Output Voltage Low | 9 | V_{OL} | — | -1.7 | -1.46 | Vdc |
| Strobe Threshold Level | 10 | V_{ST} | — | -1.30 | — | Vdc |
| Strobe Input Current High | 10 | I_{SH} | — | 25 | 50 | μAdc |
| Strobe Input Current Low | 10 | I_{SL} | — | 0.01 | 0.1 | μAdc |
| Input Common Mode Range | 14 | V_{CM} | 3.0 | 4.0 | — | Vdc |
| Input Threshold Range (by varying V_{ref}) | 8 | V_{thR} | — | 10-40 | — | mV |
| Power Dissipation | 6 | P_D | — | 185 | 230 | mW |
| Reference Supply Input Current (Pin 13) | 6 | I_{ref} | — | 10 | 40 | μA |

SWITCHING CHARACTERISTICS

| | | | | | | |
|--|----|-----------|---|-----|----|----|
| Propagation Delay (Input to Output) | 11 | t_{IO} | — | 28 | 35 | ns |
| Propagation Delay (Strobe to Output) | 12 | t_{SO} | — | 16 | 20 | ns |
| Strobe Release Time | 12 | t_{SR} | — | 18 | 30 | ns |
| Recovery Time (Differential Mode) ($e_{in} = 400 \text{ mVdc}$) | 13 | t_{DR} | — | 10 | 15 | ns |
| Recovery Time (Common Mode) ($e_{in} = 4.0 \text{ Vdc}$) | 14 | t_{CMR} | — | 3.0 | 15 | ns |
| Strobe Width Minimum | 12 | t_S | — | 8.0 | — | ns |

TEMPERATURE TESTS (-55°C to +125°C)

| | | | | | | | |
|-------------------------|---|---|----------|------|------|-----|-----------------|
| Input Threshold Voltage | $\begin{cases} (-55^\circ\text{C}) \\ (+125^\circ\text{C}) \end{cases}$ | 8 | V_{th} | 18 | 21.5 | 25 | mV |
| | | | | 15 | 18.5 | 22 | |
| Input Bias Current | | 7 | I_b | 2.2 | 7.0 | 20 | μAdc |
| Input Offset Current | | 7 | I_{io} | 0.02 | 0.1 | 1.0 | μAdc |

TYPICAL CHARACTERISTICS

FIGURE 1 – TYPICAL INPUT THRESHOLD versus TEMPERATURE

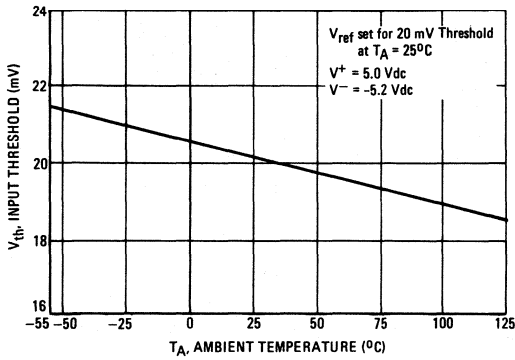


FIGURE 2 – TYPICAL INPUT THRESHOLD versus REFERENCE VOLTAGE

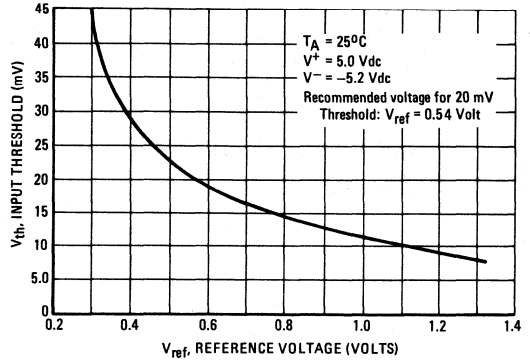


FIGURE 3A – TYPICAL INPUT THRESHOLD versus V+

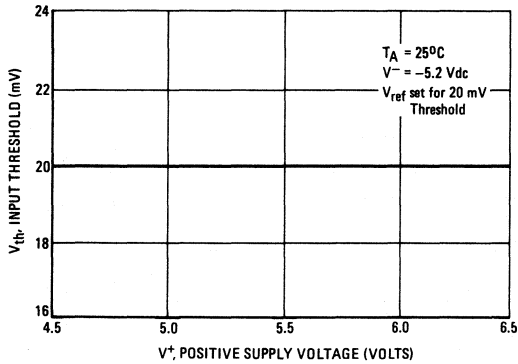


FIGURE 3B – TYPICAL INPUT THRESHOLD versus V-

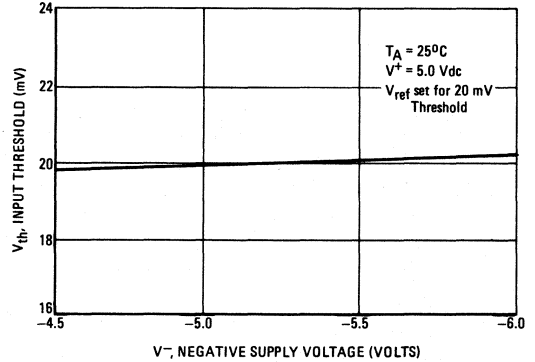


FIGURE 4 – TYPICAL INPUT THRESHOLD versus INPUT PULSE WIDTH

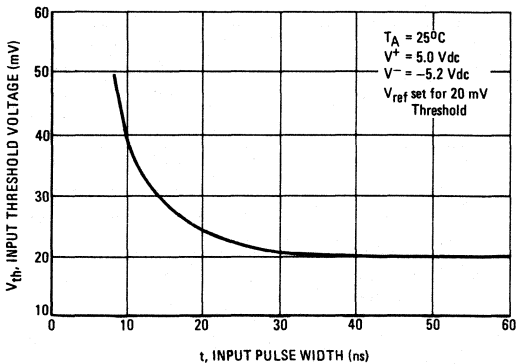
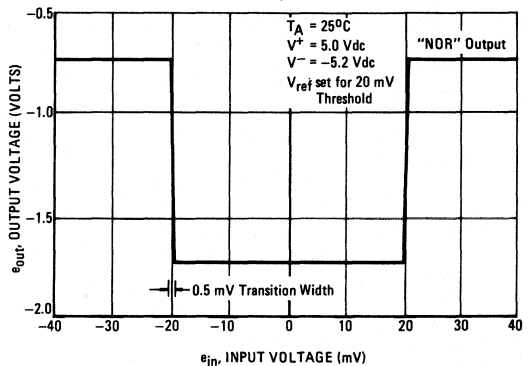


FIGURE 5 – INPUT-OUTPUT TRANSFER CHARACTERISTICS (one output)



7

MC1543L (continued)

FIGURE 6 - POWER SUPPLY CURRENT DRAIN

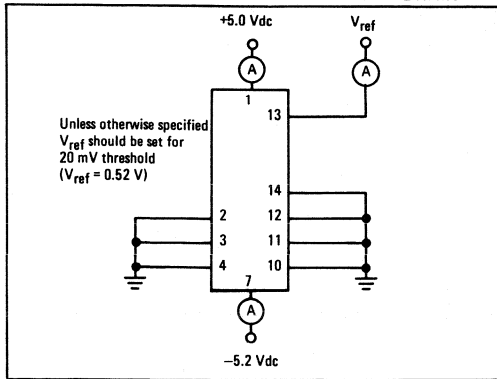


FIGURE 7 - INPUT BIAS CURRENT INPUT OFFSET CURRENT

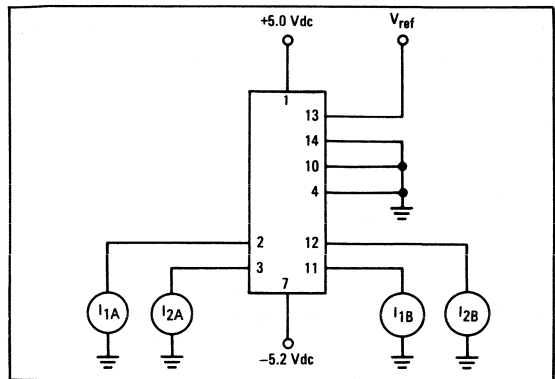


FIGURE 8 - INPUT THRESHOLD LEVEL

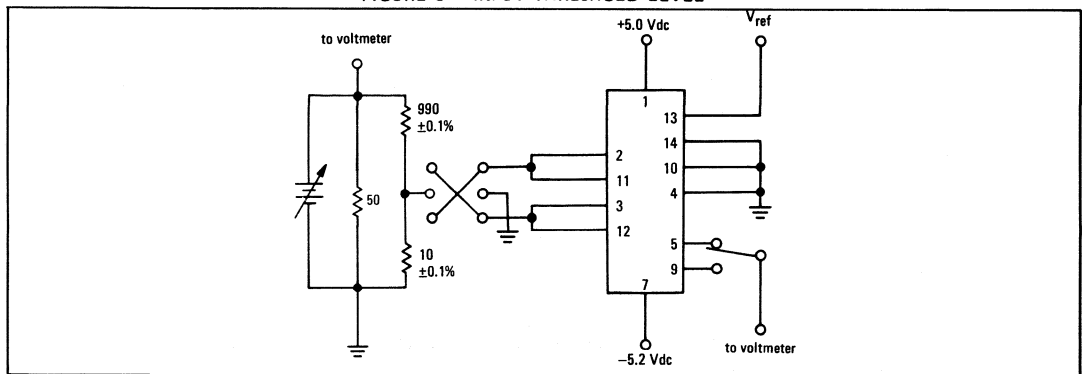


FIGURE 9 - OUTPUT VOLTAGE LEVELS

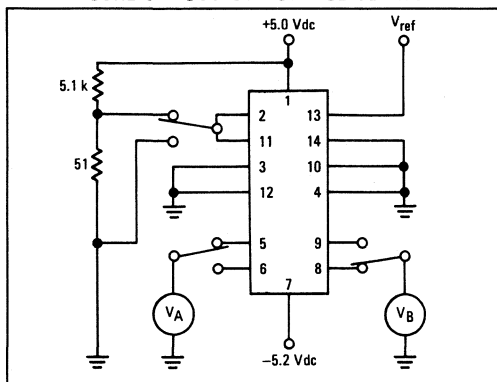


FIGURE 10 - STROBE THRESHOLD LEVEL STROBE INPUT CURRENTS

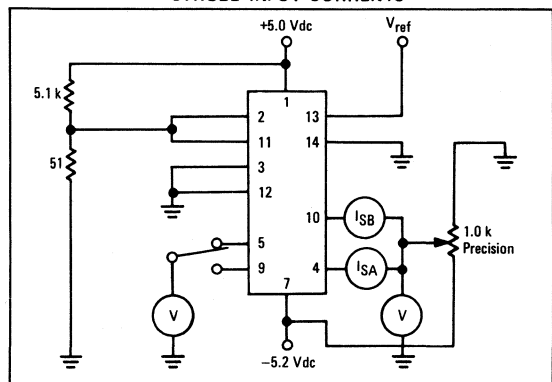


FIGURE 11 – PROPAGATION DELAY –
INPUT TO OUTPUT

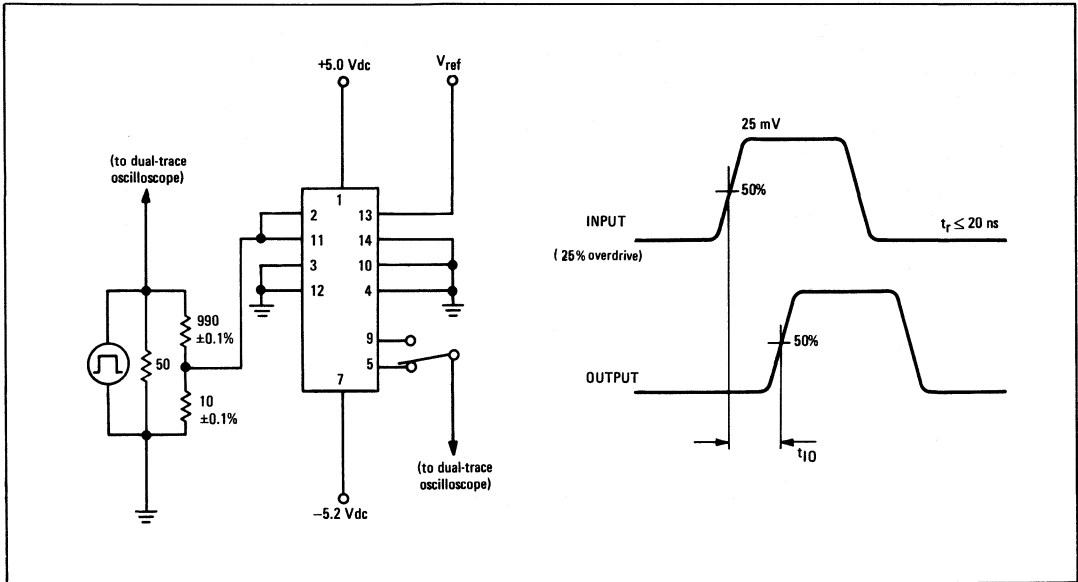
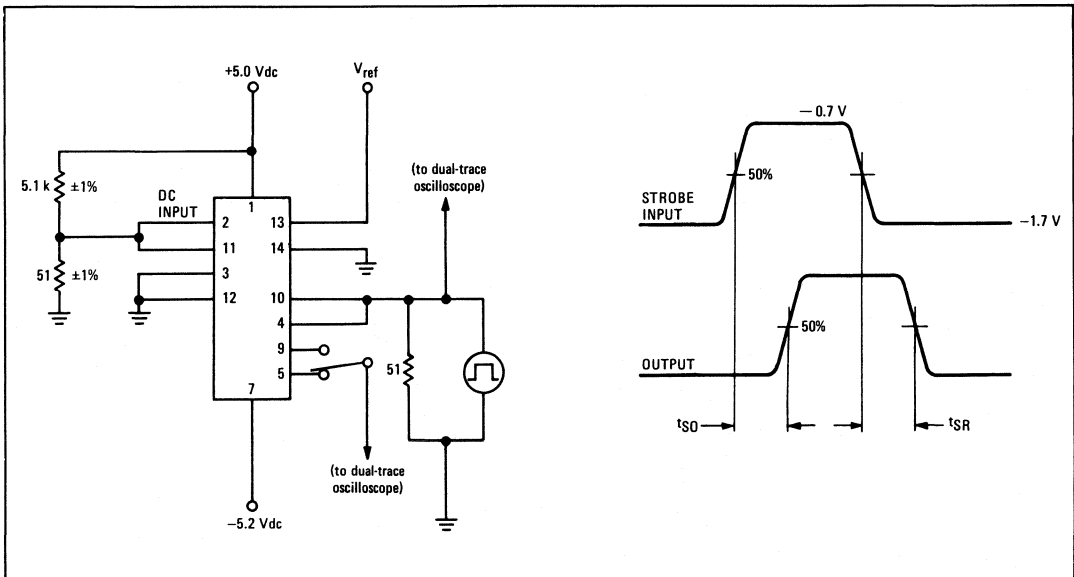


FIGURE 12 – PROPAGATION DELAY –
STROBE TO OUTPUT and STROBE RELEASE TIME



7

FIGURE 13 – DIFFERENTIAL MODE RECOVERY TIME
(See definition section)

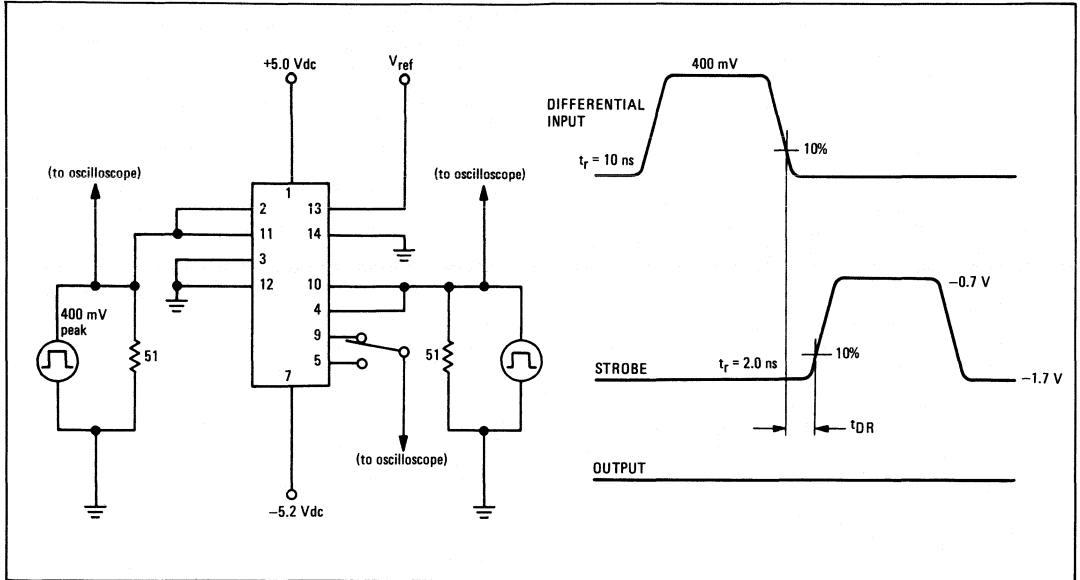
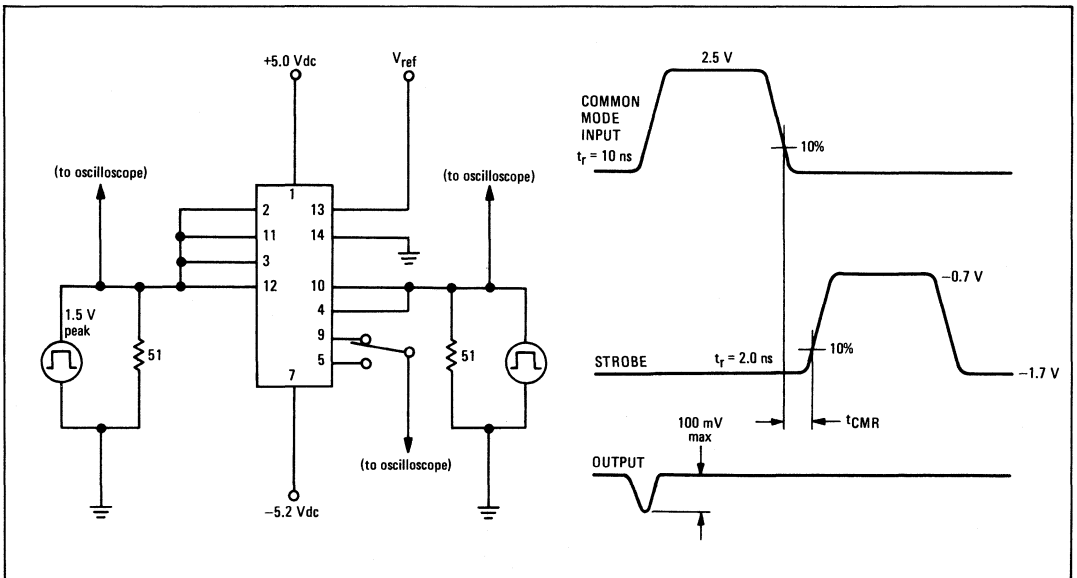


FIGURE 14 – COMMON MODE RECOVERY TIME
COMMON MODE INPUT RANGE
(See definition section)



7

DEFINITIONS

- I_{IO} Input Offset Current – The difference between amplifier input current values $|I_{1A} - I_{2A}|$ or $|I_{1B} - I_{2B}|$.
- I_{SH} Strobe High Current – The amount of input current when the strobe pin is grounded.
- I_{SL} Strobe Low Current – The leakage current when the strobe input is tied to the negative supply.
- P_D Power Dissipation – The amount of power dissipated in the unit.
- t_{CMR} Common Mode Recovery Time – The minimum time by which the strobe input may follow the high level common mode input signal without causing a signal to appear at the amplifier output.
- t_{DR} Differential Mode Recovery Time – Differential recovery time, the minimum time by which the strobe input may follow the high level differential input signal without causing a signal to appear at the amplifier output.
- t_{IO} Propagation Delay, Amplifier Input to Amplifier Output – The time required for the amplifier output to reach 50% of its final value as referenced to 50% of the level of the pulse input (Amplifier input = 25 mVdc or 25% over set threshold).
- t_S Strobe Width – The amount of time the strobe must be high to obtain a given output. Minimum strobe width is that minimum time required to cause the output to complete a full swing V_{OL} to V_{OH} or V_{OH} to V_{OL} .
- t_{SO} Propagation Delay, Strobe Input to Amplifier Output – The time required for the amplifier output pulse to achieve 50% of its final value referenced to 50% of the strobe input pulse at pins 4 or 10.
- t_{SR} Strobe Release Time – The time required for the output to change to 50% of its swing after the strobe reaches 50% of its level going low. A dc level of 50 mV is the input signal.
- V_{CM} Maximum Common Mode Input Range – The common mode input voltage which causes the output voltage level of the amplifier to change by 100 mV (strobe high).
- V_{OH} Output Voltage High – The high-level output voltage at pins 6 and 8 with no input – or at pins 5 and 9 with input above threshold.
- V_{OL} Output Voltage Low – The low-level output voltage at pins 5 and 9 with no input – or at pins 6 and 8 with input above threshold.
- V_{ST} Strobe Threshold Level – The voltage at which the strobe turns the amplifier to the ON state.
- V_{th} Input Threshold – Input pulse amplitude at pins 2, 3, 11, or 12 that causes the output gate to just reach its new value, V_{OL} or V_{OH} .
- V_{thR} Input Threshold Range – The maximum spread of input threshold level that can be attained by varying the threshold voltage reference, V_{ref} .

MC1544L MC1444L

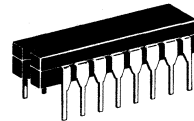
SENSE AMPLIFIERS

IDEAL FOR PLATED-WIRE, THIN-FILM AND OTHER HIGH-SPEED LOW-LEVEL SENSING APPLICATIONS

MC1544L/MC1444L features four input channels with decoded selection, two stages of gain employing capacitive coupling, and a M TTL compatible output gate. AC coupling reduces access times by eliminating the problems usually associated with input line offset voltages.

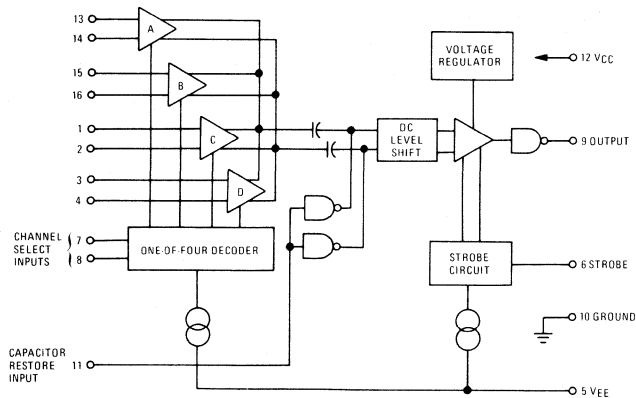
- Threshold Level – 1.0 mV typ
- Propagation Delay Time – 18 ns typ
- Decoded Input Channel Selection
- M TTL Compatible Inputs and Outputs
- Wired OR Output Capability
- DC Level Restore Gate on Capacitors Eliminates Repetition Rate Problems Common to ac-Coupled Circuits
- Output Strobe Capability

**AC-COUPLED
FOUR-CHANNEL
SENSE AMPLIFIER**
**MONOLITHIC SILICON
EPITAXIAL PASSIVATED
INTEGRATED CIRCUIT**



CERAMIC PACKAGE
CASE 620

FIGURE 1 – BLOCK DIAGRAM



TRUTH TABLE

| PIN 7 | PIN 8 | CHANNEL SELECTED |
|-------|-------|------------------|
| HI | HI | A |
| LO | HI | B |
| HI | LO | C |
| LO | LO | D |

MC1544L, MC1444L (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| RATING | SYMBOL | VALUE | UNIT |
|--|-----------------------------|-------------------------|---------------------------|
| Power Supply Voltage | V_{CC} V_{EE} | +7.0 -8.0 | Vdc |
| Common-Mode Input Voltage | V_{CM+} V_{CM-} | +5.0 -6.0 | Vdc |
| Differential-Mode Input Voltage | V_{DM+} V_{DM-} | +5.0 -6.0 | Vdc |
| Capacitor Restore, Channel Select, and Strobe Input Voltage | V_{CR} , V_{CS} , V_S | +5.5 | Vdc |
| Power Dissipation (Package Limitation) Derate above $T_A = +25^\circ\text{C}$ | P_D | 1.0 6.7 | W mW/ $^\circ\text{C}$ |
| Operating Temperature Range | MC1544L MC1444L T_A | -55 to +125 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |
| Junction Temperature | T_J | +175 | $^\circ\text{C}$ |

FIGURE 2 - CIRCUIT SCHEMATIC

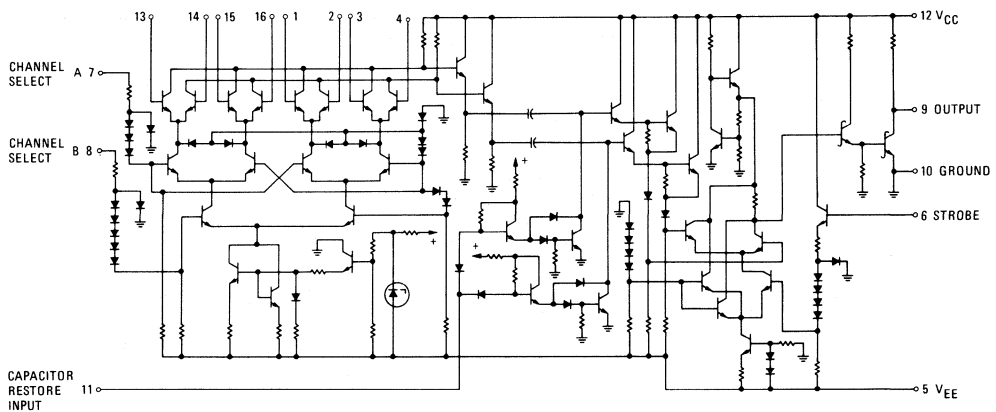


FIGURE 3 - AC TEST CIRCUIT

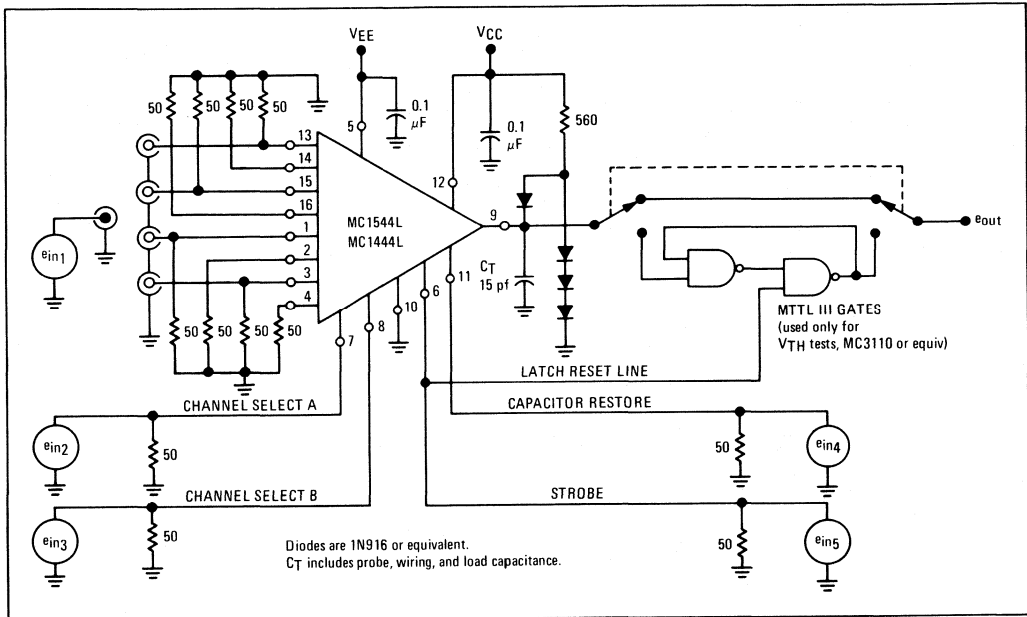


FIGURE 4 - THRESHOLD VOLTAGE TEST

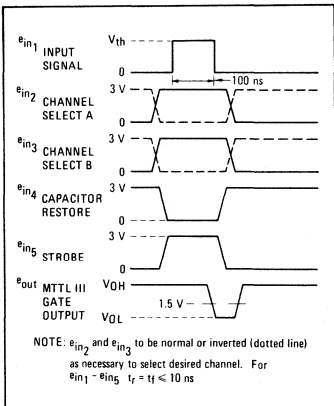


FIGURE 5 - t_{csi} , t_{cri} , t_{si} , t_{pd-} , t_{pd+}

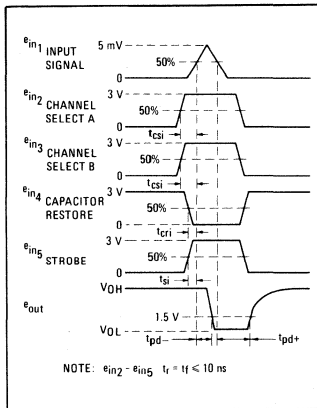


FIGURE 6 - t_{so-} , t_{so+}

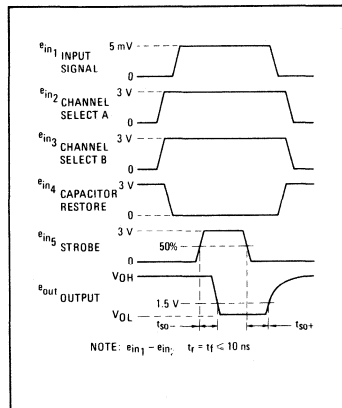


FIGURE 7 — t_{cso+} , t_{cso-}

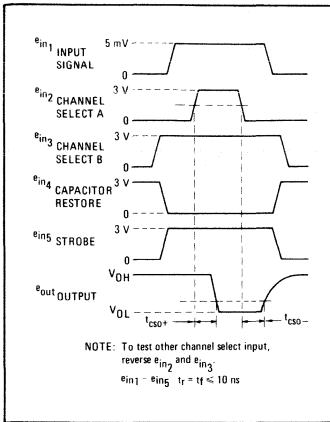
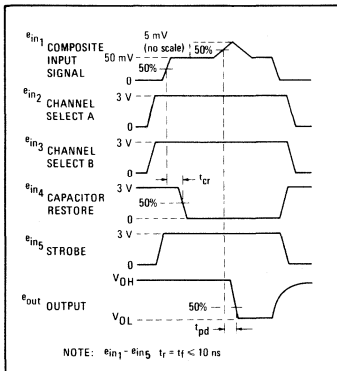


FIGURE 8 — t_{cr}



DEFINITIONS

- I_b Input current to the base of any input transistor when the base of the other transistor of the differential pair is at the same voltage
- I_{CC} Positive power supply current
- I_{CRH} The current into the channel select input when the input is at a high-level of 3.5 volts
- I_{CRL} The current out of the capacitor restore input when the input is at a low-level of 0 volts
- I_{CSH} The input current to a channel select input when that input is at a high-level of 3.5 volts
- I_{CSL} The current into a channel select input when the input is at a low-level of 0 volts
- I_{EE} Negative power supply current
- I_{io} The difference between the base currents of any input differential pair of transistors when the base voltages are equal
- I_{OH} Output logic "1" state source current
- I_{OL} Output logic "0" state sink current
- I_{SH} The current into the strobe input when the input is at a high-level of 3.5 volts
- I_{SL} The current into the strobe input when the input is at a low-level of 0 volts
- $t_{CMR\pm}$ The minimum time between the 50% level of the trailing edge of a + or - 2 volt common-mode signal ($t_r = t_f \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 21
- t_{cr} The minimum time between the 50% level of the leading edge of a 50 mV input offset signal and the 50% level of the leading edge of the capacitor restore pulse as shown in Figure 8
- t_{cri} The minimum time between the 50% level of the leading edge of the capacitor restore signal and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 5
- t_{csi} The minimum time between the 50% level of the leading edge of the channel select and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 5
- t_{cso+} The delay time from the 50% level of the trailing edge of the channel select signal to the 1.5 volt level of the positive edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 7
- t_{cso-} The delay time from the 50% level of the leading edge of the channel select signal to the 1.5 volt level of the negative edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 7
- $t_{DMR\pm}$ The minimum time between the 50% level of the trailing edge of a + or - 1 volt differential-mode signal ($t_r = t_f \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 22
- t_{pd+} The delay time from the 50% level of the trailing edge of a 5 mV input signal to the 1.5 volt level of the positive edge of the output as shown in Figure 5
- t_{pd-} The delay time from the 50% level of the leading edge of a 5 mV input signal to the 1.5 volt level of the negative edge of the output as shown in Figure 5
- t_{si} The minimum time between the 50% level of the leading edge of the strobe and the 50% level of the leading edge of the input signal as shown in Figure 5
- t_{so+} The delay time from the 50% level of the trailing edge of the strobe to the 1.5 volt level of the positive edge of the output when the input is held at the "1" level as shown in Figure 6
- t_{so-} The delay time from the 50% level of the leading edge of the strobe to the 1.5 volt level of the negative edge of the output when the input is held at the "1" level as shown in Figure 6
- V_{CC} Positive power supply voltage
- V_{CCH} Maximum operating positive power supply voltage
- V_{CCL} Minimum operating positive power supply voltage
- V_{CM+} The maximum common-mode input voltage that will not saturate the amplifier
- V_{CM-} The minimum common-mode input voltage that will not break down the amplifier
- V_{CRH} The minimum high-level voltage at the capacitor restore input required to insure that the capacitors are clamped i.e., the input threshold voltage is greater than 10 mV
- V_{CRL} The maximum low-level voltage at the capacitor restore input which will allow normal operation during the threshold test
- V_{CSH} The minimum high-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μ A
- V_{CSL} The maximum low-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μ A
- V_{DM} The maximum differential-mode input voltage that will not saturate the amplifier
- V_{EE} Negative power supply voltage
- V_{EEH} Maximum operating negative power supply voltage
- V_{EEL} Minimum operating negative power supply voltage
- V_{OH} Logic "1" state output voltage
- V_{OL} Logic "0" state output voltage
- V_{SH} The minimum high-level voltage at the strobe input which will allow normal operation during the threshold test
- V_{SL} The maximum low-level voltage at the strobe input which will result in V_{OH} at the output regardless of input signals
- V_{th} The minimum input signal (e_{in1}) required to drive the MTTL III gates to obtain the e_o waveform shown in Figure 4

TYPICAL CHARACTERISTICS
($T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 9 – THRESHOLD VOLTAGE versus TEMPERATURE

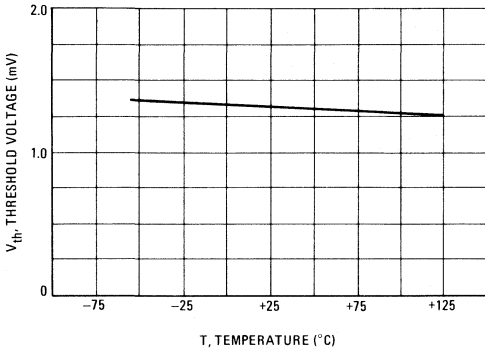


FIGURE 10 – THRESHOLD VOLTAGE versus POWER SUPPLIES

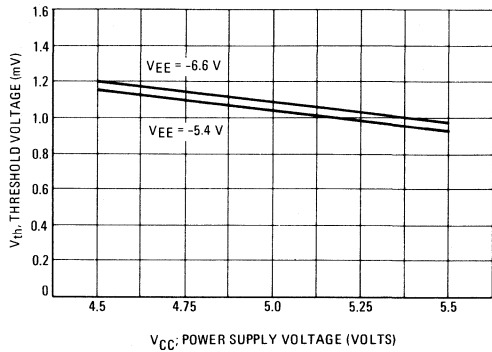


FIGURE 11 – THRESHOLD versus INPUT OFFSET VOLTAGE

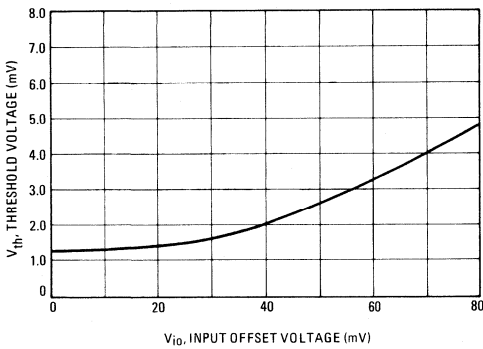


FIGURE 12 – THRESHOLD VOLTAGE versus PULSE WIDTH

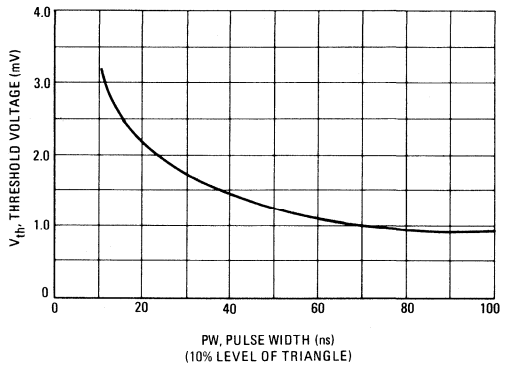


FIGURE 13 – OUTPUT VOLTAGE versus CURRENT and TEMPERATURE

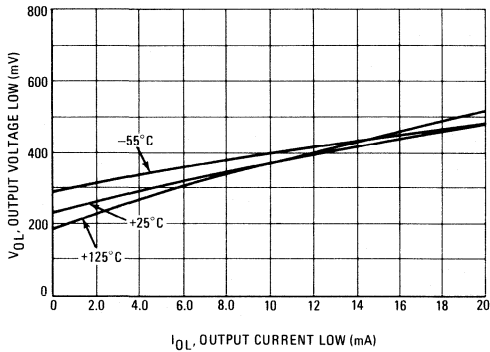
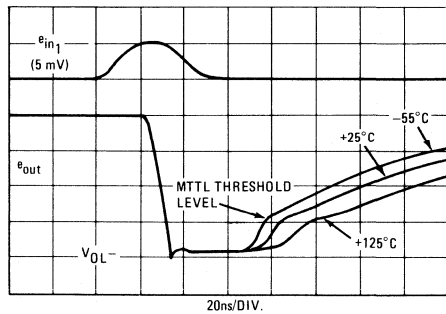


FIGURE 14 – SENSE AMPLIFIER RESPONSE versus TEMPERATURE (See Figures 3 and 5)



TYPICAL CHARACTERISTICS (continued)

FIGURE 15 – INPUT IMPEDANCE versus FREQUENCY

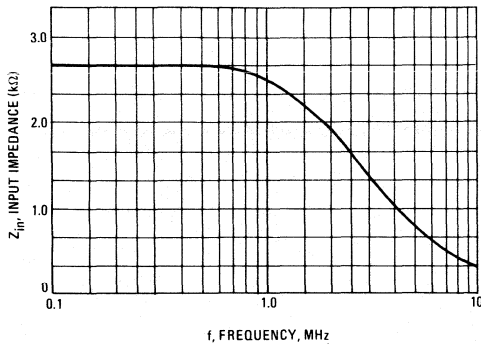


FIGURE 16 – CAPACITOR RESTORE TIME versus INPUT OFFSET VOLTAGE

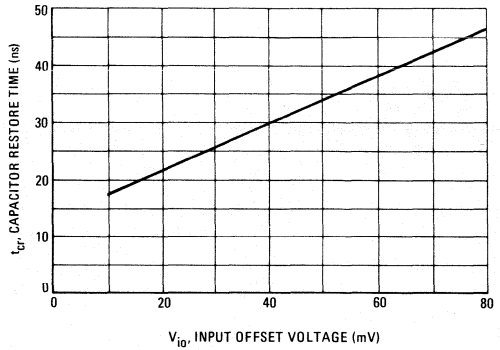


FIGURE 17 – AMPLIFIER INPUT TO OUTPUT TRANSFER CHARACTERISTIC

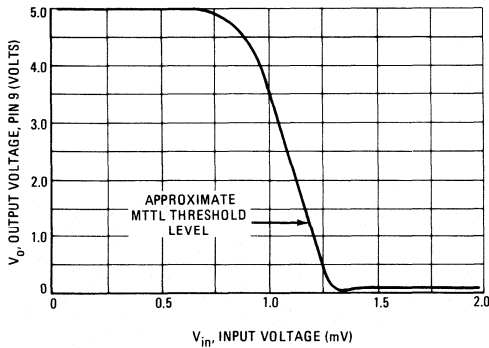


FIGURE 18 – STROBE TO OUTPUT TRANSFER CHARACTERISTICS

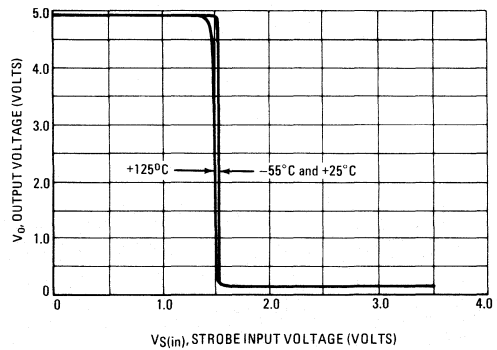


FIGURE 19 – CHANNEL SELECT A to OUTPUT TRANSFER CHARACTERISTICS

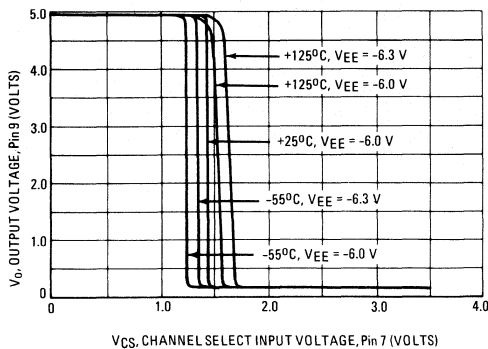


FIGURE 20 – CHANNEL SELECT B to OUTPUT TRANSFER CHARACTERISTICS

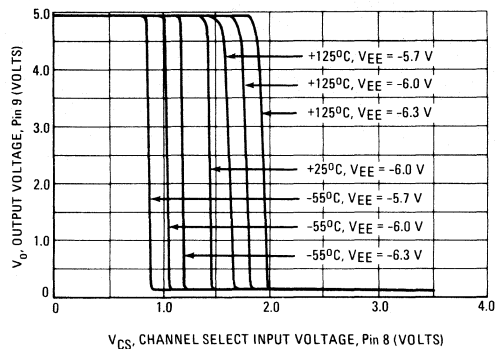


FIGURE 21 – COMMON-MODE CHARACTERISTICS

Note: The 5mV Input Signal (Differential) is superimposed on the Common-Mode Input and is shown separately for reference only.

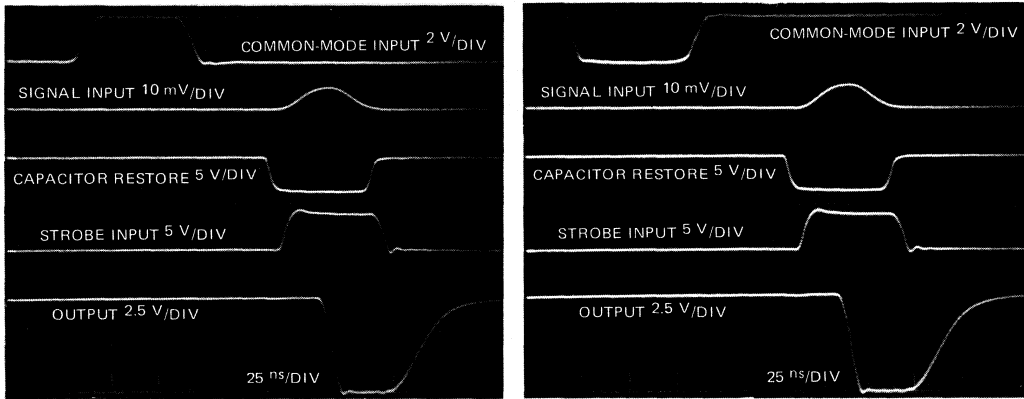
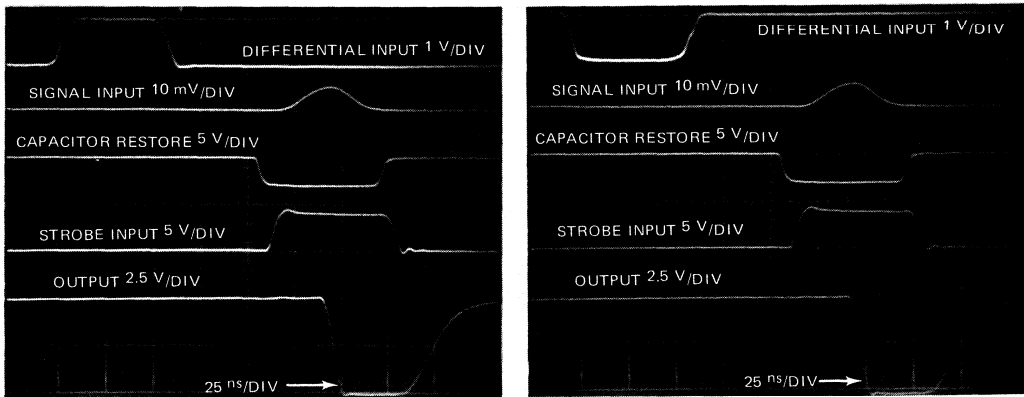


FIGURE 22 – DIFFERENTIAL-MODE CHARACTERISTICS

Note: The 5mV Input Signal is superimposed on the Differential Input and is shown separately for reference only.



7

MC1545 MC1445

HIGH-FREQUENCY CIRCUITS

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

... designed for use as a general-purpose gated wideband-amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN475 and AN491 for design details.

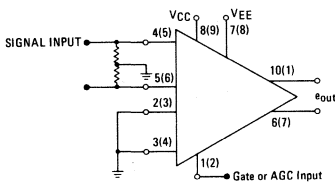
- Large Bandwidth; 75 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

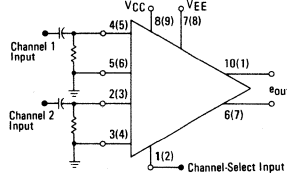
MONOLITHIC SILICON
EPITAXIAL PASSIVATED

TYPICAL APPLICATIONS

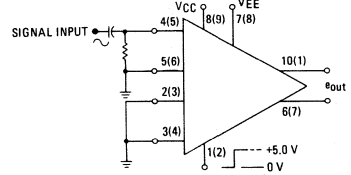
VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC



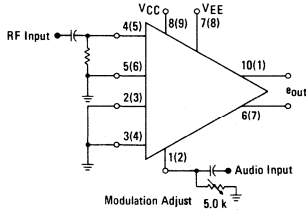
MULTIPLEX OR FSK



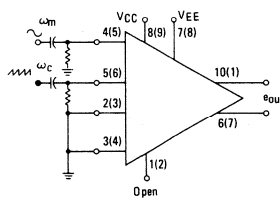
ANALOG SWITCH



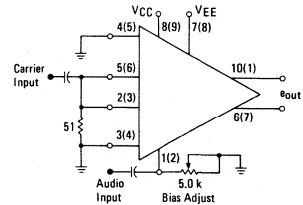
AMPLITUDE MODULATOR



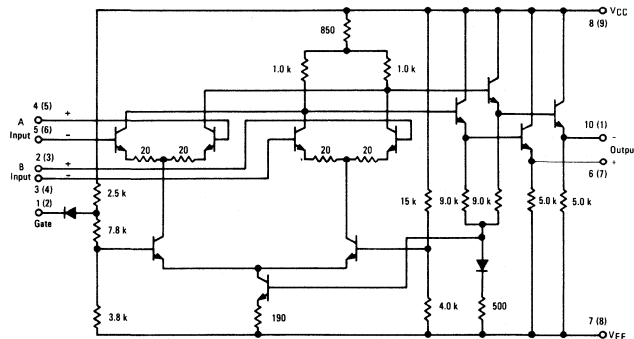
PULSE-WIDTH MODULATOR



BALANCED MODULATOR



CIRCUIT SCHEMATIC

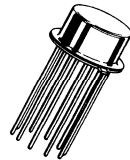


Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

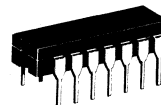
F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86



G SUFFIX
METAL PACKAGE
CASE 602A



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



See Packaging Information Section for outline dimensions.

MC1545, MC1445 (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit | |
|---|-----------------------------|--|-----------------------------|------------------|
| Power Supply Voltage | V_{CC} | +12 | Vdc | |
| | V_{EE} | -12 | Vdc | |
| Differential Input Signal | V_{ID} | ± 5.0 | Volts | |
| Load Current | I_L | 25 | mA | |
| Power Dissipation (Package Limitation) | P_D | 500 | mW | |
| | | Flat Package Derate above $T_A = +25^\circ\text{C}$ | 3.3 mW/ $^\circ\text{C}$ | |
| | | 625 | mW | |
| | | Ceramic Dual In-Line Package Derate above $T_A = +25^\circ\text{C}$ | 5.0 mW/ $^\circ\text{C}$ | |
| | | 680 | mW | |
| Metal Can Derate above $T_A = +25^\circ\text{C}$ | 4.6 mW/ $^\circ\text{C}$ | | | |
| Operating Temperature Range | MC1445 MC1545 | T_A | 0 to +75 -55 to +125 | $^\circ\text{C}$ |
| | | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0$ Vdc, $V_{EE} = 5.0$ Vdc, at $T_A = +25^\circ\text{C}$, specifications apply to both input channels unless otherwise noted)

| Characteristic | Fig. No. | Symbol* | Min | Typ | Max | Unit | | |
|--|------------------|---------|------------------|-----------|-----------|------|--------------------|-----|
| Single-Ended Voltage Gain | MC1445 MC1545 | 1, 12 | A_{vs} | 16 | 19 | 22 | dB | |
| | | | | 16 | 18 | 20 | | |
| Bandwidth | MC1445 MC1545 | 1, 12 | BW | — | 75 | — | MHz | |
| | | | | 50 | 75 | — | | |
| Input Impedance ($f = 50$ kHz) | MC1445 MC1545 | 5, 14 | z_{is} | 3.0 | 10 | — | k ohms | |
| | | | | 4.0 | 10 | — | | |
| Output Impedance ($f = 50$ kHz) | | 6, 15 | z_{os} | — | 25 | — | Ohms | |
| Output Voltage Swing ($R_L = 1.0$ k ohm, $f = 50$ kHz) | | 4, 13 | V_{OD} | 1.5 | 2.5 | — | V_{p-p} | |
| Input Bias Current ($I_{IB} = (I_1 + I_2)/2$) | MC1445 MC1545 | 16 | I_{IB} | — | 15 | 30 | $\mu\text{A dc}$ | |
| | | | | — | 15 | 25 | | |
| Input Offset Current | | 16 | $ I_{IO} $ | — | 2.0 | — | $\mu\text{A dc}$ | |
| Input Offset Voltage | MC1445 MC1545 | 17 | $ V_{IO} $ | — | — | 7.5 | mVdc | |
| | | | | — | 1.0 | 5.0 | | |
| Quiescent Output dc Level | | 17 | V_O | — | 0.2 | — | Vdc | |
| Output dc Level Change (Gate Voltage Change: +5.0 V to 0 V) | | 17 | $ \Delta V_O $ | — | 15 | — | mV | |
| Common-Mode Rejection Ratio ($f = 50$ kHz) | | 9, 18 | CMRR | — | 85 | — | dB | |
| Input Common-Mode Voltage Swing | | 18 | V_{ICR} | — | ± 2.5 | — | V_p | |
| Gate Characteristics | MC1445 MC1545 | 8 | V_{GOL} | 0.20 | 0.40 | — | Vdc | |
| | | | | 0.45 | 0.70 | — | | |
| | | | | V_{GOH} | — | 1.3 | | 3.0 |
| | | | | | — | 1.5 | | 2.2 |
| Gate Current Low (Gate Voltage = 0 V) | MC1445 MC1545 | 18 | I_{GOL} | — | — | 4.0 | mA | |
| Gate Current High (Gate Voltage = +5.0 V) | MC1445 MC1545 | 18 | I_{GOH} | — | — | 4.0 | μA | |
| | | | | — | — | 2.0 | | |
| Step Response ($e_{in} = 20$ mV) | MC1445 MC1545 | 19 | t _{PLH} | — | 6.5 | — | ns | |
| | | | | — | 6.5 | 10 | | |
| | | | t _{PHL} | — | 6.3 | — | | |
| | | | | — | 6.3 | 10 | | |
| | | | t _r | — | 6.5 | — | | |
| | | | | — | 6.5 | 10 | | |
| | | | t _f | — | 7.0 | — | | |
| — | 7.0 | 10 | | | | | | |
| Wideband Input Noise (5.0 Hz - 10 MHz, $R_S = 50$ ohms) | | 10, 20 | $V_{N(in)}$ | — | 25 | — | $\mu\text{V(rms)}$ | |
| DC Power Dissipation | MC1445 MC1545 | 11, 20 | P_D | — | 70 | 150 | mW | |
| | | | | — | 70 | 110 | | |

Note 1 V_{GOL} is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
 Note 2 V_{GOH} is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.
 *Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

MC1545, MC1445 (continued)

FIGURE 1 – SINGLE-ENDED VOLTAGE GAIN versus FREQUENCY

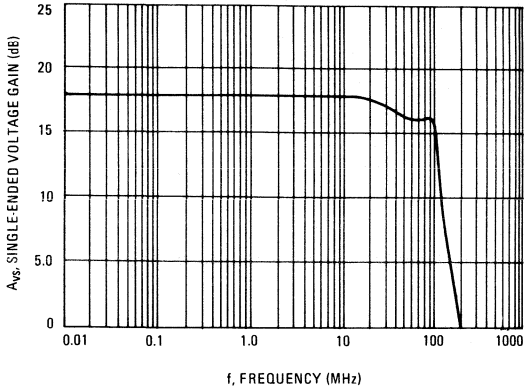


FIGURE 2 – SINGLE-ENDED VOLTAGE GAIN versus TEMPERATURE

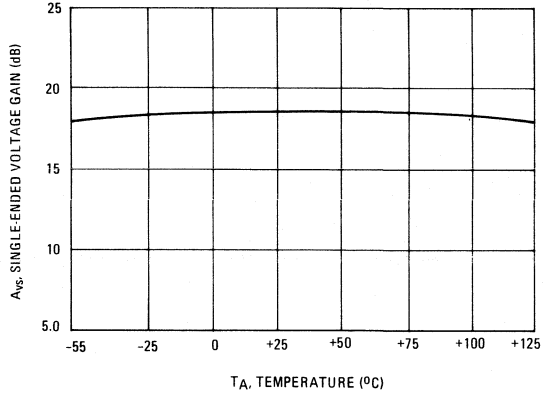


FIGURE 3 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGES

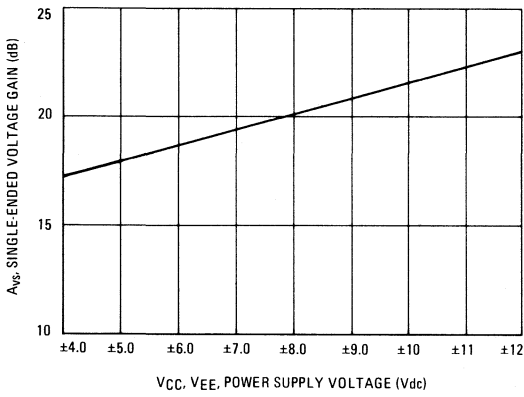


FIGURE 4 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

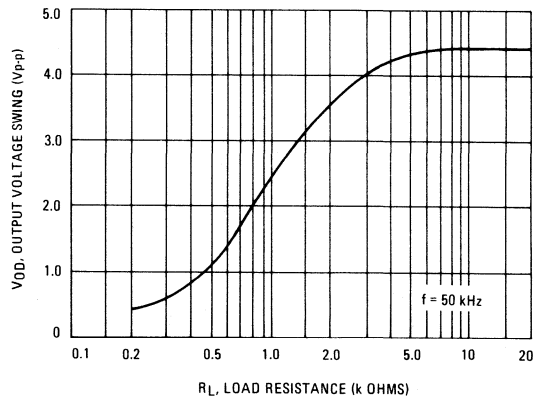


FIGURE 5 – INPUT C_p AND R_p versus FREQUENCY (BOTH CHANNELS)

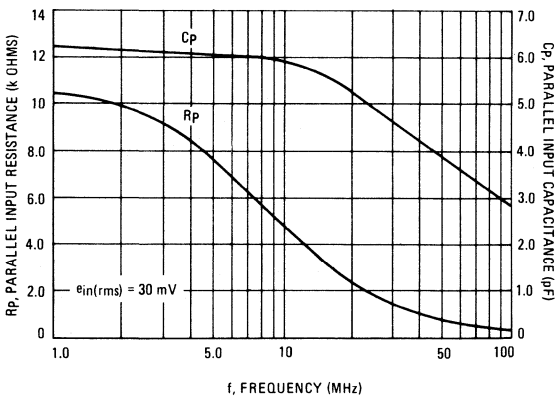
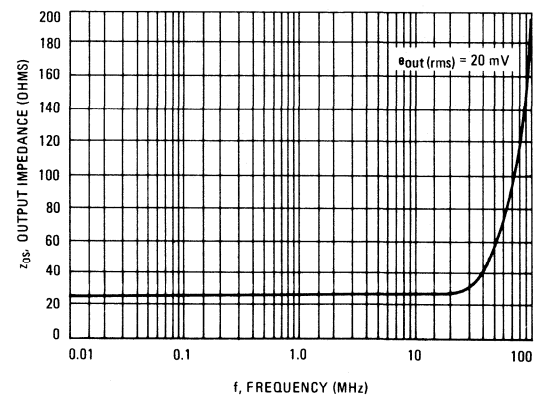


FIGURE 6 – OUTPUT IMPEDANCE versus FREQUENCY



MC1545, MC1445 (continued)

FIGURE 7 – CHANNEL SEPARATION versus FREQUENCY

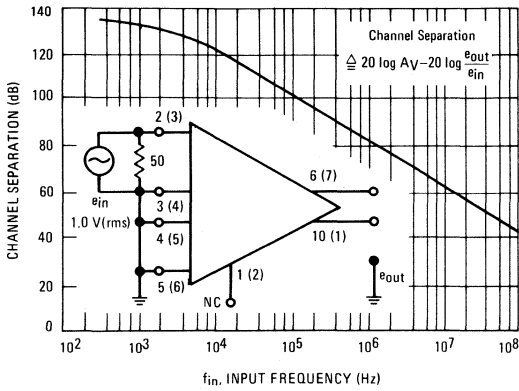


FIGURE 9 – COMMON MODE REJECTION RATIO versus FREQUENCY

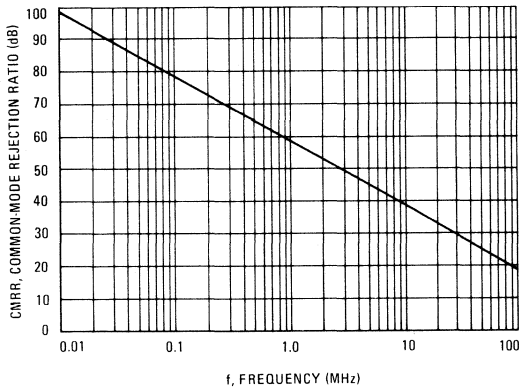
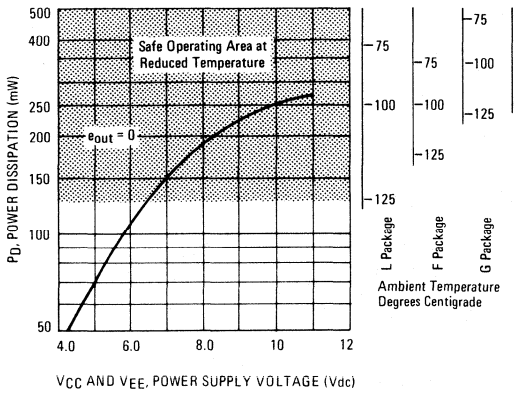


FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

FIGURE 8 – GATE CHARACTERISTICS

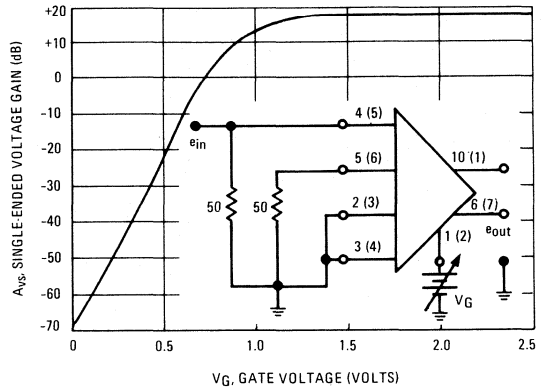


FIGURE 10 – INPUT WIDEBAND NOISE versus SOURCE RESISTANCE

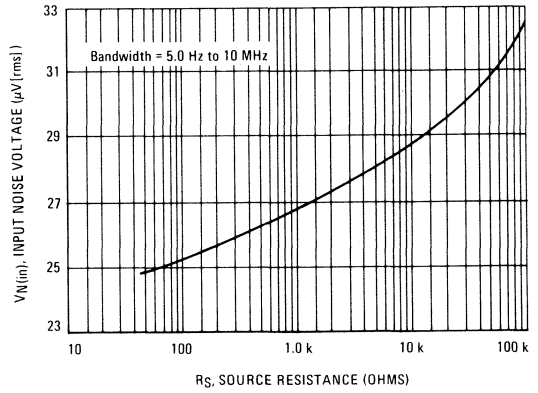
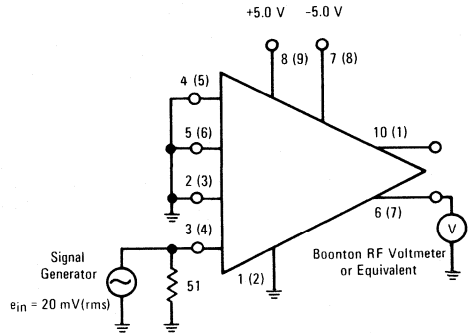


FIGURE 12 – SINGLE-ENDED VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT



MC1545, MC1445 (continued)

FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

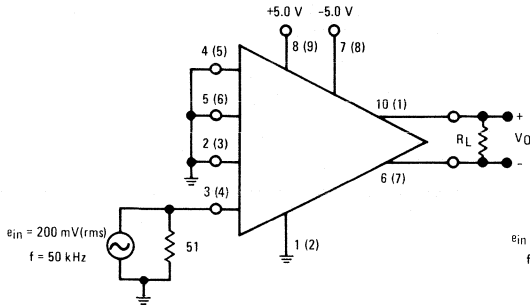


FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

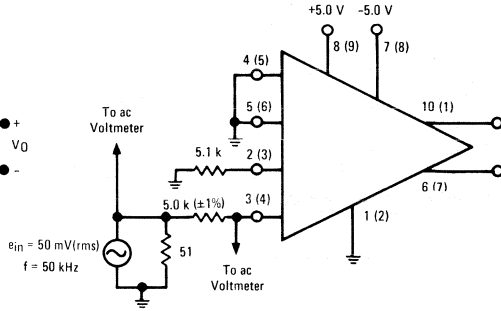


FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

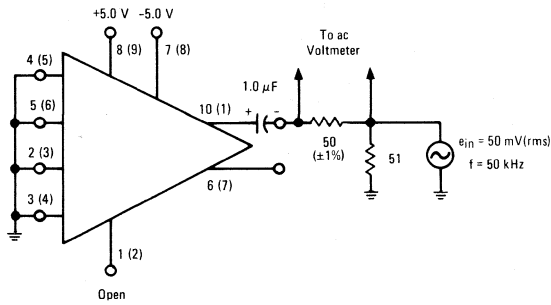


FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT

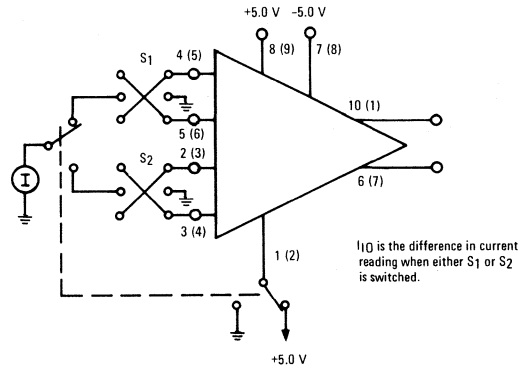


FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT

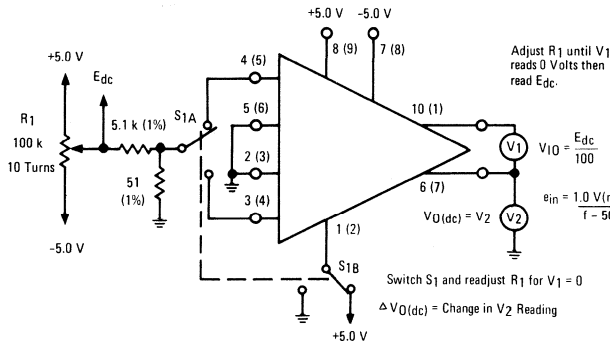
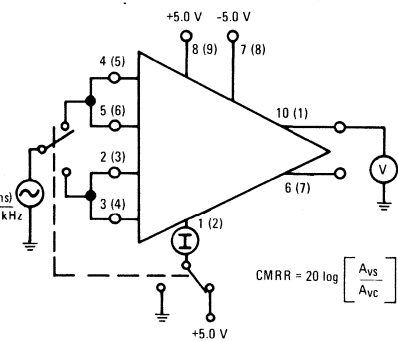
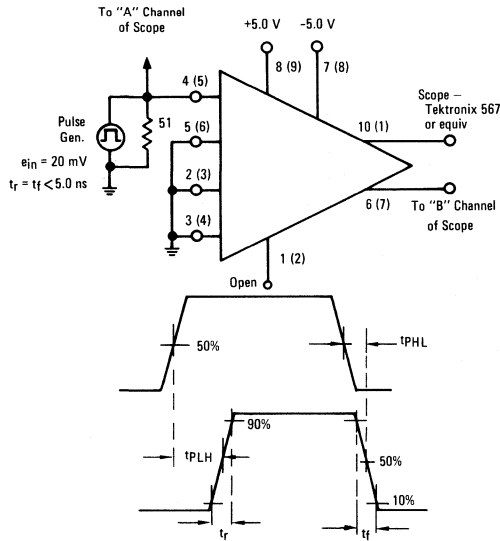


FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

FIGURE 19 – PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages,
number at left in each case denotes corresponding pin for G package.

FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT

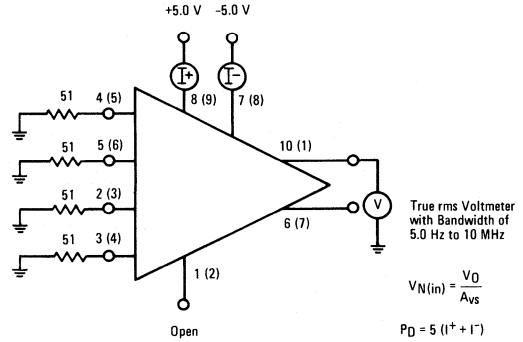
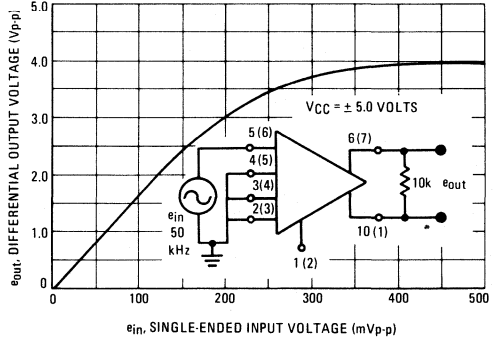


FIGURE 21 – LIMITING CHARACTERISTIC



**MC1546L
MC1446L**

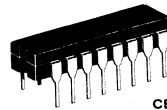
FOUR-CHANNEL PLATED-WIRE SENSE AMPLIFIER

... a sense amplifier designed to convert positive or negative 3.0 mV signals from plated-wire memories to transistor-transistor logic levels (MTTL). The problems encountered with ac-coupled plated-wire sense amplifiers are eliminated with this direct-coupled sense amplifier.

- Positive or Negative 3.0 mV Signal to Any of Four Input Channels Produces a Logic 1 or 0 Output (MC1446 – Positive or Negative 4.0 mV).
- Low Input Offset Voltages Apply to All Four Channels – 0.5 mV typ
- Wired "OR" Capability at Amplifier Output Results in Fewer Associated Circuits
- 2 by 4 Internal Decoder Simplifies Channel Selection
- Fast Recovery Time from Overload Signals – 40 ns typ
- Good Isolation Between ON and OFF Channels
- Channel Select and Strobe Operate from Standard MTTL Levels

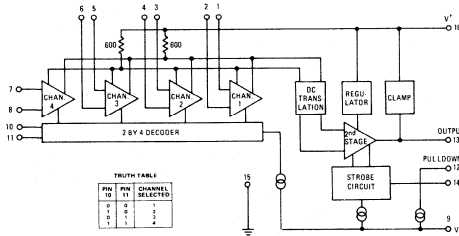
FOUR-CHANNEL PLATED-WIRE SENSE AMPLIFIER

**MONOLITHIC SILICON
EPITAXIAL PASSIVATED
INTEGRATED CIRCUIT**

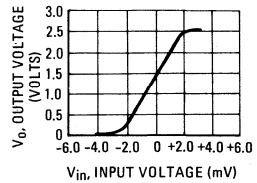


CERAMIC PACKAGE
CASE 620

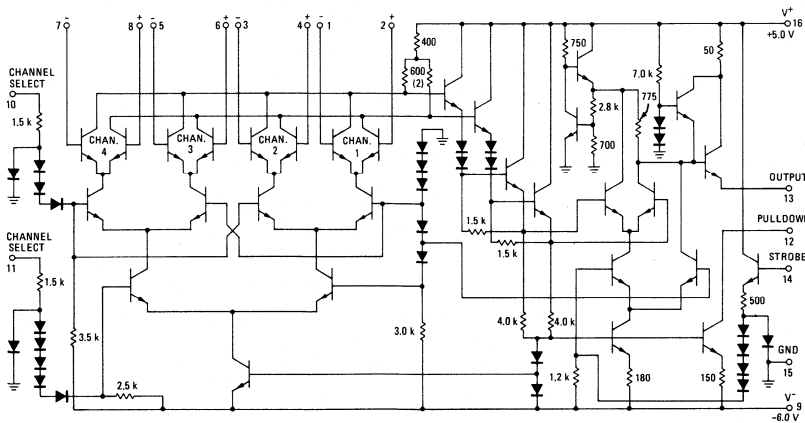
BLOCK DIAGRAM



TRANSFER CHARACTERISTICS



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MC1546L, MC1446L (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|--------------------|------------------|----------------------------|
| Power Supply Voltage | V ⁺ | +10 | Vdc |
| | V ⁻ | -10 | |
| Differential Input Signal | V _{in} | ±5.0 | Volts |
| Common-Mode Input | CMV _{in} | ±5.0 | Volts |
| Output Current | I _{out} | 25 | mA |
| Power Dissipation (Package Limitation) Ceramic Package Derate above T _A = +25°C | P _D | 575 3.85 | mW mW/°C |
| Operating Temperature Range | MC1546L | T _A | -55 to +125 |
| | MC1446L | | 0 to +75 |
| Storage Temperature Range | MC1546L MC1446L | T _{stg} | -65 to +175 -55 to +125 |

ELECTRICAL CHARACTERISTICS

(V⁺ = +5.0 Vdc ±1%, V⁻ = -6.0 Vdc ±1%, T_A = +25°C unless otherwise noted)

| Characteristic | Fig. | Symbol | MC1546L | | | MC1446L | | | Unit |
|--|------|------------------------------------|---------|------|------|---------|------|-----|-------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Voltage Gain | 1 | A _V | - | 600 | - | - | 600 | - | - |
| Output Voltage Level | 2 | V _o | 0.8 | 1.4 | 2.0 | 0.4 | 1.4 | 2.4 | Vdc |
| T _A = T _{low} * to T _{high} * e _{in} = 0, 0 e _{in} = +3.0, +4.0 mV e _{in} = -3.0, -4.0 mV | | | 2.0 | - | - | 2.0 | - | - | |
| | | | - | - | 0.4 | - | 0.4 | - | |
| Input Bias Current | 3 | I _b | - | 15 | 40 | - | 15 | 60 | μA |
| Input Offset Current | 3 | I _{io} | - | 0.1 | 2.0 | - | 0.1 | 4.0 | μA |
| Channel Select Current | 4 | I _{CH} I _{CL} | - | 1.7 | 2.4 | - | 1.7 | 2.6 | mA |
| | | | - | 0.5 | 0.9 | - | 0.5 | 1.0 | |
| Channel Select Voltage | 5 | V _{CH} V _{CL} | 2.0 | - | - | 2.0 | - | - | Volts |
| | | | - | - | 0.8 | - | - | 0.8 | |
| Strobe Voltage | 5 | V _{SH} V _{SL} | 2.0 | - | - | 2.0 | - | - | Volts |
| | | | - | - | 0.8 | - | - | 0.8 | |
| Strobe Input Current | 4 | I _S | - | 30 | 100 | - | 30 | 150 | μA |
| Output Source Current | 6 | I _{o+} | 5.0 | 8.0 | - | 4.0 | 8.0 | - | mA |
| Output Sink Current | 6 | I _{o-} | -3.0 | -4.0 | - | -2.5 | -4.0 | - | mA |
| Positive Supply Current | 6 | I ⁺ | - | 19 | 25 | - | 19 | 27 | mA |
| Negative Supply Current | 6 | I ⁻ | - | -17 | -22 | - | -17 | -24 | mA |
| Input Common-Mode Voltage Range | 7 | CMV _(in) | - | +2.7 | - | - | +2.7 | - | Volts |
| | | | - | -1.0 | - | - | -1.0 | - | |
| | | | - | +2.7 | - | - | +2.7 | - | |
| Channels Not Selected | - | -6.0 | - | - | -6.0 | - | - | | |
| Input Differential-Mode Voltage Range | 7 | DMV _(in) | - | ±0.5 | - | - | ±0.5 | - | Volts |
| | | | - | ±2.0 | - | - | ±2.0 | - | |
| | | | - | - | - | - | - | - | |

* T_{low} = -55°C for MC1546, 0°C for MC1446; T_{high} = +125°C for MC1546, +75°C for MC1446

SWITCHING CHARACTERISTICS

| | | | | | | | | | |
|--|----|----------------------------------|----|----|----|---|----|---|----|
| Propagation Delay Time | 8 | t _{pd} | 10 | 14 | 18 | - | 14 | - | ns |
| Output Rise or Fall Time | 8 | t _r or t _f | - | 30 | - | - | 30 | - | ns |
| Strobe Delay Time | 9 | t _{dS} | - | 14 | 18 | - | 14 | - | ns |
| Strobe Width (min) | 9 | t _{S(min)} | - | 20 | - | - | 20 | - | ns |
| Channel Select Time | 10 | t _{Csel} | - | 14 | 18 | - | 14 | - | ns |
| Common-Mode Recovery Time (channel selected) | 7 | t _{CMR} | - | 60 | - | - | 60 | - | ns |
| Differential-Mode Recovery Time (channel selected) | 8 | t _{DMR} | - | 40 | - | - | 40 | - | ns |

TEST CIRCUITS

FIGURE 1 – VOLTAGE GAIN

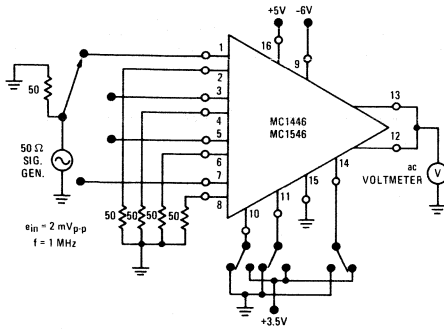
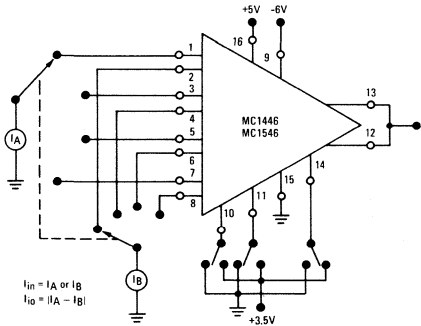


FIGURE 3 – INPUT CURRENTS



$I_{in} = I_A \text{ or } I_B$
 $I_{io} = |I_A - I_B|$

FIGURE 5 – CHANNEL SELECT TRANSFER CHARACTERISTICS

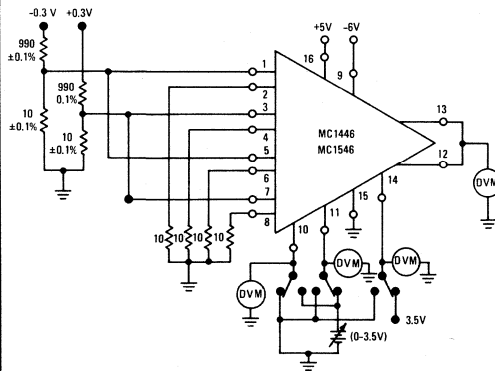


FIGURE 2 – OUTPUT DC LEVELS

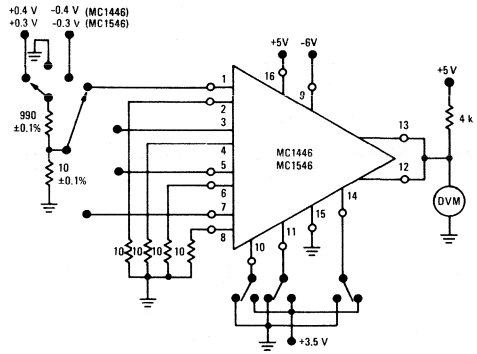


FIGURE 4 – CHANNEL SELECT AND STROBE INPUT CURRENTS

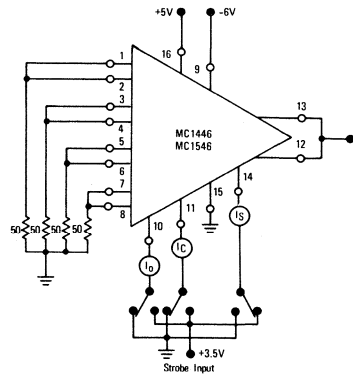
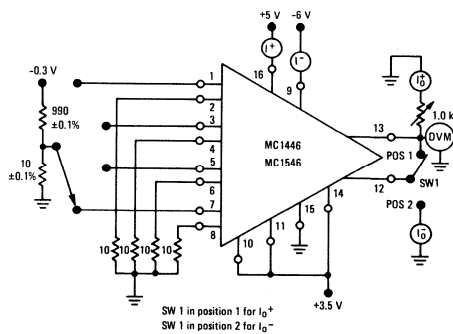


FIGURE 6 – OUTPUT CURRENTS



SW 1 in position 1 for I_{o+}
 SW 1 in position 2 for I_{o-}

FIGURE 7 – INPUT COMMON-MODE CHARACTERISTICS

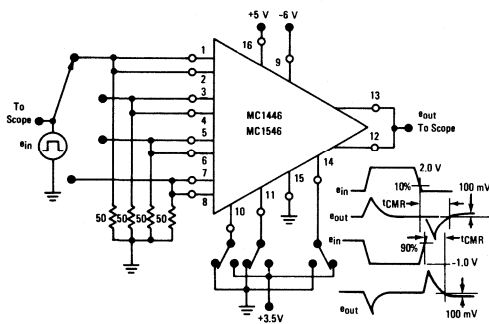


FIGURE 8 – CIRCUIT PROPAGATION DELAY, OUTPUT RISE AND FALL TIMES, AND DIFFERENTIAL-MODE RECOVERY TIME

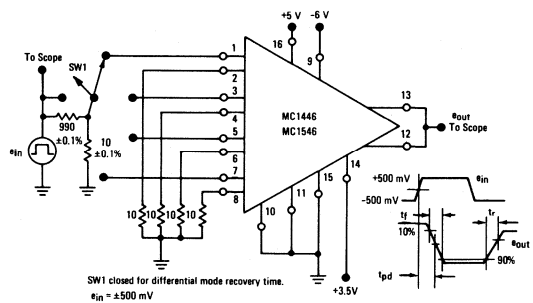


FIGURE 9 – STROBE CHARACTERISTICS

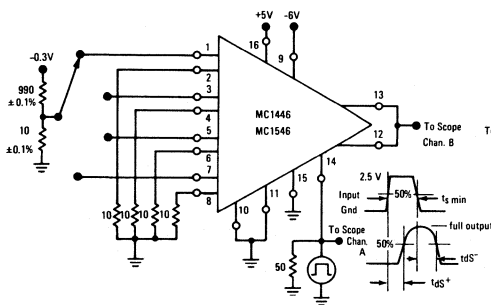
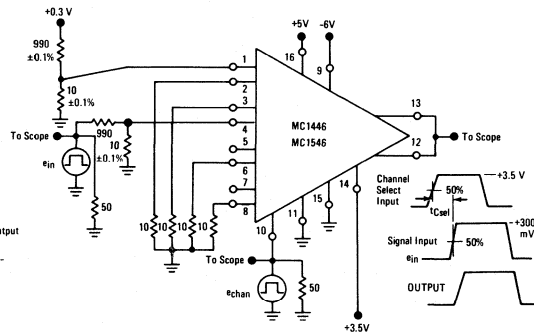


FIGURE 10 – CHANNEL SELECT TIME



7

TYPICAL RECOVERY TIME WAVEFORMS

FIGURE 11 – COMMON-MODE RECOVERY TIME

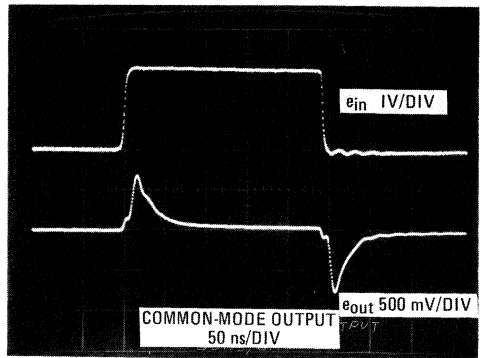
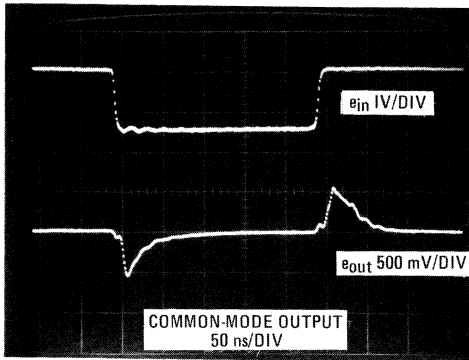
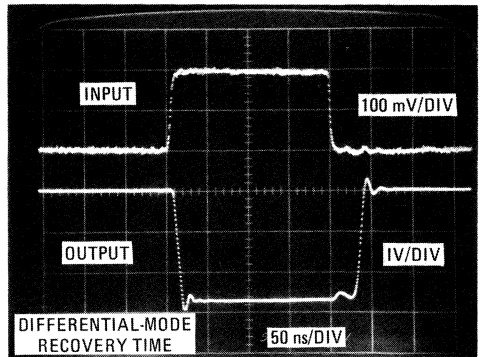
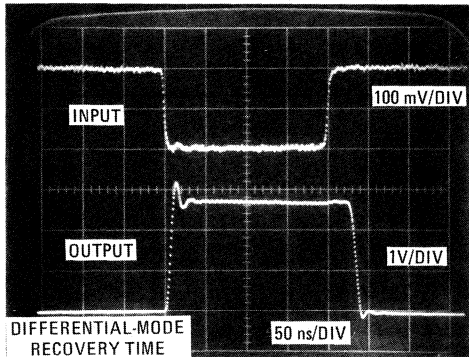


FIGURE 12 – DIFFERENTIAL-MODE RECOVERY TIME



TYPICAL CHARACTERISTICS
($T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 13 – VOLTAGE GAIN versus TEMPERATURE

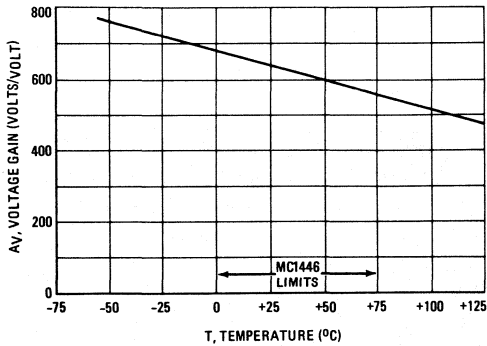


FIGURE 14 – DC OUTPUT VOLTAGE LEVEL versus TEMPERATURE (All Inputs Grounded)

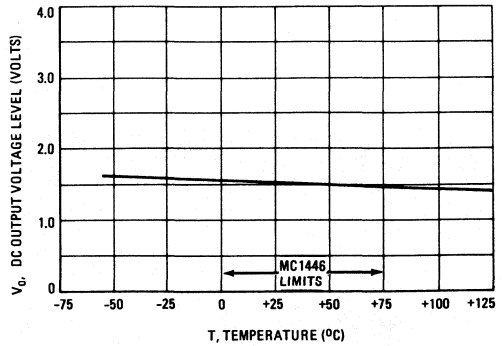


FIGURE 15 – AMPLIFIER TRANSFER CHARACTERISTICS

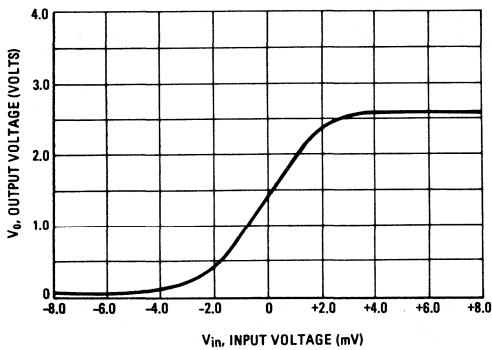


FIGURE 16 – CHANNEL SELECT versus OUTPUT TRANSFER CHARACTERISTICS

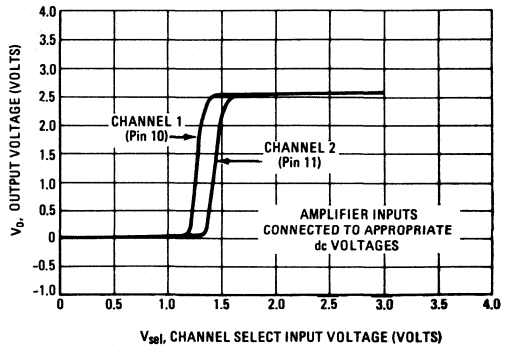


FIGURE 17 – STROBE INPUT TRANSFER CHARACTERISTICS (Input High)

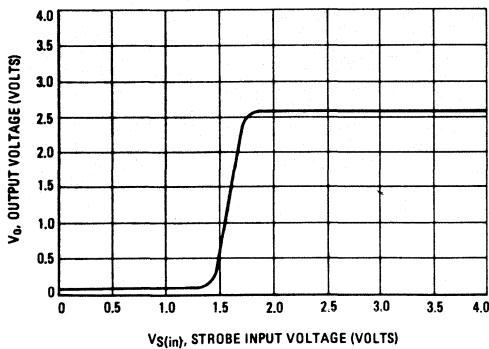
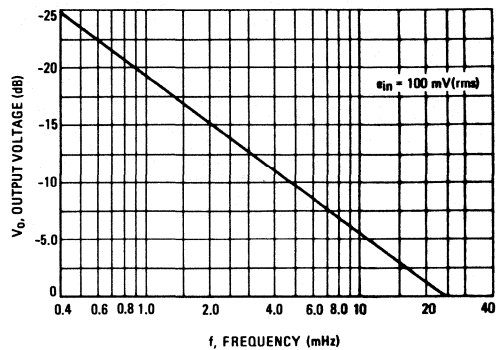


FIGURE 18 – COMMON-MODE GAIN versus FREQUENCY



7

TYPICAL CHARACTERISTICS (continued)

FIGURE 19 – VOLTAGE GAIN versus FREQUENCY

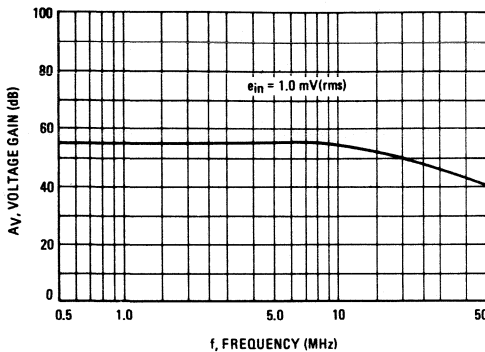
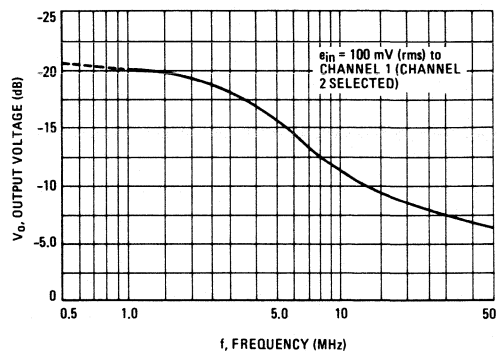


FIGURE 20 – ADJACENT CHANNEL ISOLATION versus FREQUENCY



CIRCUIT DESCRIPTION OF THE MC1546L/MC1446L

The MC1546L/MC1446L was designed to translate a positive 3.0 mV signal from a plated wire memory to an MTTL "1" level, or a negative 3.0 mV to an MTTL "0" level. This sense amplifier also eliminates the requirement for a bipolar switch in series with the plated wire because the bit selection is done inside the sense amplifier.

The circuit operation can be described in sections as follows:

1. All channels have been designed for low input offsets – 0.5 V typical.
2. Channel "ORing" is accomplished by using common collector load resistors for four differential amplifier pairs.
3. Channel selection is accomplished by current steering through the four differential pairs. The circuit below the four differential pairs forms a matrix tree which can be thought of as a 2-by-4 decode matrix. The bottom transistor is the current source for the first stage of gain.
4. DC translation between the first and second stages of gain is done through an emitter-follower stage, two diodes and another emitter follower for each side of the differential amplifier. The currents in these translator legs are combined and run through diodes to the negative supply. These diodes are used to bias both the first and second gain stages. This also gives the appropriate gain versus temperature and dc output level versus temperature characteristics.
5. The top of the second stage amplifier is regulated at a voltage equal to five diode drops above ground. It can be seen that if the 700 ohm resistor in the regulator has one diode (or V_{BE}) across it then the 2.8 k ohm resistor will have four diode drops across it. This makes a five diode drop voltage

above ground that is fairly independent of the positive supply.

6. The current in the second stage of the amplifier is set by the 180-ohm resistor in the emitter of the current source. It can be seen that this resistor has one diode drop (approximately 750 mV) across it. Therefore, an analysis will show that the voltage drop across the 775-ohm load resistor in the second stage will be approximately two diodes when the differential amplifier is balanced. Accounting for the additional diode voltage drop of the emitter-follower output transistor will set the output dc level at two diodes above ground or very near the center of MTTL threshold.
7. The strobe circuit works by steering current in the second stage. When the strobe is low, the entire current of the second stage current source is steered through the 775-ohm load resistor. This clamps the output to a low state so that an input signal cannot cause an output. When the strobe is high, the current is steered through the second stage differential amplifier pair and the output will go to a level dictated by the presence of an input signal.
8. The output circuit of the sense amplifier may be thought of as a push-pull type. The emitter of the push transistor is brought out to a separate pin from the collector of the pull transistor. This will facilitate "Wire ORing" the outputs of several sense amplifiers. Several emitter outputs can be wired together along with only one collector/pull-down transistor. The unused collectors of the pull-down transistor must be grounded. An example of the use of "Wire ORing" is to have four MC1546 devices wired-OR into a 16-channel sense amplifier in which a channel may be selected by selecting channels in parallel at the amplifier inputs and strobing the proper sense amplifier.

APPLICATIONS INFORMATION

The MC1546/MC1446 devices are designed to convert signals from plated-wire memories as small as positive or negative 3 mV to MTTL logic levels. The output level of the sense amplifier with no input signal present and with the strobe high is typically 1.4 volts (typical input threshold of MTTL logic). Hence, if the strobe goes high during the absence of an input signal from the plated-wire memory, the sense amplifier output will rise to 1.4 volts. This condition could cause false outputs; therefore careful considerations must be given to strobe timing. Figure 21 illustrates a typical timing sequence of the MC1546/MC1446 device as recommended for proper operation.

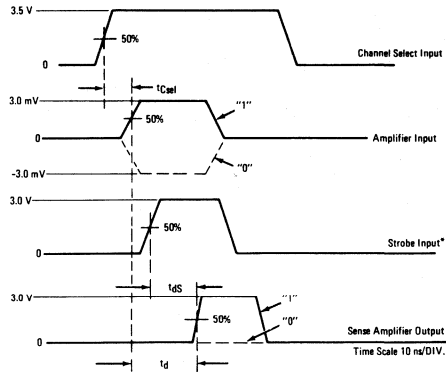
Figure 22 shows how these sense amplifiers are used in an N-word-line-by-32-bit basic memory plane organized as 4-N words of 8 bits each. During a read cycle, the read current is pulsed through a selected word-line and thus generates outputs to all of the 32-bit positions in the line. The internal one-of-four decoder selects the desired channels of the eight sense amplifiers for a particular system word. When the strobe goes high, the sense amplifier outputs switch according to the data present at the amplifier inputs. The data readout on the other 24-bit lines is not lost due to the Non-Destructive Read-Out properties of a plated-wire memory. On the next read cycle the decoder of the sense amplifier in combination with the selected word-line determines the 8-bits of data to read.

APPLICATIONS INFORMATION (continued)

Memory organizations that have more than four words per word-line require that the sense amplifier outputs be wired-OR. To wire-OR the outputs of several sense amplifiers all of the emitters of the output-pullup transistors are tied together. Only one collector of the pulldown transistors is tied to the wired-OR emitters of the pullup transistors. The remaining pulldown transistors must be grounded as noted in Figure 23. Ten or more sense amplifiers may be wired-OR together without any reduction in usable logic levels since only one sense amplifier per bit is on at any given time. Variations in propagation delay time (t_{pd}), versus the number of wired-OR sense amplifiers and the output capacitance are given in Figure 24.

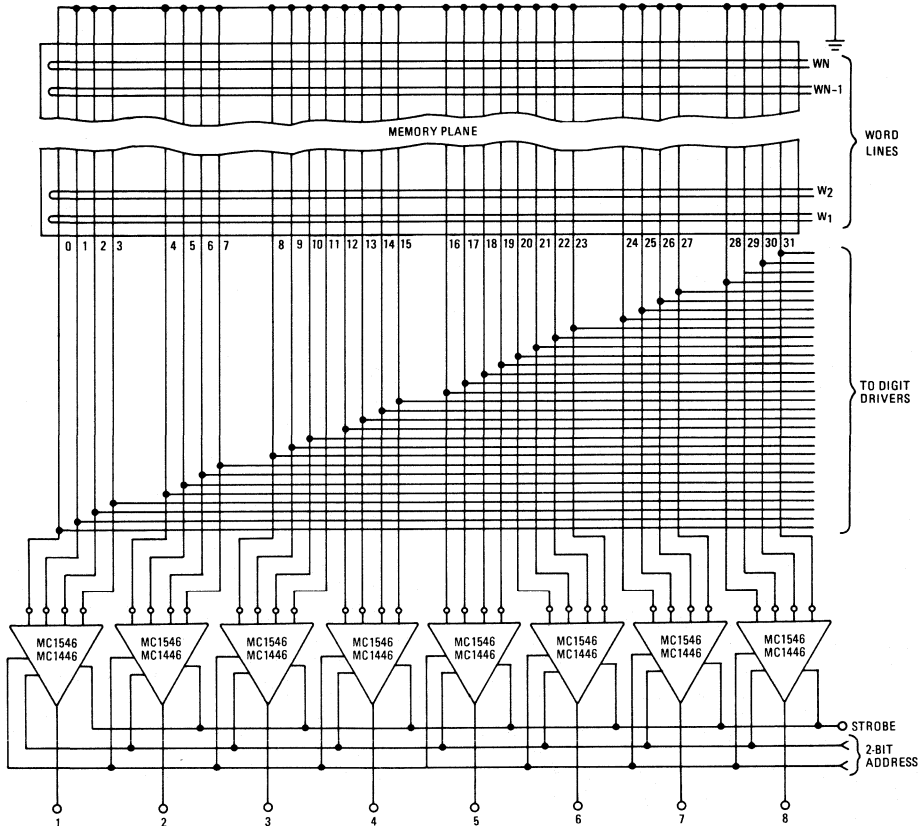
In Figure 25, eight are required for each bit of a 32-word/word-line memory. For those sense amplifiers that have wired-OR outputs, the strobe is used for decoding by attaching each strobe to a 3-bit binary-to-1-of-8-bit decoder (MC4006). Thus only one sense amplifier per bit can be strobed at a given time. High fan-out gates are required on the channel select lines since a high current must be supplied to the select lines to drive them to the logic "1" level. The strobe current is low, thereby allowing many strobe lines to be driven with only one gate.

FIGURE 21 – TYPICAL TIMING SEQUENCE OF THE MC1546/MC1446



*The strobe pulse width is smaller than the amplifier input pulse width.

FIGURE 22 – N-WORD-LINE-BY-32-BIT MEMORY PLANE ORGANIZED AS 4-N WORDS OF 8 BITS EACH



APPLICATIONS INFORMATION (continued)

FIGURE 23 – WIRED "OR" MC1546/MC1446 DEVICES

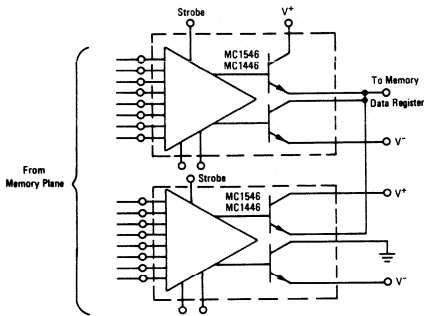


FIGURE 24 – TYPICAL PROPAGATION DELAY TIME VARIATION (per number of devices at stated capacitance)

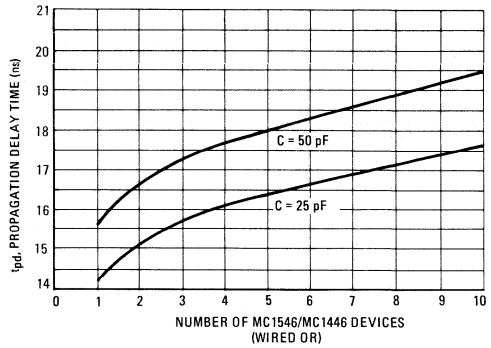
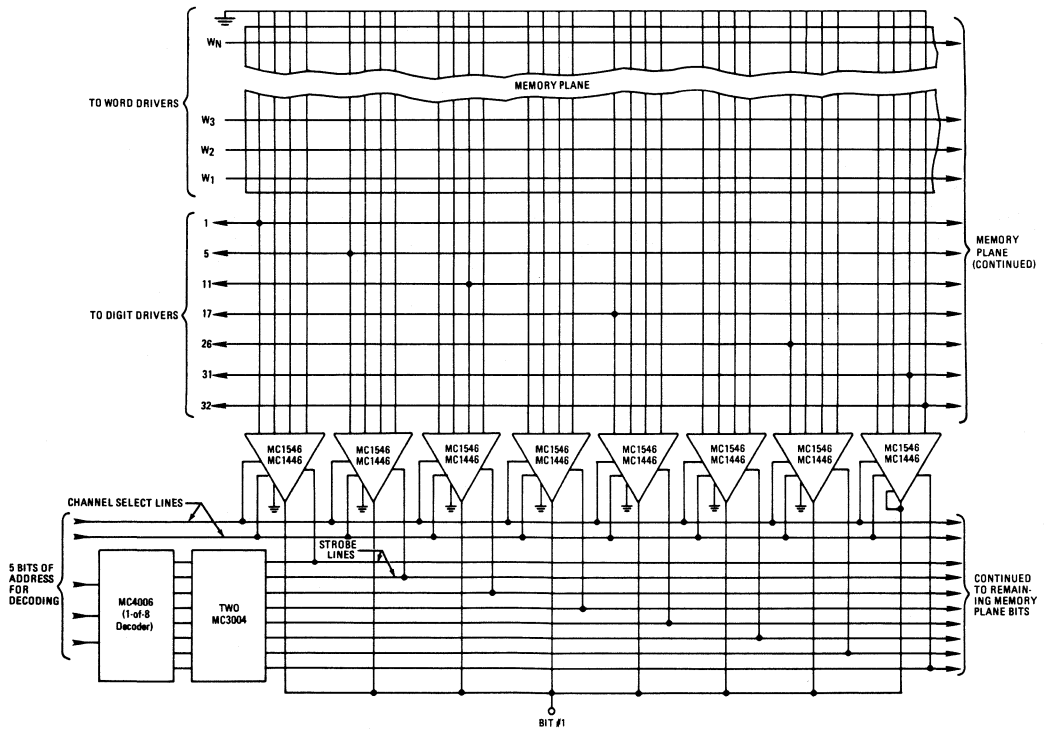


FIGURE 25 – 32 WORDS/WORD - LINE ORGANIZED MEMORY



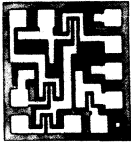
DEFINITIONS

| | | |
|---|---|--|
| <p>A_V the voltage gain from a channel input to amplifier output (input signal is 2 mV peak-to-peak and the strobe is high)</p> <p>CMV_{in} maximum input common-mode voltage on any channel that will not cause the amplifier to saturate</p> <p>DMV_{in} maximum input differential-mode voltage on any channel signal that will not saturate the amplifier</p> <p>I^+ current from the positive supply with no load (pin 12 shorted to pin 13)</p> <p>I^- current into the negative supply with both channel select pins at +3.5 volts</p> <p>I_b input current into the base of any input transistor when the opposite transistor of the differential pair is at the same voltage</p> <p>I_{CH} input current at channel select pin when the channel select voltage is at V_{CH}</p> <p>I_{CL} input current at channel select pin when the channel select voltage is at V_{CL}</p> <p>I_{io} difference between base currents of any input differential pair of transistors</p> <p>I_{o+} output source current to a load with the output remaining above 2.4 volts, excluding the amplifier's own sink current</p> <p>I_{o-} the current that the amplifier will sink into pin 12</p> <p>t_{CMR} time required for the amplifier to recover from the maximum specified common-mode input, (recovery – output within 10% of its quiescent state)</p> <p>$t_{C\ sel}$ time between the 50% point of the channel gate input and the 50% point of the signal input that still allows a full width signal at the amplifier output</p> | <p>t_{DMR} time required for the amplifier to recover from maximum specified differential-mode input, (recovery – output within 10% of its quiescent state)</p> <p>t_{dS} delay time from the 50% point of the strobe input leading or trailing edge to the corresponding 50% point of the output</p> <p>t_f time rise (and time fall) of the input signal must be less than 10 ns</p> <p>t_{pd} the delay time from the 50% point of a 5.0 mV input leading or trailing edge to the corresponding 50% point of the amplifier output</p> <p>t_r time from 10% to 90% of the rise and fall times respectively of the output signal with a 5.0 mV input signal</p> <p>t_{Smin} minimum pulse width at 50% points at strobe input allows a full output (pulse rise times of less than 10 ns, amplifier differential input equal to 3 mV)</p> | <p>V_{CH} minimum voltage required at the channel select pin to cause a given channel to give 99% of the maximum gain through the amplifier</p> <p>V_{CL} maximum voltage allowable at the channel select pin to cause a given channel to give 1% or less of the gain when channel is fully selected</p> <p>V_o output dc level with inputs grounded and strobe high</p> <p>V_{oH} minimum output high level</p> <p>V_{oL} maximum output low level</p> <p>V_{SH} the minimum voltage required at the strobe pin to allow 99% of a full output</p> <p>V_{SL} the maximum voltage allowable at the strobe pin to allow 1% or less of a full output</p> |
|---|---|--|

MC1550

HIGH-FREQUENCY CIRCUITS

INTEGRATED CIRCUIT LINEAR AMPLIFIER



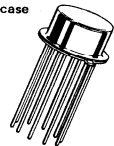
... a versatile, common-emitter, common base cascode circuit for use in communications applications. See Application Notes AN-215, AN-247 and AN-299 for additional information.

- Constant Input Impedance over entire AGC range
- Extremely Low γ_{12} – 4.3 μmhos at 60 MHz
- High Power Gain – 30 dB @ 60 MHz (0.5 MHz BW)
- Good Noise Figure – 5 dB @ 60 MHz

RF – IF AMPLIFIER INTEGRATED CIRCUIT MONOLITHIC SILICON EPITAXIAL PASSIVATED

Pin 7 connected to case

G SUFFIX
METAL PACKAGE
CASE 602B



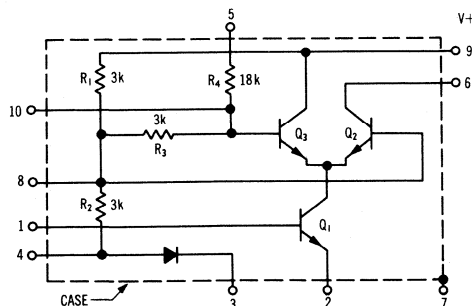
F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|------------------|-------------|----------------------|
| Power Supply Voltage, Pin 9 | V+ | 20 | Vdc |
| AGC Supply Voltage | V _{AGC} | 20 | Vdc |
| Differential Input Voltage, Pin 1 to Pin 4 ($R_S = 500$ ohms) | V _{in} | ± 5.0 | V(rms) |
| Power Dissipation (Package Limitation) | P _D | | |
| Metal Can | | 680 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 4.6 | mW/ $^\circ\text{C}$ |
| Flat Package | | 500 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 3.3 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T _A | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T _{stg} | -65 to +150 | $^\circ\text{C}$ |

CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1550 is built with monolithic fabrication techniques utilizing diffused resistors and small-geometry transistors. Excellent AGC performance is obtained by shunting the signal through the AGC transistor Q_3 , maintaining the operating point of the input transistor Q_1 . This keeps the input impedance constant over the entire AGC range.

The amplifier is intended to be used in a common-emitter, common-base configuration (Q_1 and Q_2) with Q_3 acting as an AGC transistor. The input signal is applied between pins 1 and 4, where pin 4 is ac-coupled to ground. DC source resistance between pins 1 and 4 should be small (less than 100 ohms). Pins 2 and 3 should be connected together and grounded. Pins 8 and 10 should be bypassed to ground. The positive supply voltage is applied at pin 9 and at higher frequencies, pin 9 should also be bypassed to ground. The output is taken between pins 6 and 9. The substrate is connected to pin 7 and should be grounded. AGC voltage is applied to pin 5.

See Packaging Information Section for outline dimensions.

MC1550 (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +6 \text{ Vdc}$, $T_A = +25^\circ\text{C}$)

| Characteristic | Conditions | Figure | Symbol | Min | Typ | Max | Unit |
|---------------------------|---|--------|-----------|--------------|--------|--------------|------|
| DC CHARACTERISTICS | | | | | | | |
| Output Voltage | $V_{AGC} = 0 \text{ Vdc}$ $V_{AGC} = +6 \text{ Vdc}$ | 1 | V_O | 3.80 5.90 | — — | 4.65 6.00 | Vdc |
| Test Voltage | $V_{AGC} = 0 \text{ Vdc}$ $V_{AGC} = +6 \text{ Vdc}$ | 1 | V8 | 2.85 3.25 | — — | 3.40 3.80 | Vdc |
| Supply Drain Current | $V_{AGC} = 0 \text{ Vdc}$ $V_{AGC} = +6 \text{ Vdc}$ | 1 | I_D | — — | — — | 2.2 2.5 | mAdc |
| AGC Supply Drain Current | $V_{AGC} = 0 \text{ Vdc}$ $V_{AGC} = +6 \text{ Vdc}$ | 1 | I_{AGC} | — — | — — | -0.2 0.18 | mAdc |

SMALL-SIGNAL CHARACTERISTICS

| | | | | | | | |
|---------------------------|------------------------------------|---|-------|----|----|----|-----|
| Small-Signal Voltage Gain | $f = 500 \text{ kHz}$ | 2 | A_V | 22 | — | 29 | dB |
| Bandwidth | -3.0 dB | 2 | BW | 22 | — | — | MHz |
| Transducer Power Gain | $f = 60 \text{ MHz}$, BW = 6 MHz | 3 | A_p | — | 25 | — | dB |
| | $f = 100 \text{ MHz}$, BW = 6 MHz | | | — | 21 | — | |

TYPICAL CHARACTERISTICS

($V^+ = 6.0 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 1 – DC CHARACTERISTICS TEST CIRCUIT

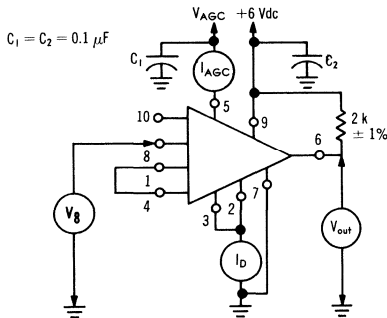


FIGURE 3 – POWER GAIN TEST CIRCUIT @ 60 MHz

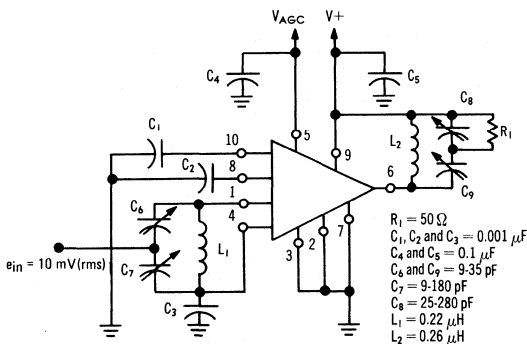


FIGURE 2 – VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT

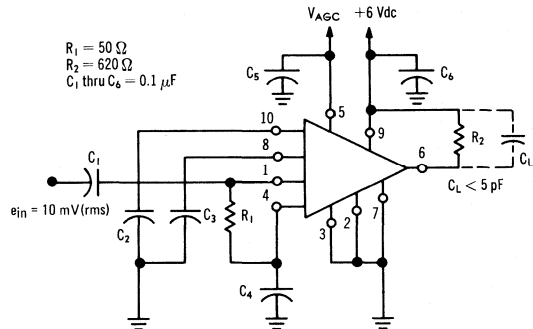
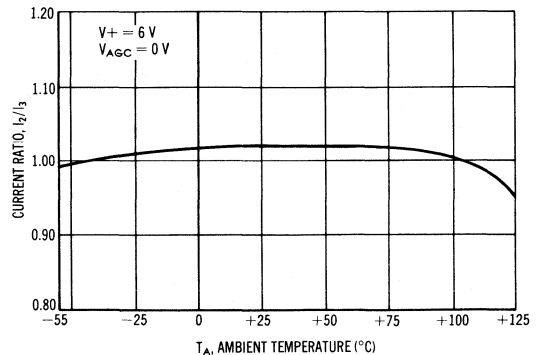


FIGURE 4 – DRAIN CURRENT TEMPERATURE CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

FIGURE 5 – INPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

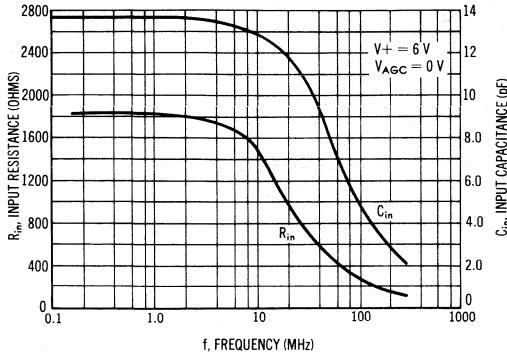


FIGURE 6 – INPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

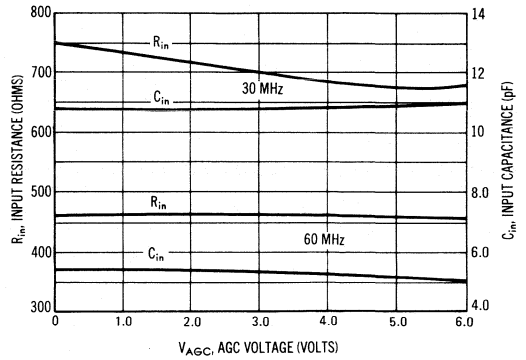


FIGURE 7 – OUTPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

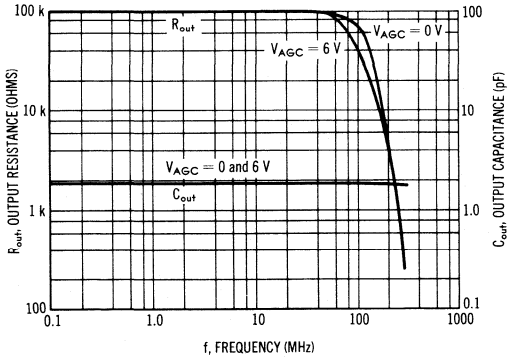


FIGURE 8 – OUTPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

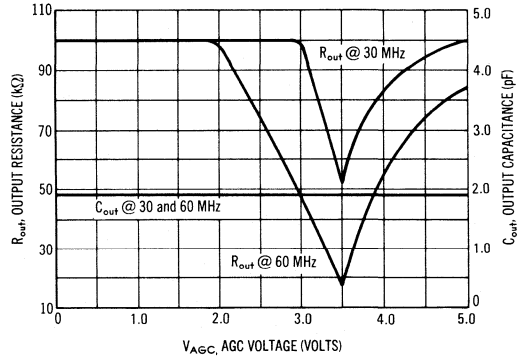


FIGURE 9 – MAXIMUM TRANSDUCER POWER GAIN versus FREQUENCY

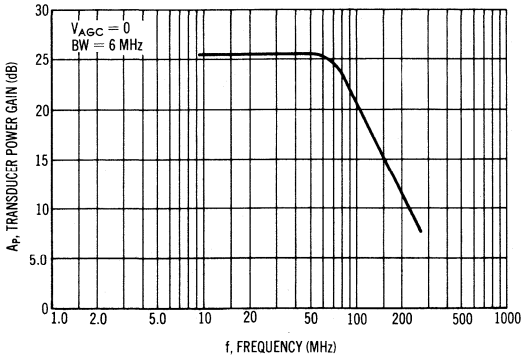
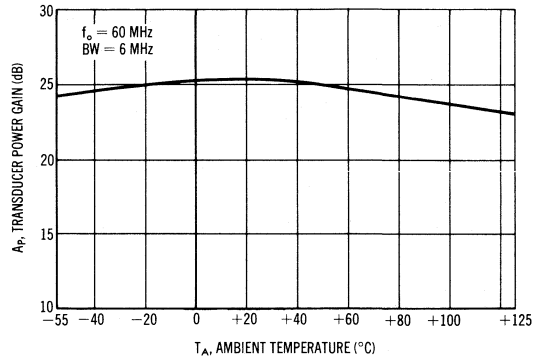


FIGURE 10 – TRANSDUCER POWER GAIN versus TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 11 – TRANSDUCER POWER BANDWIDTH versus AGC VOLTAGE

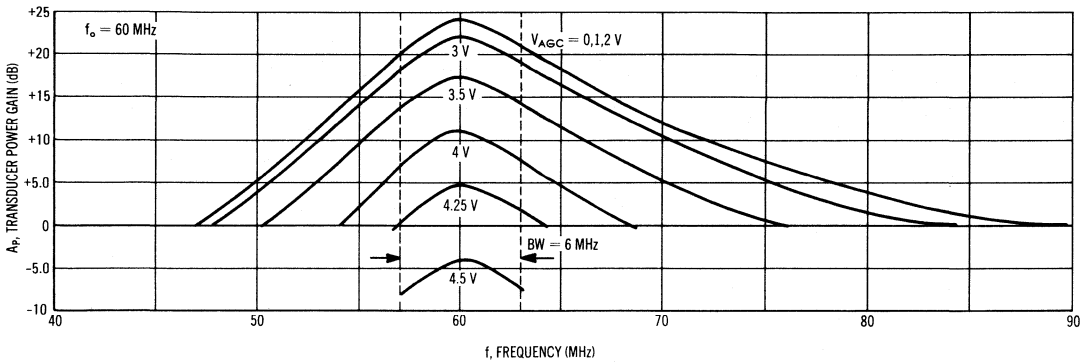


FIGURE 12 – NOISE FIGURE AND OPTIMUM SOURCE RESISTANCE versus FREQUENCY

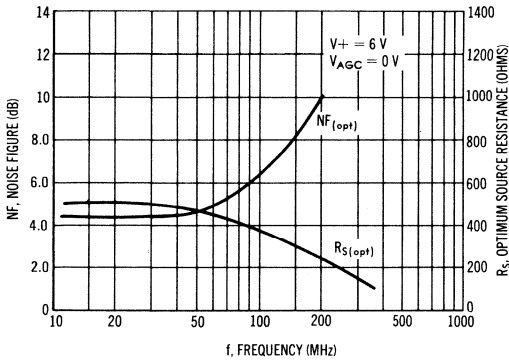


FIGURE 13 – NOISE FIGURE versus SOURCE RESISTANCE

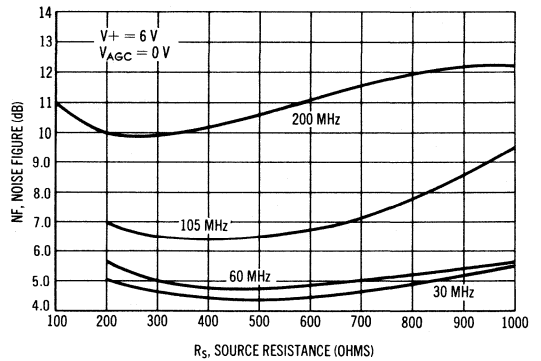


FIGURE 14 – y_{21} , FORWARD-TRANSFER ADMITTANCE versus FREQUENCY

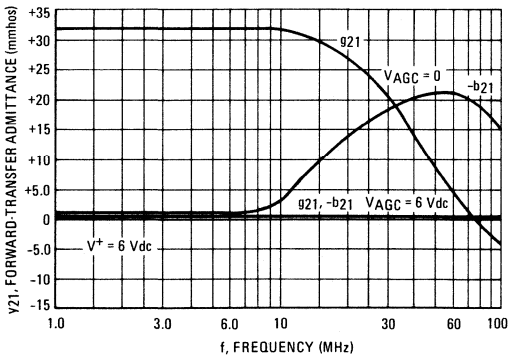
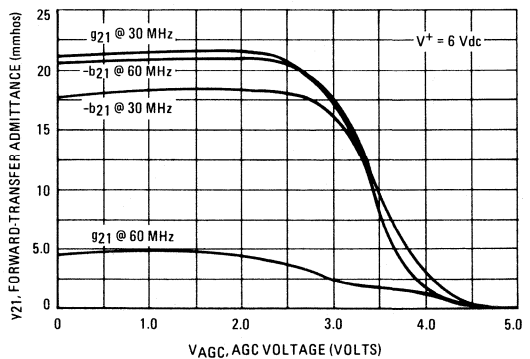


FIGURE 15 – y_{21} , FORWARD-TRANSFER ADMITTANCE versus AGC VOLTAGE



TYPICAL CHARACTERISTICS

($V^+ = 6.0 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 16 – y_{12} , REVERSE TRANSFER-ADMITTANCE versus FREQUENCY

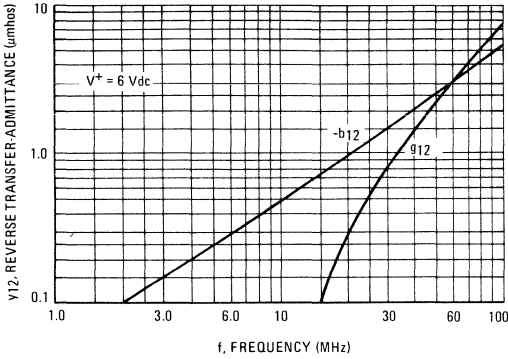


FIGURE 17 – y_{11} , INPUT-ADMITTANCE versus FREQUENCY

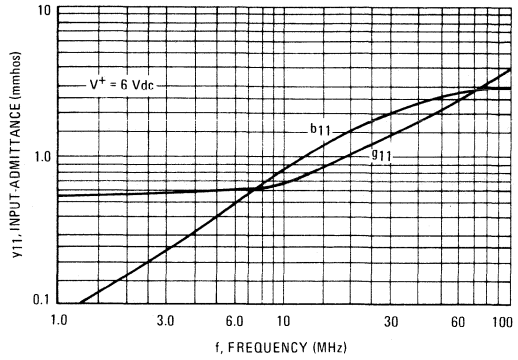
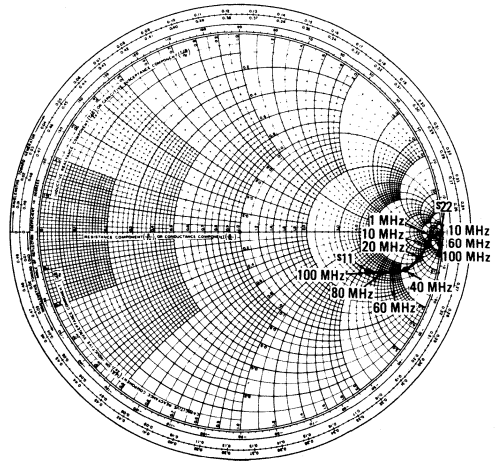


FIGURE 19 – s_{11} AND s_{22} , INPUT AND OUTPUT REFLECTION COEFFICIENT



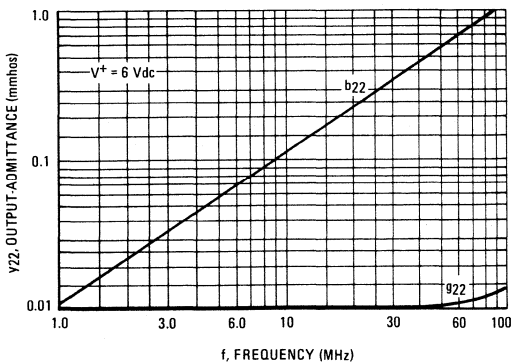
The y_{12} shown in Figure 16 illustrates the extremely low feedback of the MC1550 with no contribution from the external mounting circuitry. However, in many cases the external circuitry may contribute as much or more to the total feedback than does the MC1550.

To perform more accurate design calculations of gain, stability, and input - output impedances it is recommended that the designer first determine the total feedback of device plus circuitry.

This can be done in one of two ways:

- (1) Measure the total y_{12} or s_{12} of the MC1550 installed in its mounting circuitry, or
- (2) Measure the y_{12} of the circuitry alone (without the MC1550 installed) and add the circuit y_{12} to the y_{12} for the MC1550 given in Figure 16.

FIGURE 18 – y_{22} , OUTPUT-ADMITTANCE versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

($V^+ = 6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 20 — s_{11} , INPUT REFLECTION COEFFICIENT versus FREQUENCY

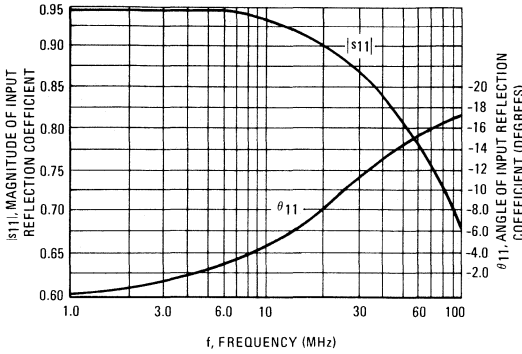


FIGURE 21 — s_{22} , OUTPUT REFLECTION COEFFICIENT versus FREQUENCY

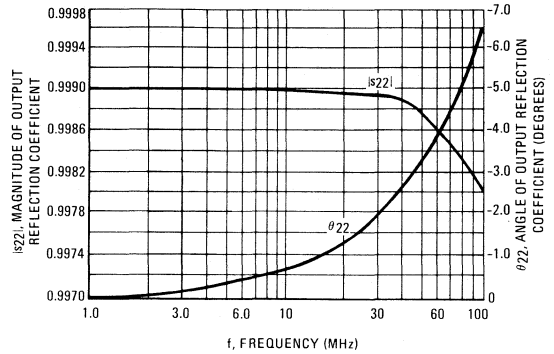


FIGURE 22 — s_{21} , FORWARD TRANSMISSION COEFFICIENT (GAIN)

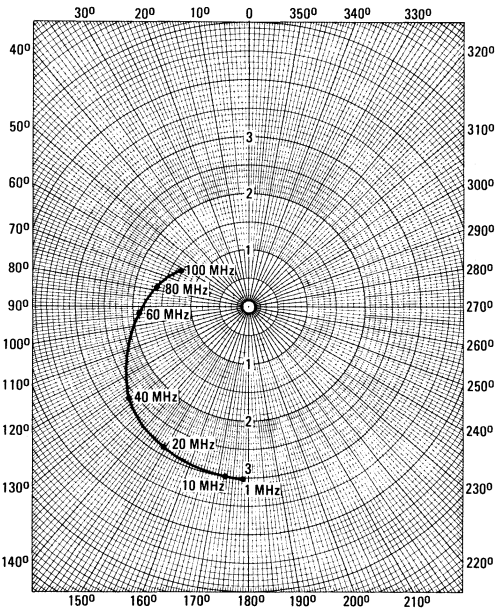
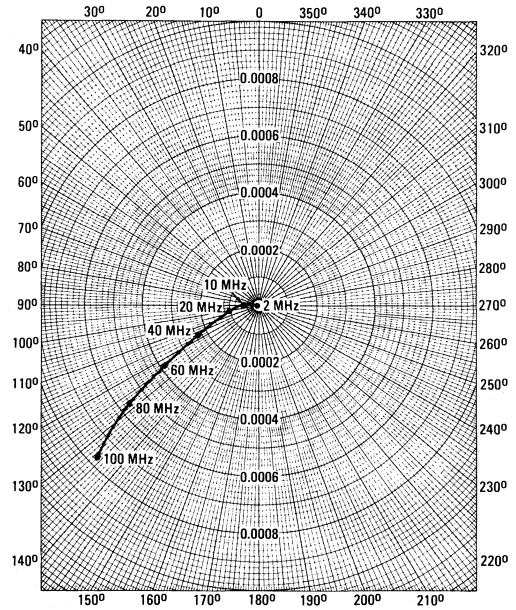


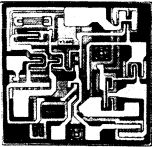
FIGURE 23 — s_{12} , REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



MC1552G

MC1553G

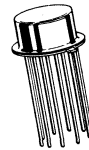
MONOLITHIC VIDEO AMPLIFIER



... a three-stage, direct-coupled, common-emitter cascade incorporating series-series feedback to achieve stable voltage gain, low distortion, and wide bandwidth. Employs a temperature-compensated dc feedback loop to stabilize the operating point and a current-biased emitter follower output. Intended for use as either a wide-band linear amplifier or as a fast rise pulse amplifier.

- High Gain — 34 dB ± 1 dB (MC1552)
52 dB ± 1 dB (MC1553)
- Wide Bandwidth — 40 MHz (MC1552)
35 MHz (MC1553)
- Low Distortion — 0.2% at 200 kHz
- Low Temperature Drift — ±0.002 dB/°C

HIGH FREQUENCY
INTEGRATED CIRCUITS
SILICON
EPITAXIAL PASSIVATED



METAL PACKAGE
CASE 602B

Pin 6 connected to case

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|------------------|-------------|-------------|
| Power Supply Voltage, Pin 9 | V ⁺ | 9 | Vdc |
| Input Voltage, Pin 1 to Pin 2 (R _S = 500 ohms) | V _{in} | 1.0 | V(rms) |
| Power Dissipation (Package Limitation) Derate above T _A = +25°C | P _D | 680 4.6 | mW mW/°C |
| Operating Temperature Range | T _A | -55 to +125 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

CIRCUIT SCHEMATICS

FIGURE 1 — MC1552 (LOW GAIN)

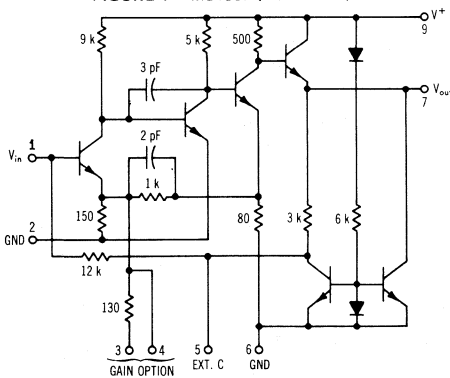
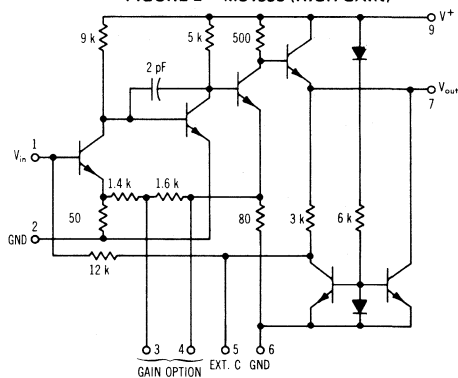


FIGURE 2 — MC1553 (HIGH GAIN)



See Packaging Information Section for outline dimensions.

MC1552G, MC1553G (continued)

ELECTRICAL CHARACTERISTICS (V₊ = +6 Vdc, T_A = +25°C unless otherwise noted)

| Characteristic | Fig. No. | Gain * Option | Symbol | Min | Typ | Max | Unit |
|--|----------|---------------|---------------------------------------|-----|-------|-----|------|
| Voltage Gain MC1552 | 3 | 50 | V _{out} /V _{in} | 44 | 50 | 56 | V/V |
| MC1553 | | 100 | | 87 | 100 | 113 | |
| | | 200 | | 175 | 200 | 225 | |
| | | 400 | | 350 | 400 | 450 | |
| Voltage Gain Variation (T _A = -55°C to +125°C) | 3 | All | — | — | ±0.2 | — | dB |
| Bandwidth | 3, 6 | 50 | BW | 21 | 40 | — | MHz |
| MC1552 | | 100 | | 17 | 35 | — | |
| MC1553 | | 200 | | 17 | 35 | — | |
| | | 400 | | 7.5 | 15 | — | |
| Input Impedance (f = 100 kHz, R _L = 1 kΩ) | — | All | Z _{in} | 7 | 10 | — | kΩ |
| Output Impedance (f = 100 kHz, R _S = 50 Ω) | — | All | Z _{out} | — | 16 | 50 | Ω |
| DC Output Voltage | 3 | All | V _{out} (dc) | 2.5 | 2.9 | 3.2 | Vdc |
| DC Output Voltage Variation (T _A = -55°C to +125°C) | 3 | All | ΔV _{out} (dc) | — | ±0.05 | — | Vdc |
| Output Voltage Swing (Z _L ≥ 1 kΩ, V _{in} = 100 mV(rms)) | 3 | All | V _{out} | 3.6 | 4.2 | — | Vp-p |
| Power Dissipation | — | All | P _D | — | 75 | 120 | mW |
| Delay Time | 3, 4 | 50 | t _{pd} | — | 8 | — | ns |
| MC1552 | | 100 | | — | 9 | — | |
| MC1553 | | 200 | | — | 10 | — | |
| | | 400 | | — | 25 | — | |
| Rise Time | 3, 4 | 50 | t _r | — | 9 | 16 | ns |
| MC1552 | | 100 | | — | 12 | 20 | |
| MC1553 | | 200 | | — | 11 | 20 | |
| | | 400 | | — | 30 | 45 | |
| Overshoot | 3, 4 | All | (V _{os} /V _p)100 | — | 5 | — | % |
| Noise Figure (R _S = 400 Ω, f _o = 30 MHz, BW = 3 MHz) | — | All | NF | — | 5 | — | dB |
| Total Harmonic Distortion (V _{out} = 2 Vp-p, f = 200 kHz, R _L = 1 kΩ) | — | All | THD | — | 0.2 | — | % |

*To obtain the voltage-gain characteristic desired, use the following pin connections:

| Type | Voltage Gain | Pin Connections |
|--------|--------------|------------------------|
| MC1552 | 50 | Pin 3 Open |
| | 100 | Ground Pin 3 |
| | 200 | Connect Pin 3 to Pin 4 |
| MC1553 | 400 | Pins 3 and 4 Open |

1. Ground Pin 6 as close to can as possible to minimize overshoot. Best results by directly grounding can.
2. If large input and output coupling capacitors are used, place shield between them to avoid input-output coupling.
3. A high-frequency capacitor must always be used to bypass the power supply. This capacitor should be as close to the circuit as possible.
4. Voltage gain can be adjusted to any value between 50 and 3000 by connecting an external resistor from Pin 4 to ground on MC1552, or from Pin 3 to ground on MC1553, as shown in

Figure 8. Under these conditions, the following equations must be used to determine C₁ and C₂ rather than the circuits shown in Figure 5.

$$\text{Fig. 5b } C_1 = \frac{1}{2\pi f_c (1.7 \times 10^4)} \text{ Farads; } C_2 = \frac{1}{8 C_1 (V_{out}/V_{in})} \text{ Farads}$$

$$\text{Fig. 5c } C_1 = \frac{V_{out}/V_{in}}{2\pi f_c (1.5 \times 10^4)} \text{ Farads}$$

$$\text{Fig. 5d } C_2 = \frac{V_{out}/V_{in}}{2\pi f_c (3 \times 10^3)} \text{ Farads}$$

FIGURE 3 – TEST CIRCUIT

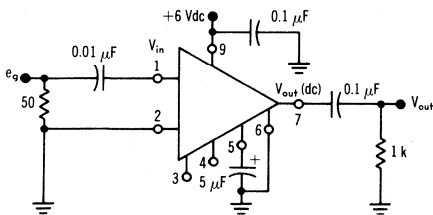
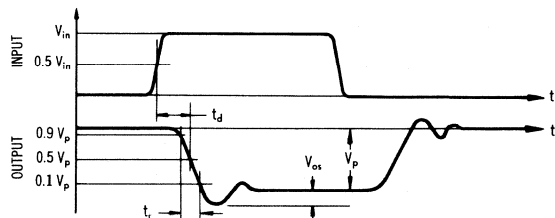


FIGURE 4 – PULSE RESPONSE DEFINITIONS

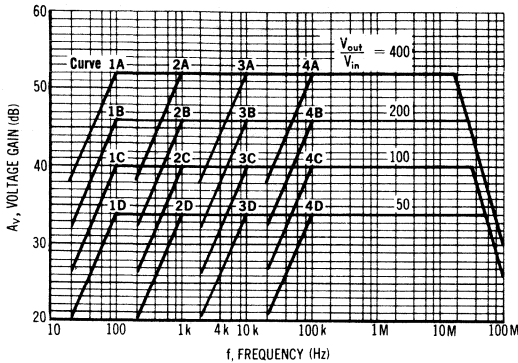


MC1552G, MC1553G (continued)

TYPICAL CHARACTERISTICS

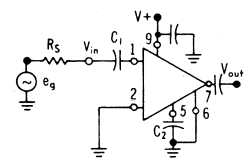
$T_A = +25^\circ\text{C}$

FIGURE 5a – FREQUENCY RESPONSE



TEST CIRCUITS FOR FREQUENCY RESPONSE

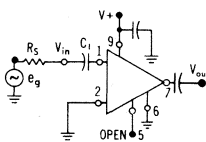
FIGURE 5b – CAPACITIVE COUPLED INPUT ($R_S < 5\text{ k}\Omega$)



| Curve No. | C_1 (μF) | C_2 (μF) |
|-----------|-------------------------|-------------------------|
| 1A | 0.1 | 250 |
| 1B | 0.1 | 150 |
| 1C | 0.1 | 70 |
| 1D | 0.1 | 40 |

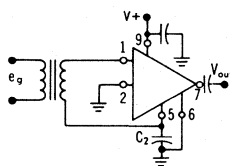
| Curve No. | C_1 (μF) | C_2 (μF) |
|-----------|-------------------------|-------------------------|
| 2A | 0.01 | 30 |
| 2B | 0.01 | 18 |
| 2C | 0.01 | 8.0 |
| 2D | 0.01 | 4.0 |
| (pF) | | |
| 3A | 1000 | 3.0 |
| 3B | 1000 | 1.8 |
| 3C | 1000 | 0.8 |
| 3D | 1000 | 0.4 |
| 4A | 100 | 0.3 |
| 4B | 100 | 0.18 |
| 4C | 100 | 0.08 |
| 4D | 100 | 0.04 |

FIGURE 5c – CAPACITIVE COUPLED INPUT ($R_S < 500\ \Omega$)



| Curve No. | C_1 (μF) | Curve No. | C_1 (μF) |
|-----------|-------------------------|-----------|-------------------------|
| 1A | 20 | 3A | 0.4 |
| 1B | 10 | 3B | 0.2 |
| 1C | 7.0 | 3C | 0.1 |
| 1D | 3.0 | 3D | 0.06 |
| 2A | 3.0 | 4A | 0.04 |
| 2B | 1.0 | 4B | 0.02 |
| 2C | 0.8 | 4C | 0.01 |
| 2D | 0.5 | 4D | 0.007 |

FIGURE 5d – TRANSFORMER COUPLED INPUT



| Curve No. | C_2 (μF) | Curve No. | C_2 (μF) |
|-----------|-------------------------|-----------|-------------------------|
| 1A | 200 | 3A | 2.0 |
| 1B | 100 | 3B | 1.0 |
| 1C | 70 | 3C | 0.7 |
| 1D | 30 | 3D | 0.3 |
| 2A | 20 | 4A | 0.2 |
| 2B | 10 | 4B | 0.1 |
| 2C | 7.0 | 4C | 0.07 |
| 2D | 3.0 | 4D | 0.03 |

FIGURE 6 – VOLTAGE GAIN versus FREQUENCY

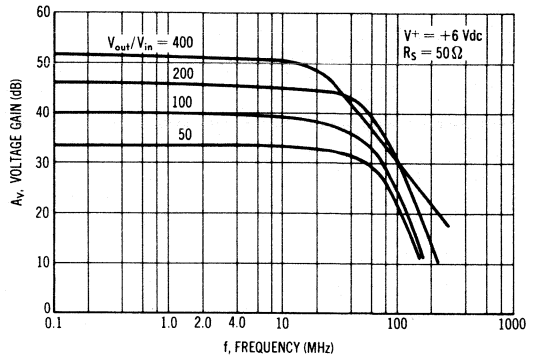


FIGURE 7 – MAXIMUM NEGATIVE SWING SLEW RATE versus LOAD CAPACITANCE

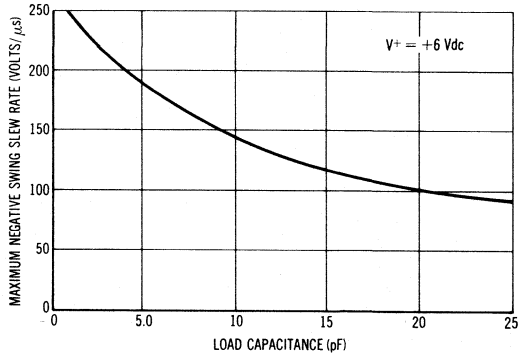
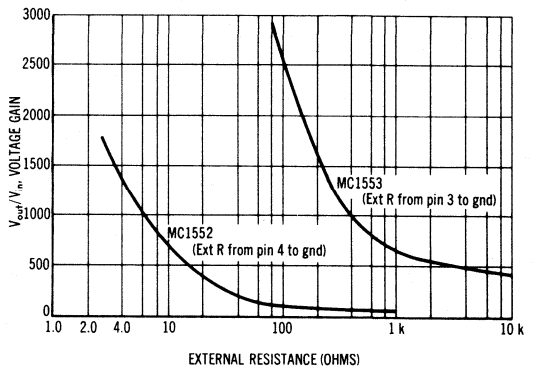


FIGURE 8 – VOLTAGE GAIN ADJUSTMENT BY USE OF EXTERNAL RESISTOR



INPUT ADMITTANCE

$V^+ = 6 \text{ Vdc}$, $R_L = 1 \text{ k}\Omega$, $T_A = +25^\circ\text{C}$

FIGURE 9 – GAIN = 50

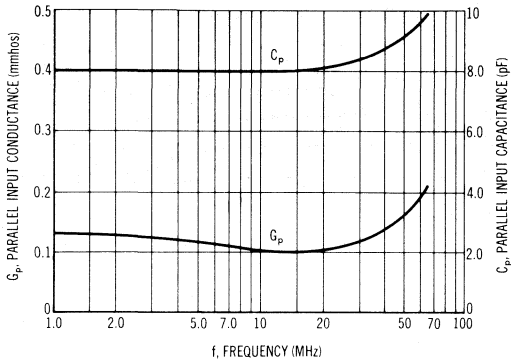


FIGURE 10 – GAIN = 100

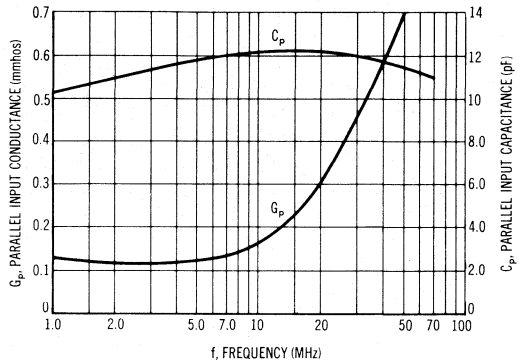


FIGURE 11 – GAIN = 200

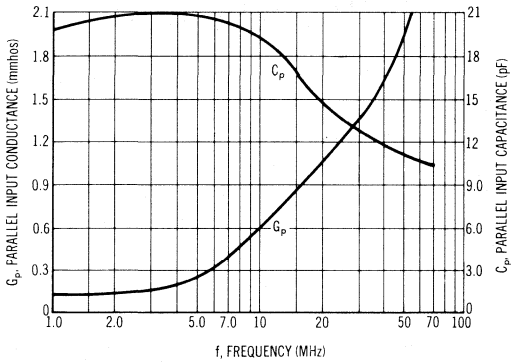


FIGURE 12 – GAIN = 400

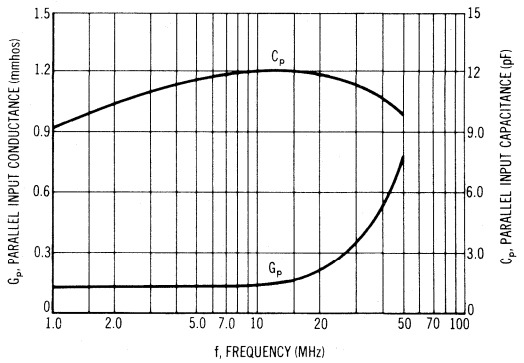


FIGURE 13 – OUTPUT IMPEDANCE versus FREQUENCY

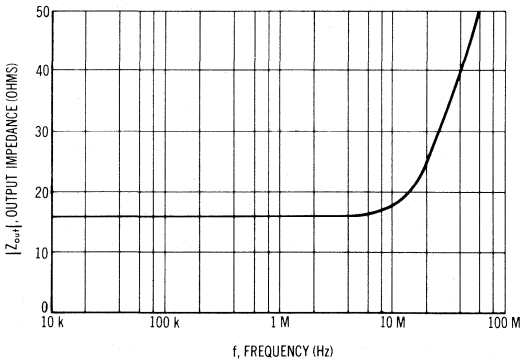
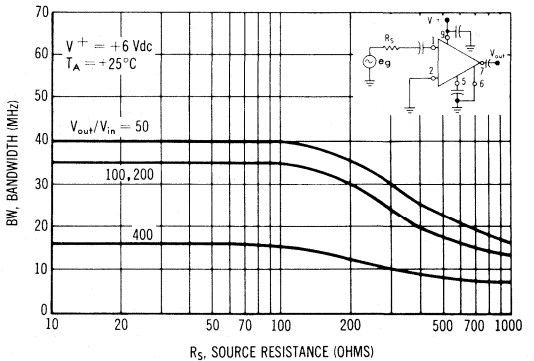


FIGURE 14 – BANDWIDTH versus SOURCE RESISTANCE

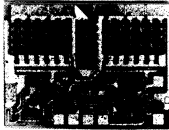


7

MC1554G MC1454G

POWER AMPLIFIER

MONOLITHIC 1-WATT POWER AMPLIFIERS

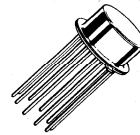


... designed to amplify signals to 300-kHz with 1-Watt delivered to a direct coupled or capacitively coupled load.

- Low Total Harmonic Distortion – 0.4% (Typ) @ 1 Watt
- Low Output Impedance – 0.2 Ohm
- Excellent Gain – Temperature Stability

1-WATT POWER AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC
SILICON EPITAXIAL PASSIVATED



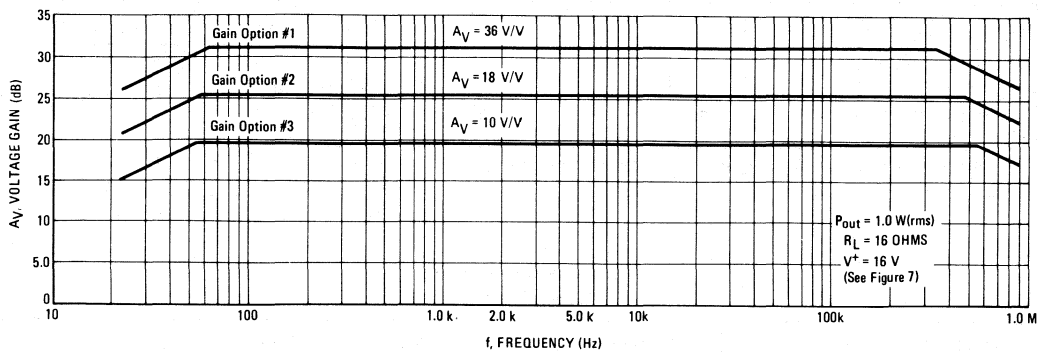
METAL PACKAGE
CASE 602B



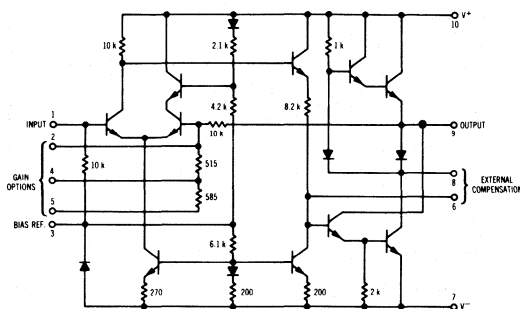
(bottom view)

Pin 7 connected to case

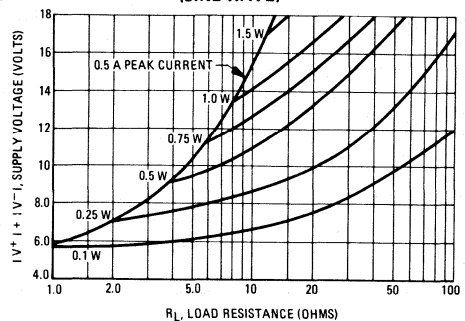
VOLTAGE GAIN versus FREQUENCY ($R_L = 16 \text{ OHMS}$)



CIRCUIT SCHEMATIC



MAXIMUM AVAILABLE OUTPUT POWER (SINE WAVE)



See Packaging Information Section for outline dimensions.

MC1554G, MC1454G (continued)

ELECTRICAL CHARACTERISTICS ($T_C = +25^\circ\text{C}$ unless otherwise noted)
 Frequency compensation shown in Figures 6 and 7.

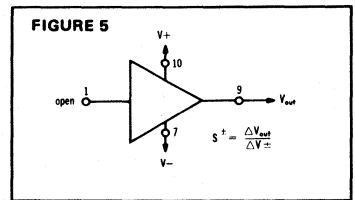
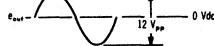
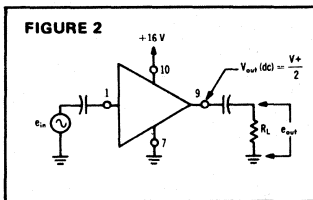
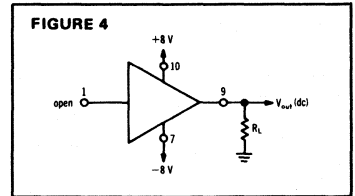
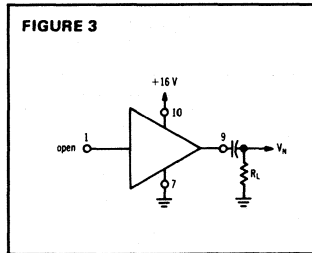
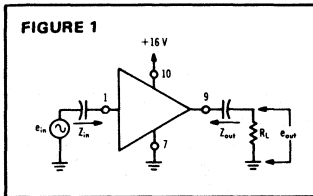
| Characteristic | Figure | R _L (Ohms) | Gain Option* | Symbol | MC1554 (-55 to +125°C) | | | MC1454 (0 to +70°C) | | | Unit | | | | | | | | | |
|--|--------|--------------------------|-----------------|----------------------|---------------------------|-----|-----|------------------------|-----|-----|---------|--|----|----|---|-----|---|---|-----|---|
| | | | | | Min | Typ | Max | Min | Typ | Max | | | | | | | | | | |
| Output Power (for e _{out} < 5.0% THD) | 1 | 16 | — | P _{out} | 1.0 | 1.1 | — | — | 1.0 | — | Watt | | | | | | | | | |
| Power Dissipation (@ P _{out} = 1.0 W) | 1 | 16 | — | P _D | — | 0.9 | 1.2 | — | 0.9 | — | Watt | | | | | | | | | |
| Voltage Gain | 1 | 16 | 10 | A _V | 8.0 | 10 | 12 | — | 10 | — | V/V | | | | | | | | | |
| | | 16 | 18 | | — | 18 | — | 18 | — | | | | | | | | | | | |
| | | 16 | 36 | | — | 36 | — | 36 | — | | | | | | | | | | | |
| Input Impedance | 1 | — | 10 | Z _{in} | 7.0 | 10 | — | 3.0 | 10 | — | kΩ | | | | | | | | | |
| Output Impedance | 1 | — | 10 | Z _{out} | — | 0.2 | — | — | 0.4 | — | Ω | | | | | | | | | |
| Power Bandwidth (for e _{out} < 5.0% THD) | 2 | 16 | 10 | | — | 270 | — | — | 270 | — | kHz | | | | | | | | | |
| | | 16 | 18 | | — | 250 | — | 250 | — | | | | | | | | | | | |
| | | 16 | 36 | | — | 210 | — | 210 | — | | | | | | | | | | | |
| Total Harmonic Distortion (for e _{in} < 0.05% THD, f = 20 Hz to 20 kHz) | 2 | | | THD | | | | | | | % | | | | | | | | | |
| | | | | | | | | | | | | P _{out} = 1.0 Watt (sinewave) | 16 | 10 | — | 0.4 | — | — | 0.4 | — |
| | | | | | | | | | | | | P _{out} = 0.1 Watt (sinewave) | 16 | 10 | — | 0.5 | — | — | 0.5 | — |
| Zero Signal Current Drain | 3 | ∞ | — | I _D | — | 11 | 15 | — | 11 | 20 | mAdc | | | | | | | | | |
| Output Noise Voltage | 3 | 16 | 10 | V _n | — | 0.3 | — | — | 0.3 | — | mV(rms) | | | | | | | | | |
| Output Quiescent Voltage (Split Supply Operation) | 4 | 16 | — | V _{out(dc)} | — | ±10 | ±30 | — | ±10 | — | mVdc | | | | | | | | | |
| Positive Supply Sensitivity (V ⁻ constant) | 5 | ∞ | — | S ⁺ | — | -40 | — | — | -40 | — | mV/V | | | | | | | | | |
| Negative Supply Sensitivity (V ⁺ constant) | 5 | ∞ | — | S ⁻ | — | -40 | — | — | -40 | — | mV/V | | | | | | | | | |

*To obtain the voltage gain characteristic desired, use the following pin connections: Voltage Gain

Pin Connection

- 10 Pins 2 and 4 open, Pin 5 to ac ground
- 18 Pins 2 and 5 open, Pin 4 to ac ground
- 36 Pin 2 connected to Pin 5, Pin 4 to ac ground

Characteristic Definitions (Linear Operation)



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MC1554G, MC1454G (continued)

MAXIMUM RATINGS ($T_C = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit | |
|--|------------------|-----------|-------------------------------|------------------|
| Total Power Supply Voltage | $ V^+ + V^- $ | 18 | Vdc | |
| Peak Load Current | I_{out} | 0.5 | Ampere | |
| Audio Output Power | P_{out} | 1.8 | Watts | |
| Power Dissipation (package limitation) | | | | |
| $T_A = +25^\circ\text{C}$ Derate above 25°C | P_D | 600 | mW | |
| | $1/\theta_{JA}$ | 4.8 | $\text{mW}/^\circ\text{C}$ | |
| $T_C = +25^\circ\text{C}$ Derate above 25°C | P_D | 1.8 | Watts | |
| | $1/\theta_{JC}$ | 14.4 | $\text{mW}/^\circ\text{C}$ | |
| Operating Temperature Range | MC1454 MC1554 | T_A | 0 to $+70$ -55 to $+125$ | $^\circ\text{C}$ |
| Storage Temperature Range | | T_{stg} | -55 to $+150$ | $^\circ\text{C}$ |

TYPICAL CONNECTIONS

FIGURE 6 – SPLIT SUPPLY OPERATION VOLTAGE
GAIN (A_V) = 10, $f_{LOW} \approx 25$ Hz

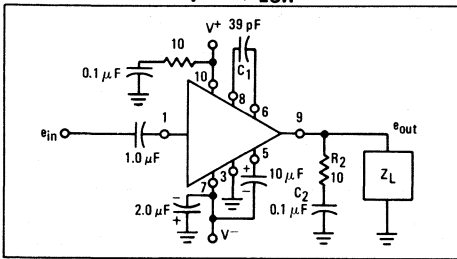
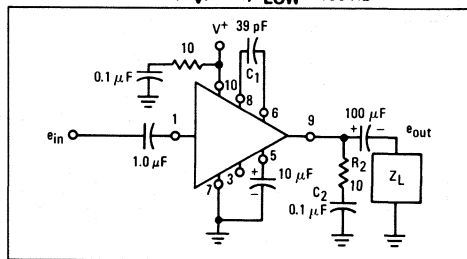


FIGURE 7 – SINGLE SUPPLY OPERATION VOLTAGE
GAIN (A_V) = 10, $f_{LOW} \approx 100$ Hz



RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to:

1. An R-C stabilizing network (0.1 μF in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 6 and 7, using short leads, to eliminate local VHF instability caused by lead inductance to the load.
2. Excessive lead inductance from the V^+ supply to pin 10 can cause high frequency instability. To prevent this, the V^+ by-pass capacitor should be connected with short leads from the V^+ pin to ground. If this capacitor is remotely located a series R-C network (0.1 μF and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 6 and 7.

3. Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points.

Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads. This can be assured by either (a) use of short leads which are well isolated, (b) narrow-banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low-pass filter in combination with the source impedance, or (c) use of a shielded input cable. In applications which require upper band-edge control the input low-pass filter is recommended.

TYPICAL CHARACTERISTICS

FIGURE 8 – TOTAL HARMONIC DISTORTION
versus LOAD RESISTANCE

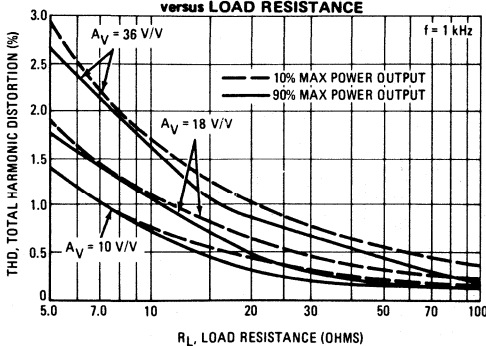
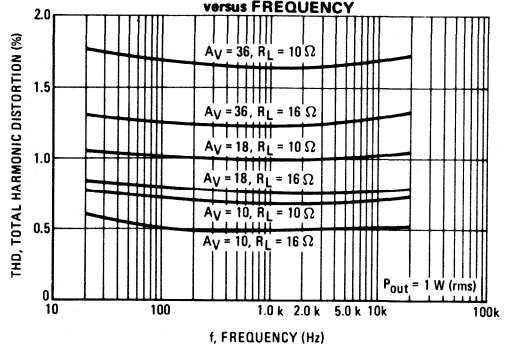


FIGURE 9 – TOTAL HARMONIC DISTORTION
versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – VOLTAGE GAIN versus TEMPERATURE

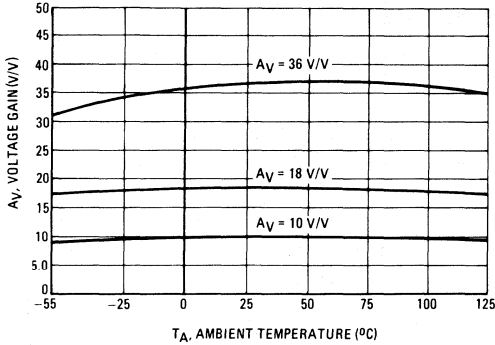


FIGURE 11 – OUTPUT VOLTAGE CHANGE

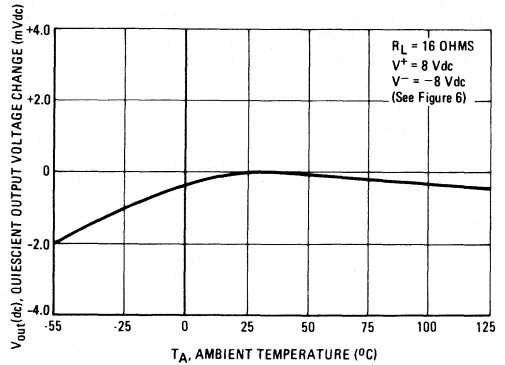


FIGURE 12 – VOLTAGE GAIN versus FREQUENCY ($R_L = \infty$)

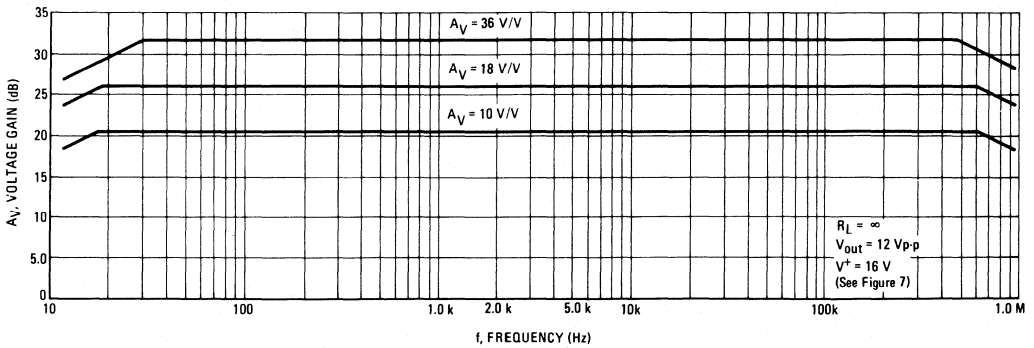
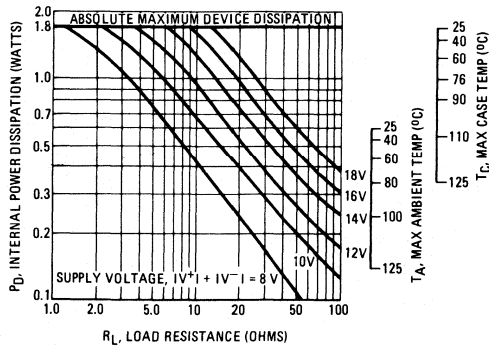


FIGURE 13 – MAXIMUM DEVICE DISSIPATION (SINE WAVE)



7

MC1556G
MC1456G
MC1456CG

**INTERNALLY COMPENSATED, HIGH PERFORMANCE
 MONOLITHIC OPERATIONAL AMPLIFIER**

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information, see Application Note AN-522.

- Low Input Bias Current – 15 nA max
- Low Input Offset Current – 2.0 nA max
- Low Input Offset Voltage – 4.0 mV max
- Fast Slew Rate – 2.5 V/ μ s typ
- Large Power Bandwidth – 40 kHz typ
- Low Power Consumption – 45 mW max
- Offset Voltage Null Capability
- Output Short-Circuit Protection
- Input Over-Voltage Protection

**OPERATIONAL AMPLIFIER
 INTEGRATED CIRCUIT**

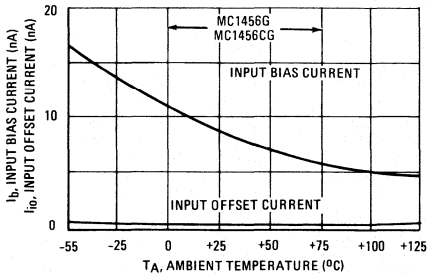
EPITAXIAL PASSIVATED

CASE 601
 TO-99

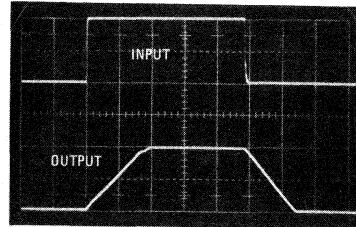


(bottom view)

**TYPICAL INPUT BIAS CURRENT AND INPUT
 OFFSET CURRENT versus TEMPERATURE for MC1556G**

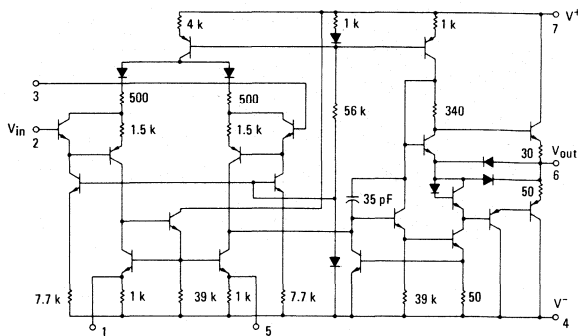


VOLTAGE-FOLLOWER PULSE RESPONSE

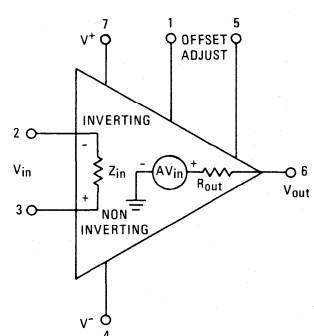


2 μ s/DIVISION

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

MC1556G, MC1456G, MC1456CG (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | MC1456G | | Unit |
|---|-------------------|-----------------|-------------|-------|
| | | MC1556G | MC1456CG | |
| Power Supply Voltage | V ⁺ | +22 | +18 | Vdc |
| | V ⁻ | -22 | -18 | |
| Differential Input Signal | V _{in} | ±V ⁺ | | Volts |
| Common-Mode Input Swing | CMV _{in} | ±V ⁺ | | Volts |
| Load Current | I _L | 20 | | mA |
| Output Short Circuit Duration | t _S | Continuous | | |
| Power Dissipation (Package Limitation) Derate above T _A = +25°C | P _D | 680 | | mW |
| | | 4.6 | | mW/°C |
| Operating Temperature Range | T _A | -55 to +125 | 0 to +75 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V⁺ = +15 Vdc, V⁻ = -15 Vdc, T_A = +25°C unless otherwise noted)

| Characteristic | Fig. | Symbol | MC1556G | | | MC1456G | | | MC1456CG | | | Unit |
|---|-------|--|---------|-----------|-----|---------|-----------|-----|----------|-----------|-----|------------------------|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current T _A = +25°C T _A = T _{low} to T _{high} (See Note 1) | | I _b | - | 6.0 | 15 | - | 15 | 30 | - | 15 | 90 | nAdc |
| | | | - | - | 30 | - | - | 40 | - | - | - | |
| Input Offset Current T _A = +25°C T _A = +25°C to T _{high} T _A = T _{low} to +25°C | | I _{io} | - | 1.0 | 3.0 | - | 5.0 | 10 | - | 5.0 | 30 | nAdc |
| | | | - | - | 3.0 | - | - | 14 | - | - | - | |
| | | | - | - | 6.0 | - | - | 14 | - | - | - | |
| Input Offset Voltage T _A = +25°C T _A = T _{low} to T _{high} | | V _{io} | - | 2.0 | 4.0 | - | 5.0 | 10 | - | 5.0 | 12 | mVdc |
| | | | - | - | 6.0 | - | - | 14 | - | - | - | |
| Differential Input Impedance (Open-Loop, f = 20 Hz) Parallel Input Resistance Parallel Input Capacitance | | R _p C _p | - | 5.0 | - | - | 3.0 | - | - | 3.0 | - | Meg ohms pF |
| | | | - | 6.0 | - | - | 6.0 | - | - | 6.0 | - | |
| Common-Mode Input Impedance (f = 20 Hz) | | Z _{in} | - | 250 | - | - | 250 | - | - | 250 | - | Meg ohms |
| Common-Mode Input Voltage Swing | 1 | CMV _{in} | ±12 | ±13 | - | ±11 | ±12 | - | ±10.5 | ±12 | - | V _{pk} |
| Equivalent Input Noise Voltage (A _V = 100, R _s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz) | 2 | e _n | - | 45 | - | - | 45 | - | - | 45 | - | nV/(Hz) ^{1/2} |
| Common-Mode Rejection Ratio (f = 100 Hz) | 3 | CM _{rej} | 60 | 110 | - | 70 | 110 | - | - | 110 | - | dB |
| Open-Loop Voltage Gain, (V _{out} = ±10 V, R _L = 2.0 k ohms) T _A = +25°C T _A = T _{low} to T _{high} | 4,5,6 | A _{VOL} | 100,000 | 200,000 | - | 70,000 | 100,000 | - | 25,000 | 100,000 | - | V/V |
| | | | 40,000 | - | - | 40,000 | - | - | - | - | - | |
| Power Bandwidth (A _V = 1, R _L = 2.0 k ohms, THD ≤ 5%, V _{out} = 20 V _{p-p}) | 9 | P _{BW} | - | 40 | - | - | 40 | - | - | 40 | - | kHz |
| Unity Gain Crossover Frequency (open-loop) | 5 | f _c | - | 1.0 | - | - | 1.0 | - | - | 1.0 | - | MHz |
| Phase Margin (open-loop, unity gain) | 5,7 | | - | 70 | - | - | 70 | - | - | 70 | - | degrees |
| Gain Margin | 5,7 | | - | 18 | - | - | 18 | - | - | 18 | - | dB |
| Slew Rate (Unity Gain) | | dV _{out} /dt | - | 2.5 | - | - | 2.5 | - | - | 2.5 | - | V/μs |
| Output Impedance (f = 20 Hz) | | Z _{out} | - | 1.0 | 2.0 | - | 1.0 | 2.5 | - | 1.0 | - | kohms |
| Short-Circuit Output Current | 8 | I _{SC} | - | -17, +9.0 | - | - | -17, +9.0 | - | - | -17, +9.0 | - | mA _{dc} |
| Output Voltage Swing (R _L = 2.0 k ohms) | 10 | V _{out} | ±12 | ±13 | - | ±11 | ±12 | - | ±10 | ±12 | - | V _{pk} |
| Power Supply Sensitivity V ⁻ = constant, R _s ≤ 10 k ohms V ⁺ = constant, R _s ≤ 10 k ohms | | S ⁺ S ⁻ | - | 50 | 100 | - | 75 | 200 | - | 75 | - | μV/V |
| | | | - | 50 | 100 | - | 75 | 200 | - | 75 | - | |
| Power Supply Current | | I _D ⁺ I _D ⁻ | - | 1.0 | 1.5 | - | 1.3 | 3.0 | - | 1.3 | 4.0 | mA _{dc} |
| | | | - | 1.0 | 1.5 | - | 1.3 | 3.0 | - | 1.3 | 4.0 | |
| DC Quiescent Power Dissipation (V _{out} = 0) | 11 | P _D | - | 50 | 45 | - | 40 | 90 | - | 40 | 120 | mW |

Note 1: T_{low}: 0° for MC1456G and MC1456CG
-55°C for MC1556G

T_{high}: +75°C for MC1456G and MC1456CG
+125°C for MC1556G

7

TYPICAL CHARACTERISTICS

($V^+ = +15\text{ Vdc}$, $V^- = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 1 – INPUT COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

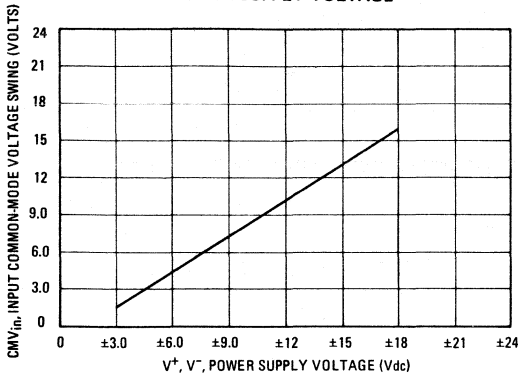


FIGURE 2 – SPECTRAL NOISE DENSITY

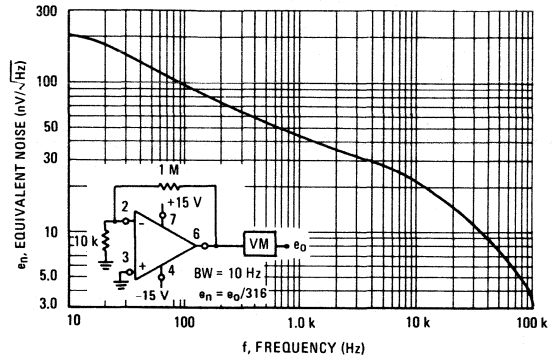


FIGURE 3 – COMMON-MODE REJECTION RATIO versus FREQUENCY

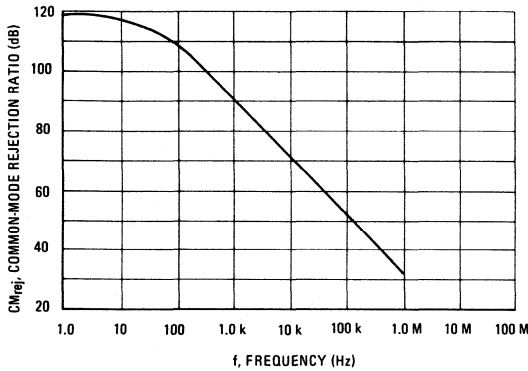


FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

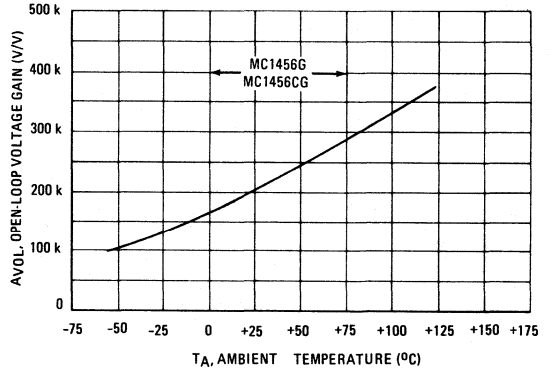


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

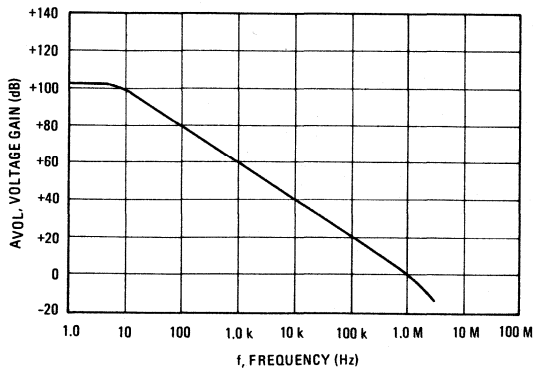
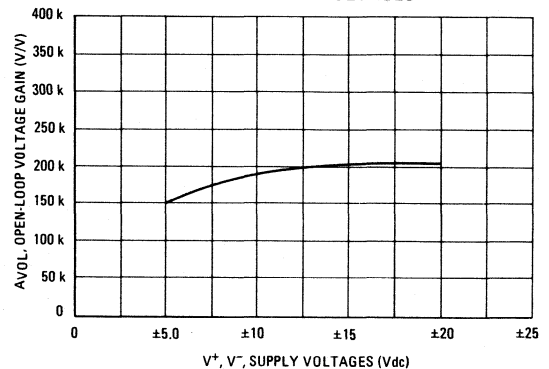


FIGURE 6 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGES



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OPEN-LOOP PHASE SHIFT

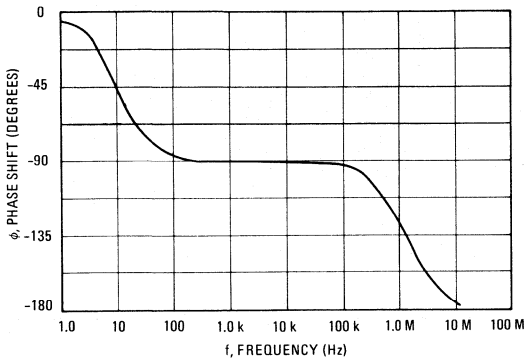


FIGURE 8 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

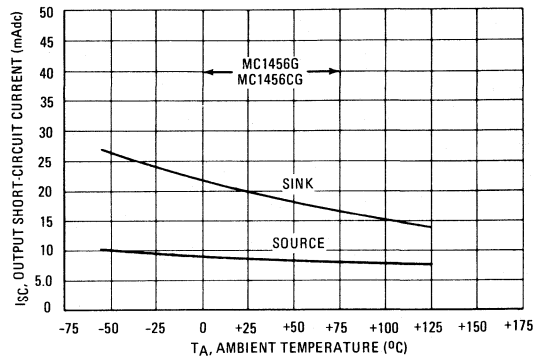


FIGURE 9 – POWER BANDWIDTH

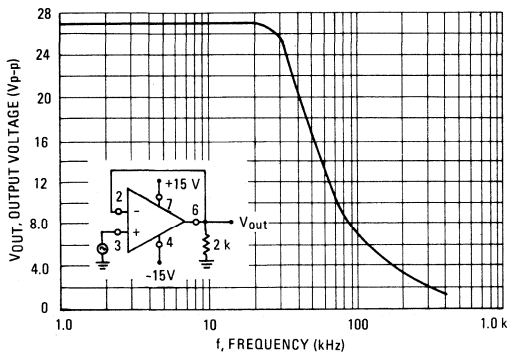


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

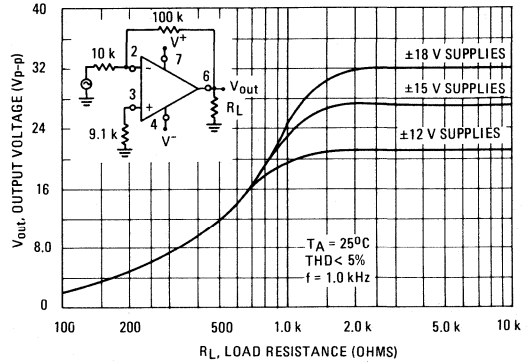
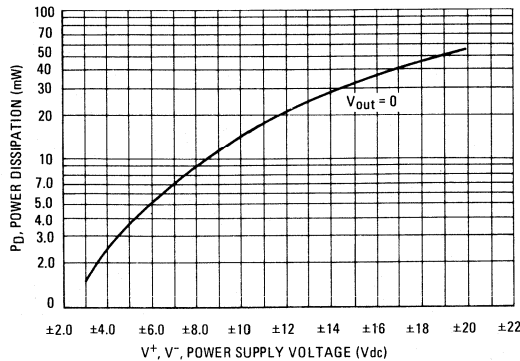


FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



TYPICAL APPLICATIONS

Where values are not given for external components they must be selected by the designer to fit the requirements of the system.

FIGURE 12 – INVERTING FEEDBACK MODEL

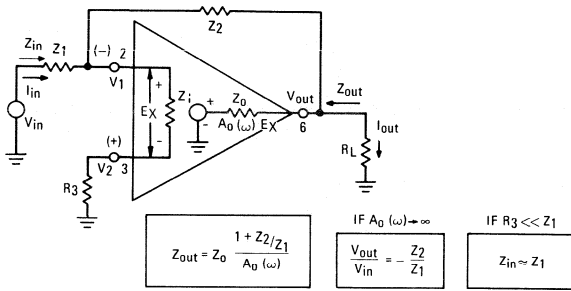


FIGURE 13 – NON-INVERTING FEEDBACK MODEL

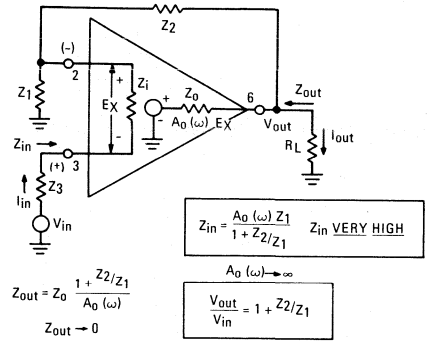


FIGURE 14 – LOW-DRIFT SAMPLE AND HOLD

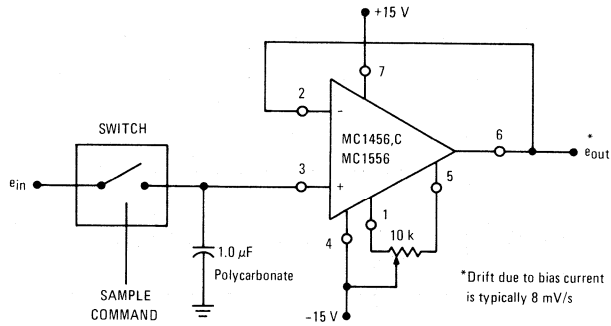
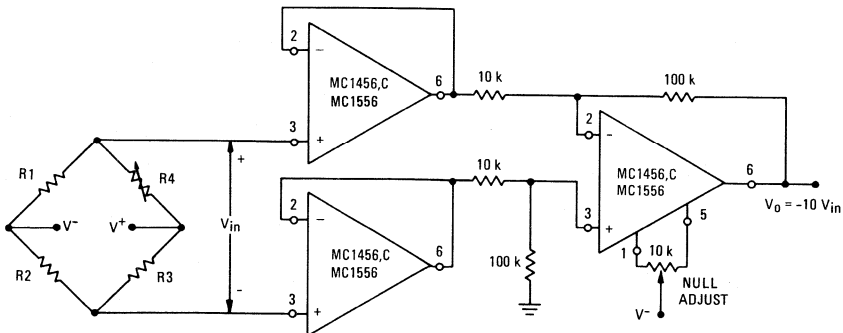
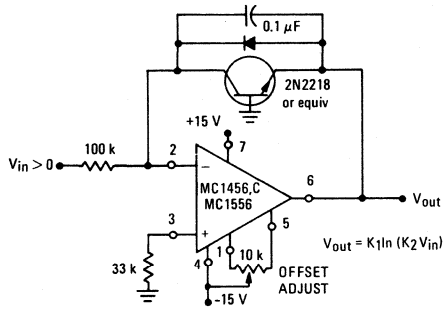


FIGURE 15 – HIGH IMPEDANCE BRIDGE AMPLIFIER



TYPICAL APPLICATIONS (continued)

FIGURE 16 – LOGARITHMIC AMPLIFIER



See Application Note AN-261 for further detail.

FIGURE 17 – VOLTAGE OFFSET NULL CIRCUIT

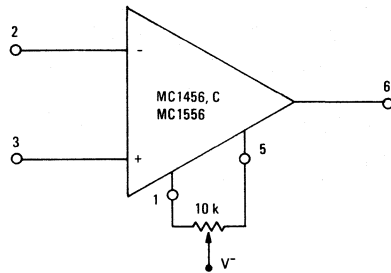
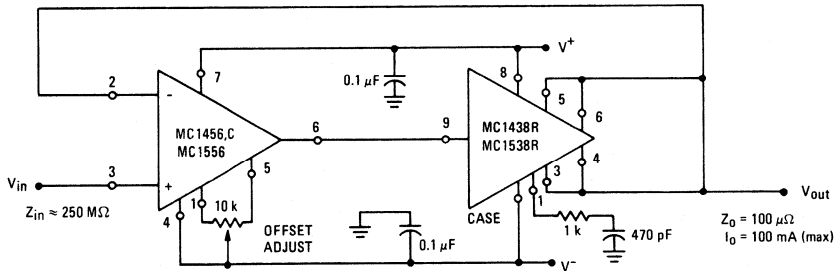


FIGURE 18 – HIGH INPUT IMPEDANCE, HIGH OUTPUT CURRENT VOLTAGE FOLLOWER



MC1558
MC1458
MC1458C

DUAL MC1741
INTERNALLY COMPENSATED, HIGH PERFORMANCE
MONOLITHIC OPERATIONAL AMPLIFIER

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

(DUAL MC1741)
DUAL
OPERATIONAL AMPLIFIER

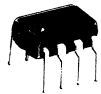
MONOLITHIC SILICON
INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 601
TO-99



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
MC1458,C (only)



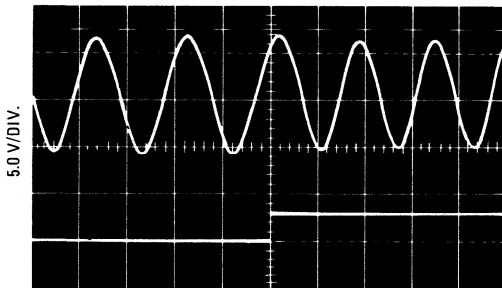
P2 SUFFIX
PLASTIC PACKAGE
CASE 605
MC1458,C (only)



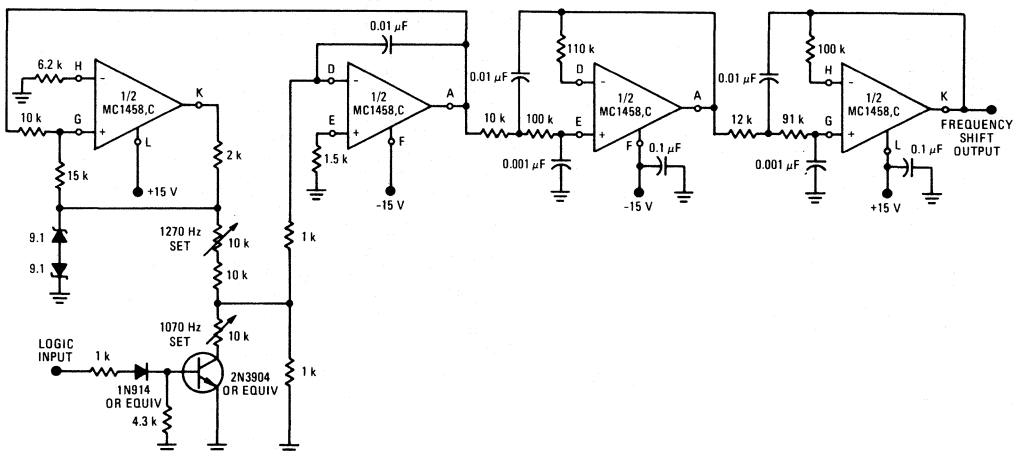
PIN CONNECTIONS

| Schematic | A | B | C | D | E | F | G | H | I | J | K | L |
|-----------------|---|---|---|---|---|---|---|---|----|----|----|----|
| G & P1 Packages | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| L & P2 Packages | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 14 |

FIGURE 1 – TYPICAL FREQUENCY-SHIFT
KEYER TONE GENERATOR



0.5 ms/DIV.



See Packaging Information Section for outline dimensions.

See current MCCC1558/1458 data sheet for flip-chip information.

MC1558, MC1458, MC1458C (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | MC1558 | MC1458,C | Unit |
|--|----------------------------------|-------------|-------------|-------|
| Power Supply Voltage | V ⁺ V ⁻ | +22 -22 | +18 -18 | Vdc |
| Differential Input Signal ① | V _{in} | ±30 | | Volts |
| Common-Mode Input Swing ② | CMV _{in} | ±15 | | Volts |
| Output Short Circuit Duration | t _S | Continuous | | |
| Power Dissipation (Package Limitation) | P _D | | | |
| Metal Can Derate above T _A = +25°C | | 680 | | mW |
| Plastic Dual In-Line Packages Derate above T _A = +25°C | | 4.6 | | mW/°C |
| Ceramic Dual In-Line Package Derate above T _A = +25°C | | 625 | | mW |
| | | 5.0 | | mW/°C |
| | | 750 | | mW/°C |
| | | 6.0 | | mW/°C |
| Operating Temperature Range | T _A | -55 to +125 | 0 to +75 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V⁺ = +15 Vdc, V⁻ = -15 Vdc, T_A = +25°C unless otherwise noted)

| Characteristics | Symbol | MC1558 | | | MC1458 | | | MC1458C | | | Unit |
|---|--|------------------|------------|-----|------------------|------------|-----|-------------|------------|-----|------------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current T _A = +25°C T _A = T _{low} to T _{high} ③ | I _b | — | 0.2 | 0.5 | — | 0.2 | 0.5 | — | 0.2 | 0.7 | μA _{dc} |
| Input Offset Current T _A = +25°C T _A = T _{low} to T _{high} | I _{io} | — | 0.03 | 0.2 | — | 0.03 | 0.2 | — | 0.03 | 0.3 | μA _{dc} |
| Input Offset Voltage (R _S ≤ 10 k Ω) T _A = +25°C T _A = T _{low} to T _{high} | V _{io} | — | 1.0 | 5.0 | — | 2.0 | 6.0 | — | 2.0 | 10 | mV _{dc} |
| Differential Input Impedance (Open-Loop, f = 20 Hz) | | | | | | | | | | | |
| Parallel Input Resistance | R _p | 0.3 | 1.0 | — | 0.3 | 1.0 | — | — | 1.0 | — | Megohm |
| Parallel Input Capacitance | C _p | — | 6.0 | — | — | 6.0 | — | — | 6.0 | — | pF |
| Common-Mode Input Impedance (f = 20 Hz) | Z _(in) | — | 200 | — | — | 200 | — | — | 200 | — | Megohms |
| Common-Mode Input Voltage Swing | CMV _{in} | ±12 | ±13 | — | ±12 | ±13 | — | ±11 | ±13 | — | V _{pk} |
| Equivalent Input Noise Voltage (A _V = 100, R _S = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz) | e _n | — | 45 | — | — | 45 | — | — | 45 | — | nV/(Hz) ^{1/2} |
| Common-Mode Rejection Ratio (f = 100 Hz) | CMR _{rej} | 70 | 90 | — | 70 | 90 | — | 60 | 90 | — | dB |
| Open-Loop Voltage Gain T _A = +25°C T _A = T _{low} to T _{high} } (V _O = ±10 V, R _L = 2.0 k ohms) T _A = +25°C T _A = T _{low} to T _{high} } (V _O = ±10 V, R _L = 10 k ohms) | A _{VOL} | 50,000 25,000 | 200,000 | — | 20,000 15,000 | 100,000 | — | — | — | — | V/V |
| Power Bandwidth (A _V = 1, R _L = 2.0 k ohms, THD ≤ 5%, V _O = 20 V p-p) | P _{BW} | — | 14 | — | — | 14 | — | — | 14 | — | kHz |
| Unity Gain Crossover Frequency (open-loop) | f _c | — | 1.1 | — | — | 1.1 | — | — | 1.1 | — | MHz |
| Phase Margin (open-loop, unity gain) | | — | 65 | — | — | 65 | — | — | 65 | — | degrees |
| Gain Margin | | — | 11 | — | — | 11 | — | — | 11 | — | dB |
| Slew Rate (Unity Gain) | dV _{out} /dt | — | 0.8 | — | — | 0.8 | — | — | 0.8 | — | V/μs |
| Output Impedance (f = 20 Hz) | Z _{out} | — | 75 | — | — | 75 | — | — | 75 | — | ohms |
| Short-Circuit Output Current | I _{SC} | — | 20 | — | — | 20 | — | — | 20 | — | mA _{dc} |
| Output Voltage Swing (R _L = 10 k ohms) R _L = 2 k ohms (T _A = T _{low} to T _{high}) | V _o | ±12 ±10 | ±14 ±13 | — | ±12 ±10 | ±14 ±13 | — | ±11 ±9.0 | ±14 ±13 | — | V _{pk} |
| Average Temperature Coefficient of Input Offset Voltage (R _S = 50 ohms, T _A = T _{low} to T _{high}) | TCV _{io} | — | 15 | — | — | 15 | — | — | 15 | — | μV/°C |
| Power Supply Sensitivity V ⁻ = constant, R _S ≤ 10 k ohms V ⁺ = constant, R _S ≤ 10 k ohms | S ⁺ S ⁻ | — | 30 30 | 150 | — | 30 30 | 150 | — | 30 30 | — | μV/V |
| Power Supply Current | I _D ⁺ I _D ⁻ | — | 2.3 2.3 | 5.0 | — | 2.3 2.3 | 5.6 | — | 2.3 2.3 | 8.0 | mA _{dc} |
| DC Quiescent Power Dissipation (V _O = 0) | P _D | — | 70 | 150 | — | 70 | 170 | — | 70 | 240 | mW |

① For supply voltages of less than ±15 V, the maximum differential input voltage is equal to ±(V⁺ + |V⁻|).

② For supply voltages of less than ±15 V, the maximum input voltage is equal to the supply voltage (+V⁺, -|V⁻|).

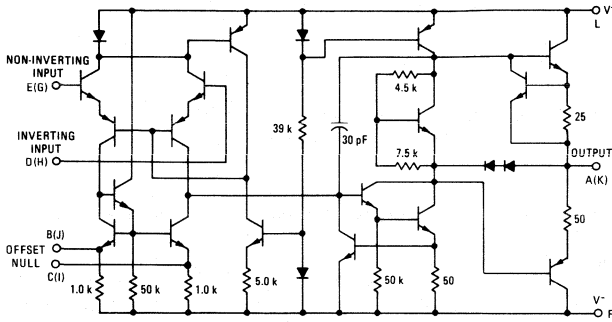
③ T_{low}: 0°C for MC1458,C

-55°C for MC1558

+75°C for MC1458,C

+125°C for MC1558

FIGURE 2 – CIRCUIT SCHEMATIC

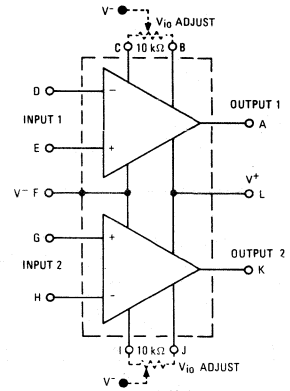


The letters without parenthesis represent the pin numbers for 1/2 of the dual circuit, letters in parenthesis represent the pin numbers for the other half.

PIN CONNECTIONS

| Schematic | A | B | C | D | E | F | G | H | I | J | K | L |
|-----------------|---|---|---|---|---|---|---|---|----|----|----|----|
| G & P1 Packages | 1 | - | - | 2 | 3 | 4 | 5 | 6 | - | - | 7 | 8 |
| L & P2 Packages | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 14 |

FIGURE 3 – EQUIVALENT CIRCUIT WITH OFFSET ADJUST



Offset Adjust is available only in 14-pin packaged devices.

TYPICAL CHARACTERISTICS

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus POWER-SUPPLY VOLTAGE

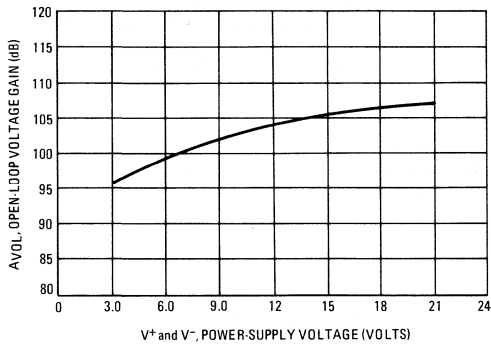


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

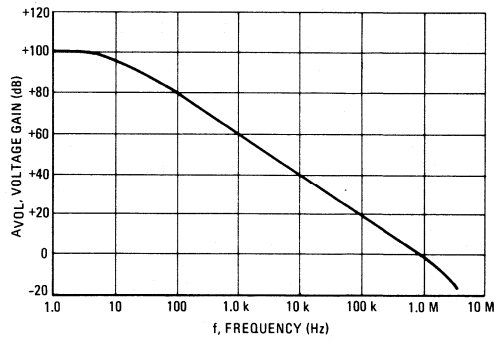


FIGURE 6 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

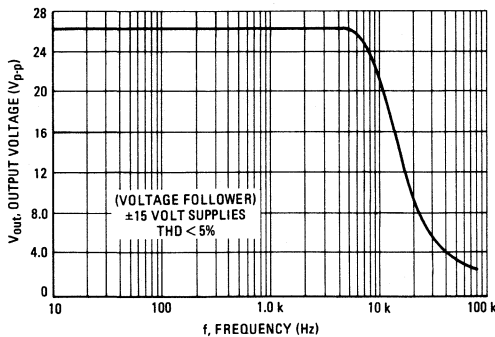
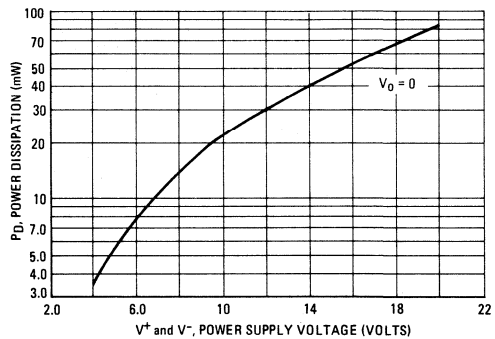


FIGURE 7 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

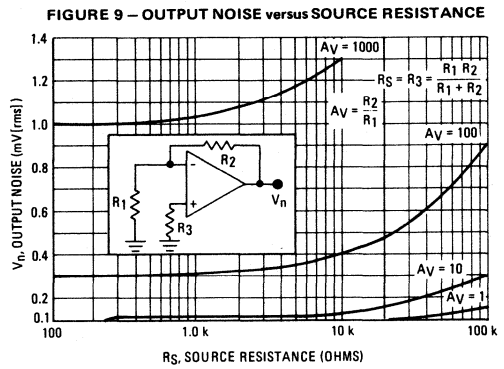
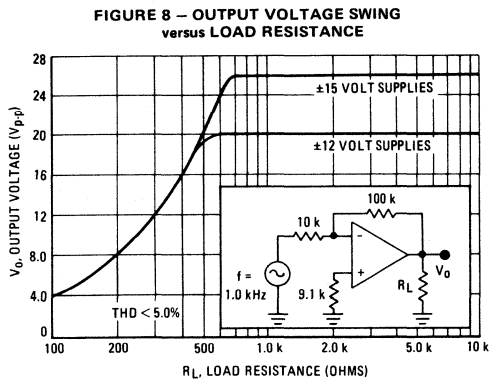
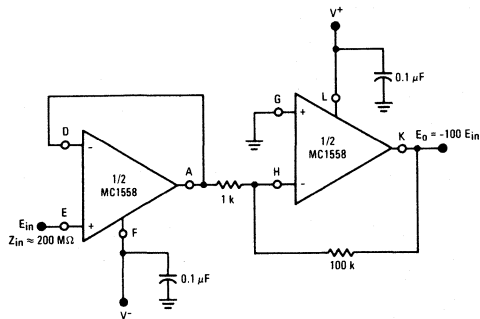


FIGURE 10 – HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER



MC1560, MC1561 MC1460, MC1461

POSITIVE VOLTAGE REGULATORS

MONOLITHIC VOLTAGE REGULATOR

... designed to deliver continuous load current up to 500 mA without use of an external power transistor.

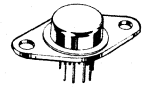
- Electronic "Shut-Down" Control and Short-Circuit Protection
- Excellent Load Regulation (Low Output Impedance = 20 milliohms typ from dc to 100 kHz)
- High Power Capability: To 17.5 Watts
- Excellent Transient Response and Temperature Stability
- High Ripple Rejection = 0.002 %/V typ
- Single External Transistor Can Boost Load Current to Greater than 10 Amperes
- Input Voltages to 40 Volts (MC1561)

POSITIVE-POWER-SUPPLY VOLTAGE REGULATOR INTEGRATED CIRCUIT EPITAXIAL PASSIVATED



Pin 10 electrically connected to case through substrate.

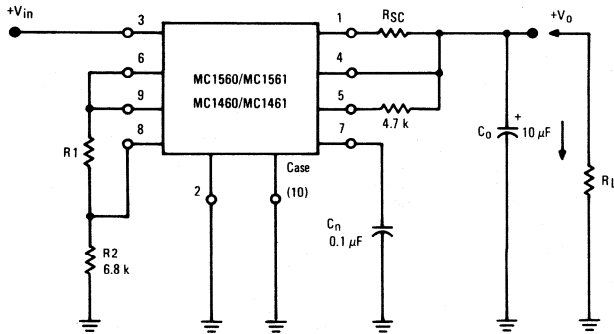
**G SUFFIX
METAL PACKAGE
CASE 602A**



Case is ground terminal

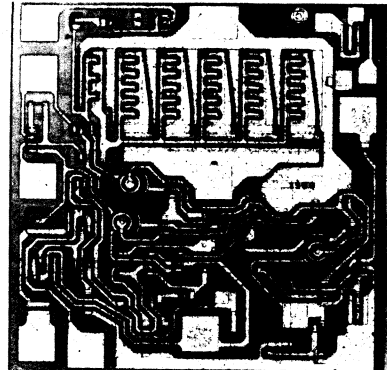
**R SUFFIX
METAL PACKAGE
CASE 614**

TYPICAL APPLICATION

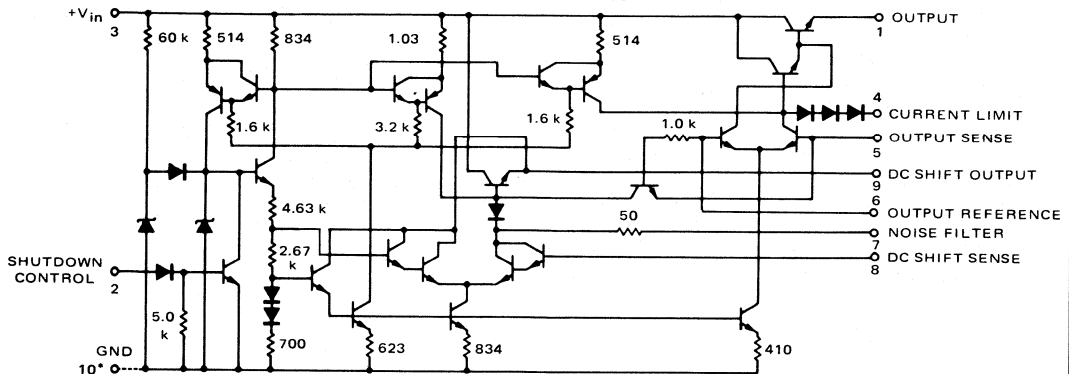


Select R1 to give desired V_O :

$$R1 \approx (2 V_O - 7.0) \text{ k}\Omega$$



CIRCUIT SCHEMATIC



**"G" package - pin 10 is ground, "R" package - case is ground.

See Packaging Information Section for outline dimensions.

MC1560, MC1561, MC1460, MC1461 (continued)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (Load Current = 100 mA for "R" Package device, unless otherwise noted)
= 10 mA for "G" Package device, unless otherwise noted)

| Characteristic Definitions (linear operation) | Characteristic | Symbol | Min | Typ | Max | Units |
|---|--|----------------|--------------------------|----------------------------|--------------------------|---------------------|
| <p>($R_{SC} = 2.7$ ohms unless otherwise noted)</p> <p>CONNECTION FOR $V_O \geq 3.5$ V</p> <p>Select R1 to give desired V_O: $R_1 \approx (2 V_O - 7) \text{ k}\Omega$</p> | <p>Input Voltage (See Note 1) (0 to $+75^\circ\text{C}$) (-55°C to $+125^\circ\text{C}$)</p> <p>MC1460, MC1560 MC1461 MC1561</p> | V_{in} | 9.0 8.5 9.0 8.5 | — — — — | 20 20 35 40 | Vdc |
| <p>CONNECTION FOR $V_O \leq 3.5$ V</p> <p>Select R2 to give desired V_O: $R_2 \approx (2 V_O) \text{ k}\Omega$ Select R1: $R_1 \approx (7.0 \text{ k}\Omega - R_2) \text{ k}\Omega$</p> | <p>Output Voltage Range</p> <p>MC1460, MC1560 MC1461 MC1561</p> | V_O | 2.5 2.5 2.5 | — — — | 17 32 37 | Vdc |
| | <p>Reference Voltage ($V_{in} = 15$ V) (Pin 8 to ground)</p> | V_{ref} | 3.2 | 3.5 | 3.8 | Vdc |
| | <p>Minimum Input-Output Voltage Differential (See Note 2) ($R_{SC} = 0$)</p> <p>MC1460, MC1461 MC1560, MC1561</p> | $V_{in} - V_O$ | — — | 2.1 2.1 | 3.0 2.7 | Vdc |
| | <p>Bias Current ($V_{in} = 15$ V) ($I_L = 1.0$ mA dc, $R_2 = 6.8 \text{ k}\Omega$, $I_B = I_{in} - I_L$)</p> <p>MC1460, MC1461 MC1560, MC1561</p> | I_B | — — | 5.0 4.0 | 12 9.0 | mAdc |
| | <p>Output Noise ($C_n = 0.1 \mu\text{F}$, $f = 10$ Hz to 5.0 MHz)</p> | v_n | — | 0.150 | — | mV (rms) |
| | <p>Temperature Coefficient of Output Voltage (See Note 3) (0 to $+75^\circ\text{C}$) (-55° to $+125^\circ\text{C}$)</p> <p>MC1460, MC1461 MC1560, MC1561</p> | TCV_O | — — | ± 0.002 ± 0.002 | — — | %/ $^\circ\text{C}$ |
| | <p>Operating Load Current Range* ($R_{SC} \leq 0.3$ ohms) R Package ($R_{SC} \leq 2.0$ ohms) G Package</p> | I_L | 1.0 1.0 | — — | 500 200 | mAdc |
| <p>$+V_{in} = 17$ Vdc $V_{in} = 1.0$ vrms $f = 1.0$ kHz</p> | <p>Input Regulation (% change in output voltage per 1-volt change in input voltage)</p> <p>MC1460, MC1461 MC1560, MC1561</p> <p>$Reg_{in} = \frac{v_o \text{ (rms)} (100)}{V_{in} \text{ (rms)}} V_O$ (See Note 4)</p> | Reg_{in} | — — | 0.003 0.002 | 0.030 0.015 | %/ V_O |
| <p>$+15$ V</p> | <p>Load Regulation</p> <p>$T_J = \text{Constant}$ ($1.0 \text{ mA} \leq I_L \leq 20 \text{ mA}$)</p> <p>MC1460 MC1560 MC1461 MC1561</p> <p>$T_C = 25^\circ\text{C}$ (See Note 5) ($1.0 \text{ mA} \leq I_L \leq 50 \text{ mA}$)</p> <p>R Package G Package</p> | Reg_{load} | — — — — | 0.5 0.3 0.7 0.4 | 2.0 1.2 2.4 1.6 | mV |
| <p>$+V_{in}$</p> | <p>Output Impedance (See Note 6) ($R_{SC} = 1.0$ ohms, $f = 10$ kHz, $V_{in} = 14$ Vdc)</p> <p>MC1460 MC1560 MC1461 MC1561</p> <p>($I_L = 25$ mA dc for G Package)</p> | Z_{out} | — — — — | 25 15 35 20 | 100 60 120 80 | milli-ohms |
| <p>$+V_{in}$</p> | <p>Shutdown Current ($V_{in} = 20$ Vdc)</p> <p>MC1460 MC1560 MC1461 MC1561</p> <p>($V_{in} = 35$ Vdc)</p> <p>$R_3 \approx \frac{V_{in} - 1.4}{1.0 \text{ mA}}$</p> | I_{sd} | — — — — | 80 20 140 70 | 300 50 500 150 | μAdc |

*Operating Load Current is also limited by dc Safe Operating Area (see Figures 15A and 15B). Care must be taken not to exceed the dc Safe Operating Area at any time.

MC1560, MC1561, MC1460, MC1461 (continued)

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

| Rating | Symbol | Value | | Unit |
|---|-----------------------------------|----------------|-----------|-------|
| Input Voltage MC1460, MC1560 MC1461 MC1561 | V _{in} | 20 35 40 | | Vdc |
| Load Current | I _L | G Package | R Package | mA |
| | | 250 | 600 | |
| Current, Pin 2 | I _{pin 2} | 10 | 10 | mA |
| Current, Pin 9 | I _{pin 9} | 5.0 | 5.0 | |
| Power Dissipation and Thermal Characteristics | | | | |
| T _A = 25°C | P _D | 0.68 | 3.0 | Watts |
| Derate above T _A = 25°C | 1/θ _{JA} | 5.44 | 24 | mW/°C |
| Thermal Resistance, Junction to Air | θ _{JA} | 184 | 41.6 | °C/W |
| T _C = 25°C | P _D | 1.8 | 17.5* | Watts |
| Derate above T _C = 25°C | 1/θ _{JC} | 14.4 | 140 | mW/°C |
| Thermal Resistance, Junction to Case | θ _{JC} | 69.4 | 7.15 | °C/W |
| Operating and Storage Junction Temperature Range | T _J , T _{stg} | -65 to +150 | | °C |

*The MC1460R and MC1560R are limited to 12 watts maximum by the voltage and current maximum ratings.

OPERATING TEMPERATURE RANGE

| Ambient Temperature | T _A | °C | |
|----------------------------------|----------------|-------------------------|--|
| MC1460, MC1461 MC1560, MC1561 | | 0 to +75 -55 to +125 | |

Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode. For output voltages greater than approximately 5.5 Vdc the minimum "total instantaneous input voltage" must increase to the extent that it will always exceed the output voltage by at least the "input-output voltage differential".

Note 2. This parameter states that the MC1560/1561 and MC1460/1461 will regulate properly with the input-output voltage differential (V_{in} - V_O) as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with (V_{in} - V_O) as low as 2.1 Vdc as shown in the typical column.

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$\text{MC1560, MC1561 } TC_{V_O} = \frac{\pm (V_{O \text{ max}} - V_{O \text{ min}})(100)}{2 (180^\circ\text{C})(V_O @ 25^\circ\text{C})} = \%/^\circ\text{C}$$

$$\text{MC1460, MC1461 } TC_{V_O} = \frac{\pm (V_{O \text{ max}} - V_{O \text{ min}})(100)}{2 (75^\circ\text{C})(V_O @ 25^\circ\text{C})} = \%/^\circ\text{C}$$

The output-voltage adjusting resistors (R1 and R2) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. The input signal can be introduced by use of a transformer which will allow the output of an audio oscillator to be coupled in series with the dc input to the regulator. (The large ac input impedance of the regulator will not load the oscillator.) A 24 V, 1.0 ampere filament transformer with the audio oscillator connected to the 110 V primary winding is satisfactory for this test. V_{in} ≈ 1.0 V (rms).

Note 5. Load regulation is specified for small (≤ +17°C) changes in junction temperature. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{V_{O|I_L = 1.0 \text{ mA}} - V_{O|I_L = 50 \text{ mA}}}{V_{O|I_L = 1.0 \text{ mA}}} \times 100$$

Note 6. The resulting low level output signal (v_O) will require the use of a tuned voltmeter to obtain a reading. Special care should be used to insure that the measurement technique does not include connection resistance, wire resistance, and wire lead inductance (i.e., measure close to the case). Note that No. 22 AWG hook-up wire has approximately 4.0 milliohms/in. dc resistance and an inductive reactance of approximately 10 milliohms/in. at 100 kHz. Avoid use of alligator clips or banana plug-jack combination.

GENERAL OPERATING INFORMATION

There is a general tendency to consider a voltage regulator as simply a dc circuit and to prepare breadboard construction accordingly. The excellent high-frequency performance and fast response capability of this integrated-circuit regulator, however, makes extra breadboarding care worthwhile when compared with the limited performance achieved in other regulators when low-frequency transistors are used in the feedback amplifier. Due to the use of VHF transistors in the integrated circuit, some VHF care (short, well-dressed leads) must be exercised in the construction and wiring of circuits ("printed-circuit" boards provide an excellent component interconnection technique).

The circuit must be grounded by a low-inductance connection to the case of the "R" package, or to pin 10 of the "G" package.

A series 4.7-kΩ resistor at Pin 5 (Figure 1) will eliminate any VHF instability problems which may result from lead lengths longer than a few inches at the regulator output. The resistor body should be as close to Pin 5 as physically possible (<1/2 inch) although the length of the lead to the load is not critical. If temperature stability is of major concern, a 4.7-kΩ resistor should also be placed in series with Pin 6 in order to cancel any drift due to bias current changes.

If long input leads are used, it may be necessary to bypass Pin 3 with a 0.1- μ F capacitor (to ground).

The "Shut-Down Control", Pin 2, can be actuated for all possible output voltages and any values of C_O and C_N with no damage to the circuit. The standard logic levels of RTL, DTL, or TTL can be used (see Figure 20). This control can be used to eliminate power consumption by circuit loads which can be put in a "standby" mode, as an ac and dc "squelch" control for communications circuits, and as a dissipation control to protect the regulator under sustained output short-circuiting (see Figures 21 and 25). As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the IC chip, a fixed dc voltage at Pin 2 will cause automatic shut-down for high junction temperatures (see Figure 23, a and b). This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels.

Due to the small value of input current at Pin 8, the external resistors, R1 and R2, can be selected with little regard to their par-

allel resistance. Further, no match to a diffused-resistor temperature coefficient is required; but R1 and R2 should have the same temperature coefficient to keep their ratio independent of temperature.

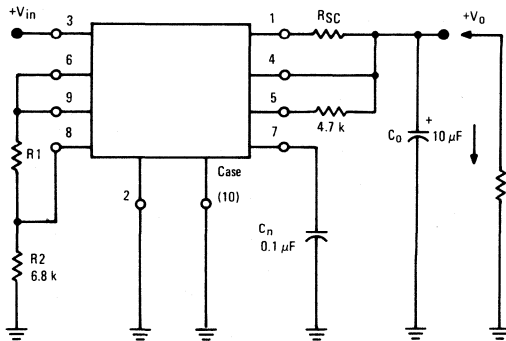
C_N values in excess of 0.1 μ F are rarely needed to reduce noise. In cases where more output noise can be tolerated, a smaller capacitor can be used (C_N min. \approx 0.001 μ F).

The connection to Pin 5 can be made by a separate lead directly to the load. Thus "remote sensing" can be achieved and undesired impedances (including that of a milliammeter used to measure I_L) can be greatly reduced in their effect on Z_{OUT} . A 10-ohm resistor placed from pin 1 to pin 5 (close to the IC) will eliminate undesirable lead-inductance effects.

Short-circuit current-limiting is achieved by selecting a value for R_{SC} which will threshold the internal diode string when the desired maximum load current flows (see Figure 5). If the device dissipation and dc safe area limits (Figure 15) are not exceeded, it can be continuously short-circuited at the output without damage.

TYPICAL CONNECTIONS

FIGURE 1 - CONNECTION FOR $V_O \geq 3.5$ V



Select R1 to give desired V_O : $R1 \approx (2 V_O - 7.0) \text{ k}\Omega$

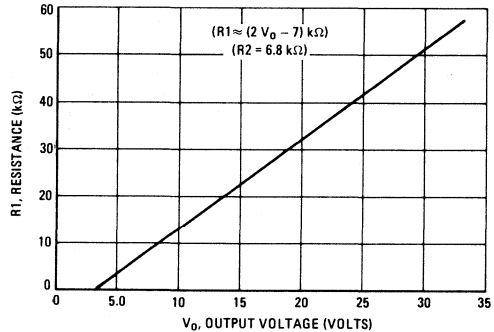
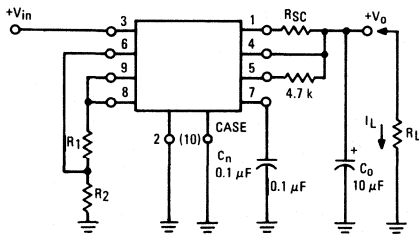
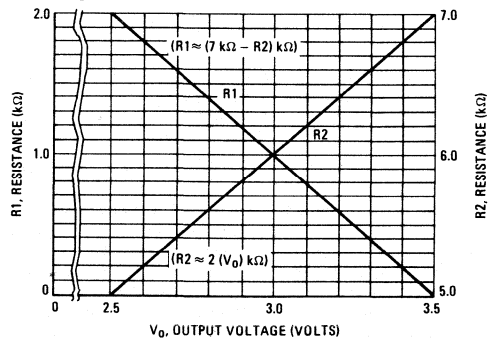


FIGURE 2 - CONNECTIONS FOR $V_O \leq +3.5$ V



Select R2 to give desired V_O :
 $R2 \approx (2 V_O) \text{ k}\Omega$
 Select R1:
 $R1 \approx 7.0 \text{ k}\Omega - R2$



TYPICAL CHARACTERISTICS

Unless otherwise stated: $C_n = 0.1 \mu\text{F}$, $C_o = 10 \mu\text{F}$, $V_o \text{ nom} = +5.0 \text{ Vdc}$, $V_{in} \text{ nom} = +9.0 \text{ Vdc}$, $T_C = +25^\circ\text{C}$, $I_L > 200 \text{ mA}$ for "R" Package only.

FIGURE 3 – INPUT TRANSIENT RESPONSE

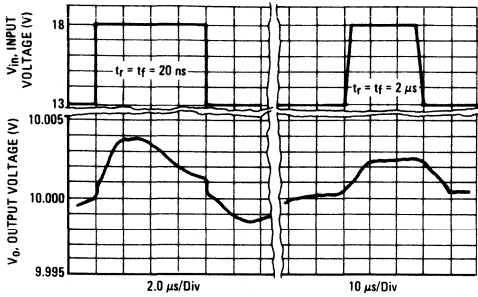


FIGURE 4 – LOAD TRANSIENT RESPONSE

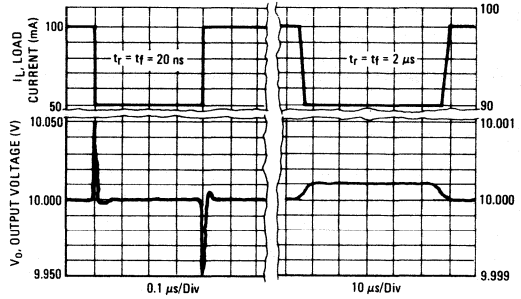


FIGURE 5 – SHORT-CIRCUIT CURRENT versus R_{SC}

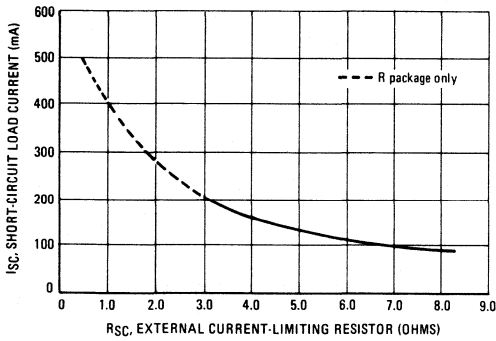


FIGURE 6 – CURRENT-LIMITING CHARACTERISTICS

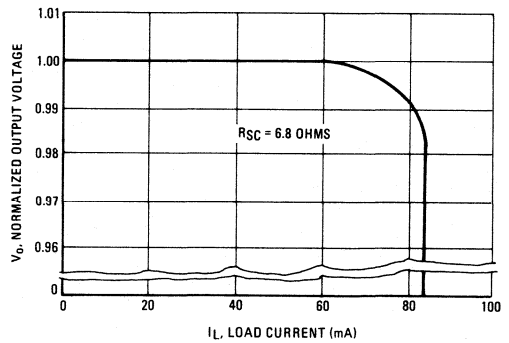


FIGURE 7 – FREQUENCY-DEPENDENCE OF OUTPUT IMPEDANCE

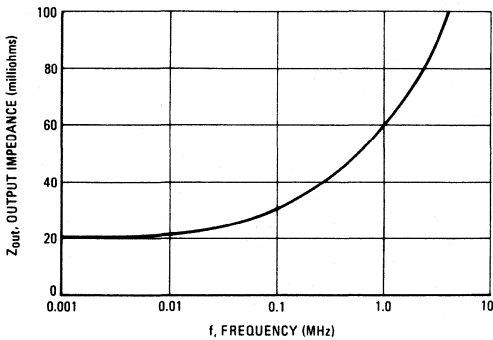
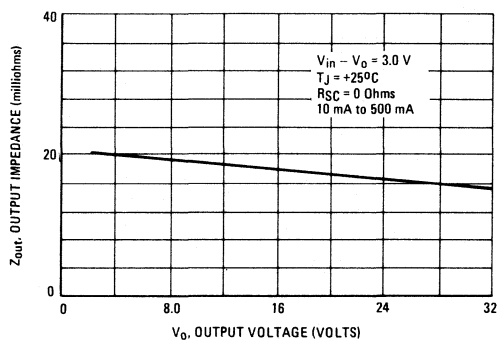


FIGURE 8 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE



TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated: $C_n = 0.1 \mu\text{F}$, $C_o = 10 \mu\text{F}$, $V_o \text{ nom} = +5.0 \text{ Vdc}$, $V_{in} \text{ nom} = +9.0 \text{ Vdc}$, $T_c = +25^\circ\text{C}$, $I_L > 200 \text{ mA}$ for "R" Package only.

FIGURE 9 – OUTPUT IMPEDANCE versus R_{SC}

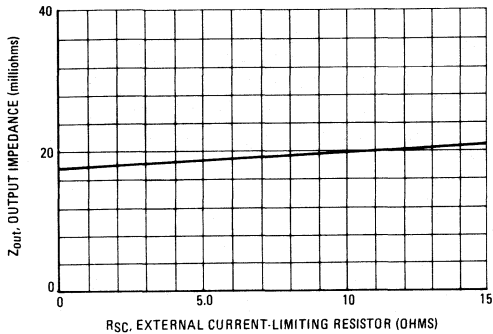


FIGURE 10 – FREQUENCY-DEPENDENCE OF INPUT REGULATION

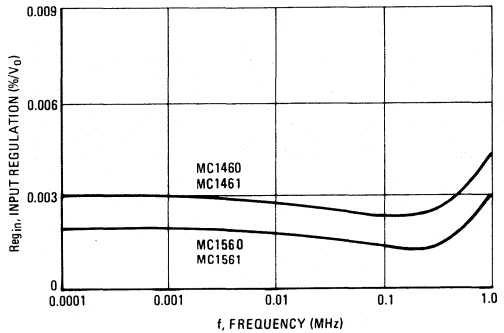


FIGURE 11 – BIAS CURRENT versus INPUT VOLTAGE

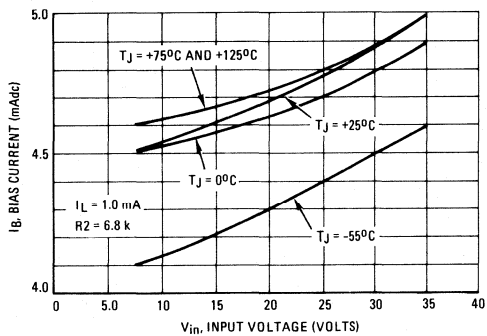


FIGURE 12 – EFFECT OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

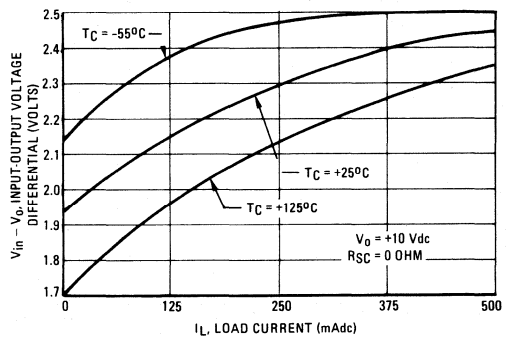


FIGURE 13 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

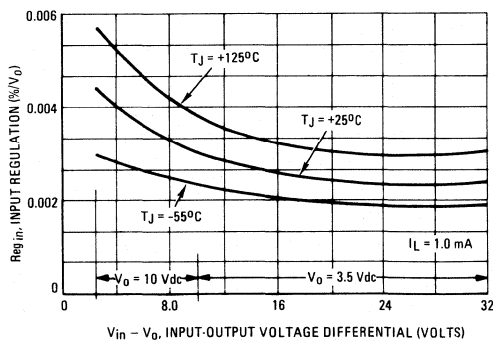
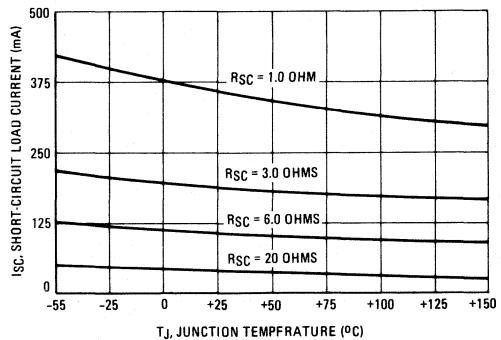


FIGURE 14 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT



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TYPICAL CHARACTERISTICS (continued)

FIGURE 15a - DC SAFE OPERATING AREA ("G" PACKAGE)

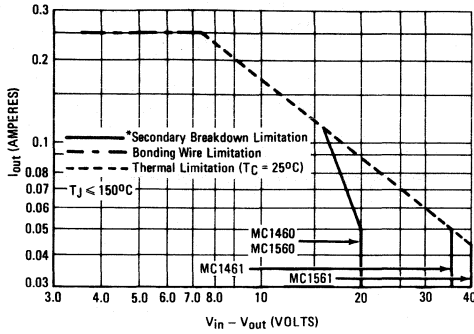
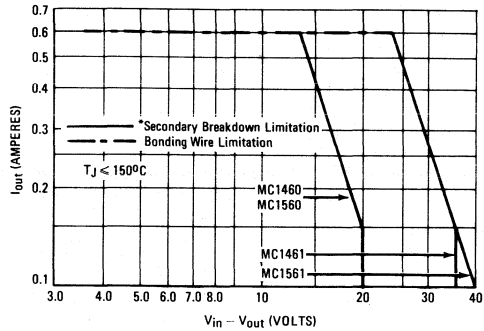


FIGURE 15b - DC SAFE OPERATING AREA ("R" PACKAGE)



*See Application Note AN-415 for an explanation of safe area and second breakdown.

TYPICAL APPLICATIONS

FIGURE 16 - A LABORATORY SUPPLY, 0 TO 25 V

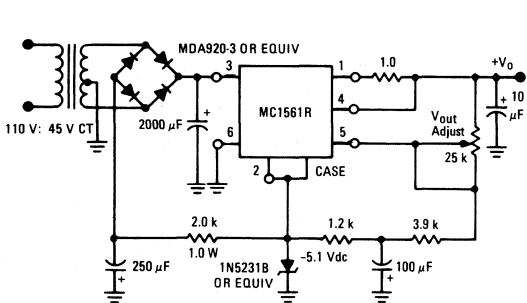


FIGURE 17 - PROVIDING TWO REGULATED OUTPUT VOLTAGES

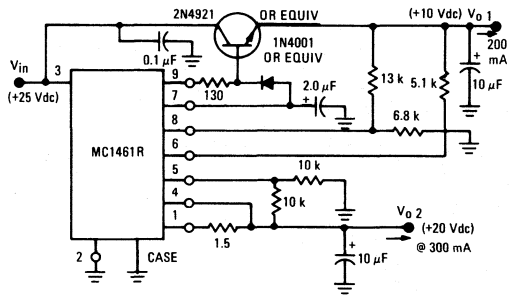
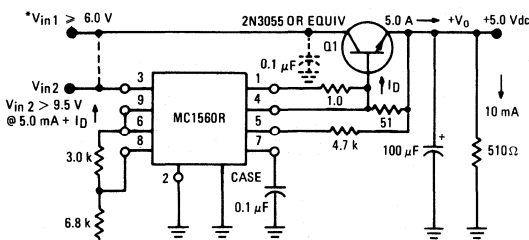
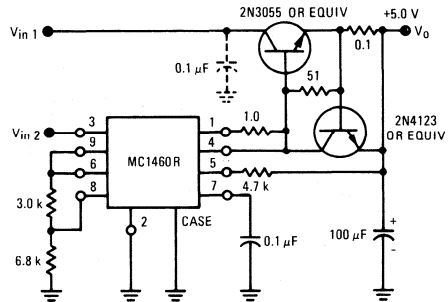


FIGURE 18 - NPN CURRENT BOOST CIRCUITS



*For ripple reduction or increased efficiency at low output voltages, the collector of Q1 can tie to a separate low-voltage supply as shown.



TYPICAL APPLICATIONS (continued)

FIGURE 19 — PNP CURRENT BOOST CIRCUIT

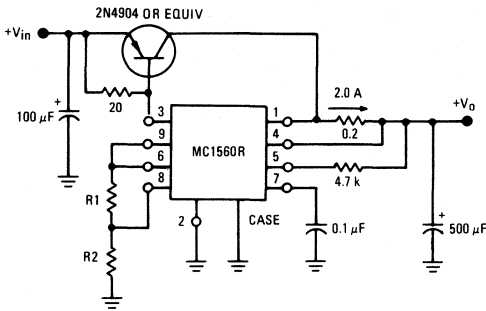


FIGURE 20 — ELECTRONIC SHUT-DOWN USING A MDTL GATE

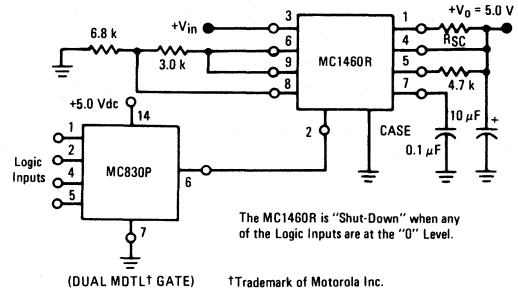


FIGURE 21 — AUTOMATIC LATCH INTO SHUT-DOWN WHEN OUTPUT IS SHORT-CIRCUITED WITH MANUAL RE-START

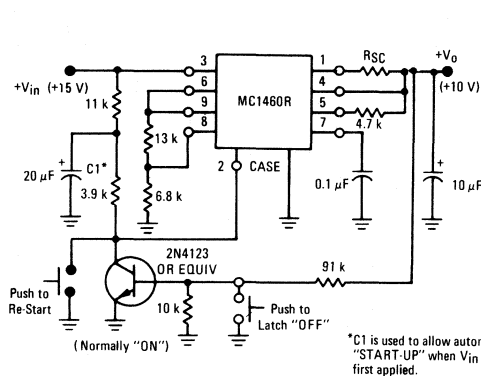


FIGURE 22 — SCR "CROWBAR" OVER VOLTAGE PROTECTION

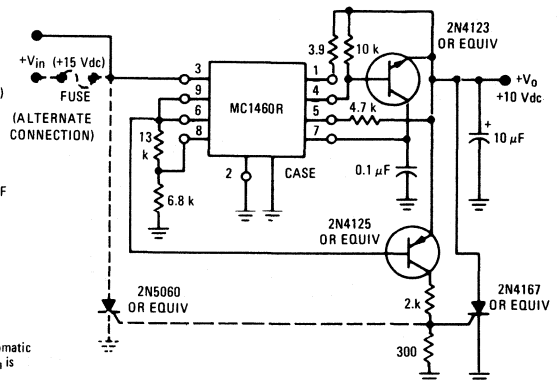
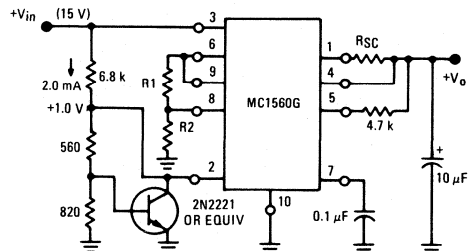
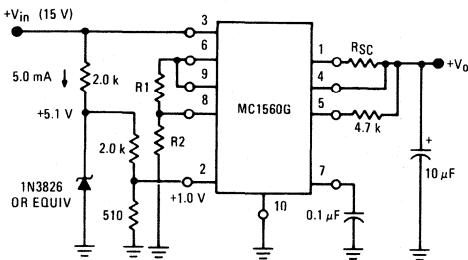


FIGURE 23 — LIMITING MAXIMUM JUNCTION TEMPERATURE

FIGURE a — USING A ZERO TC REFERENCE

FIGURE b — USING A T_A REFERENCE

$$V_{pin 2} \text{ (for shut-down)} \approx 1.38 - 3.4 \times 10^{-3} (T_J - 25^\circ\text{C})$$



TYPICAL APPLICATIONS (continued)

FIGURE 24 – THERMAL SHUTDOWN WHEN USING EXTERNAL PASS TRANSISTOR

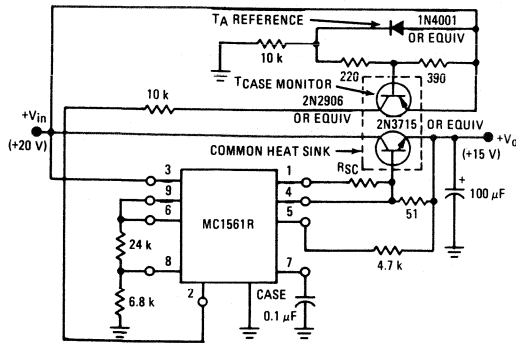


FIGURE 25 – LOW DUTY CYCLE SHORT CIRCUIT PROTECTION WITH AUTOMATIC RESET

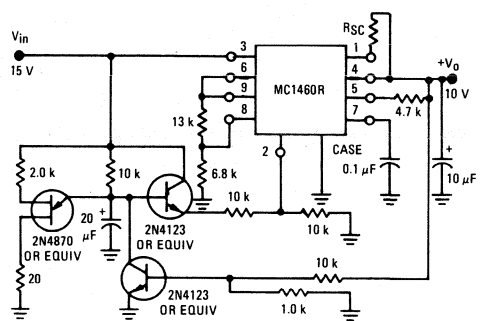


FIGURE 26 – CONNECTION FOR A NEGATIVE OUTPUT VOLTAGE

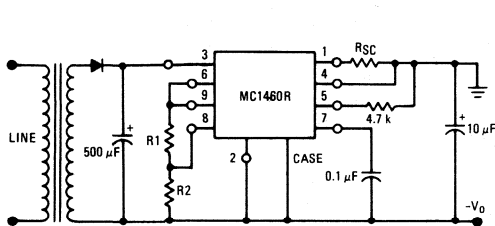


FIGURE 27 – DIGITALLY CONTROLLED 3-TERMINAL NEGATIVE REGULATOR

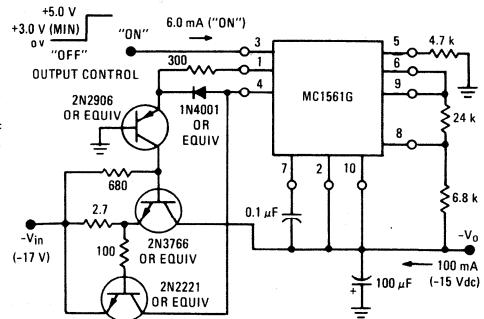
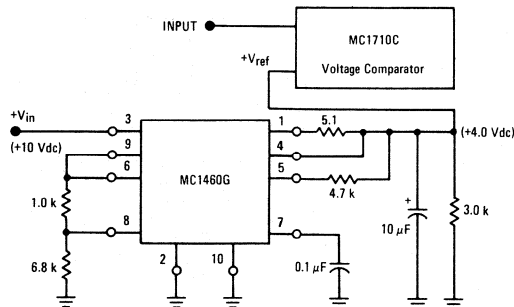


FIGURE 28 – A ZERO TC ADJUSTABLE "ZENER" REFERENCE



GENERAL INFORMATION

Latch-up of these and other regulators can occur if:

1. There are plus and minus voltages available
2. A load exists between V_o^+ and V_o^- (This "common load" may be something inconspicuous - e.g. an operational amplifier. Nearly everyone who uses + and - voltages will have a common load from V^+ to V^-).
3. V_{in}^+ and V_{in}^- are not applied at the same time.

The above conditions result in one of the two outputs becoming reverse-biased which prevents the regulator from turning "on". Latch-up can be prevented by the circuit configurations shown in Figure 29 and 30.

FIGURE 29

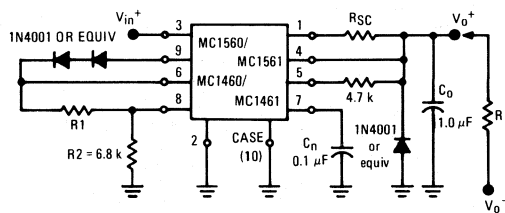
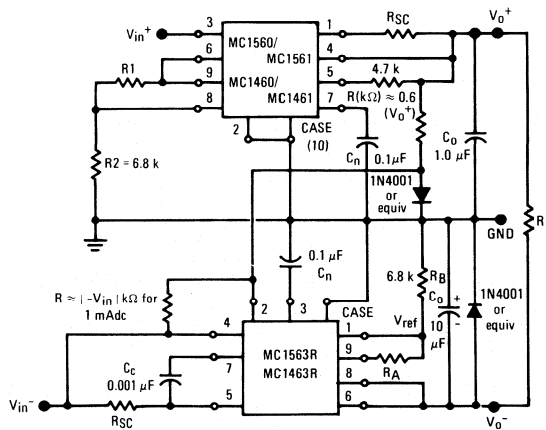


FIGURE 30



7

VOLTAGE REGULATOR CONSTRUCTION
USING THE MC1460, MC1461, MC1560,
MC1561 INTEGRATED CIRCUITS

FIGURE 31 – Regulator Layout Using Power Package For Load Currents Up To 500 mA

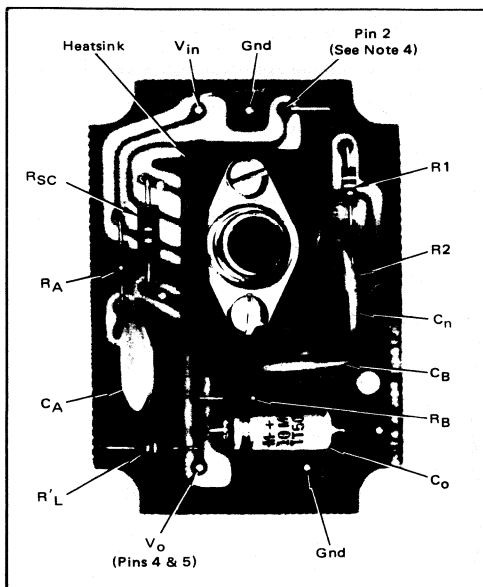
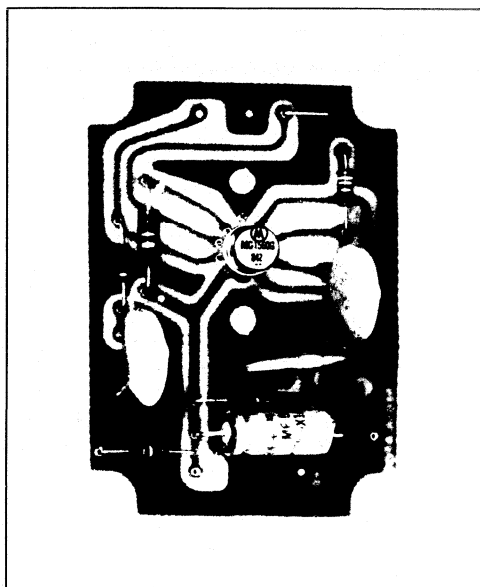


FIGURE 32 – Regulator Layout For Load Currents Up To 200 mA



There is a general tendency to consider a voltage regulator as simply a dc circuit and to prepare circuit layout accordingly. The excellent high-frequency performance and fast response capability of this integrated-circuit regulator, however, makes extra layout care worthwhile. Since short, well-dressed leads must be used, printed-circuit boards provide an excellent component interconnection technique.

The circuit layout, shown in Figure 31 for the "R" or power package IC, applies also to the lower power "G" package circuit shown in Figure 32. The R package circuits will deliver up to 500 mA into a load and the G package, 200 mA.

The circuit schematic, Figure 33, is for output voltages above 3.5 Vdc and the parts list is as follows:

PARTS LIST

| Component | Value | Description |
|-----------|--|--|
| R1 | Select | } 1/4 Watt Carbon – See Note 1 |
| R2 | 6.8 kΩ | |
| RSC | Select | 1/2 Watt Carbon – See Note 2 |
| *RA | 3 Ω | } 1/4 Watt Carbon |
| *RB | 3 Ω | |
| *R'L | Select for current of 1 mA minimum | |
| Co | 10 μF | Sprague 1500 Series, Dickson D10C Series or Equivalent |
| Cn | 0.1 μF | } Ceramic Disc – Centralab DDA104, Sprague TG-P10, or Equivalent |
| *CA | 0.1 μF | |
| *CB | 0.1 μF | |
| *Heatsink | – Thermalloy #6168 – IERC LB 66B1-77U series | |
| *Socket | (Not Shown) Robinson Nugent #0001306 Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1 | |

*Optional Parts, See Note 3 on next page.

VOLTAGE REGULATOR CONSTRUCTION (continued)

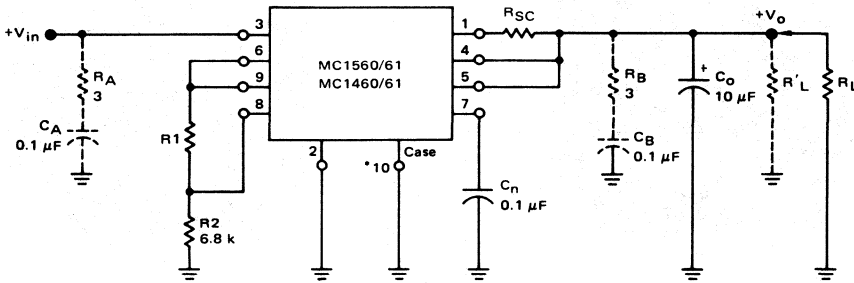
- Note 1. The value of R_1 is approximately $(2 V_O - 7) \text{ k}\Omega$, where V_O is the desired output voltage (3.5 V or greater). Optimum temperature stability can be achieved if R_1 and R_2 have the same temperature coefficient.
- Note 2. R_{SC} is a current sensing resistor for short circuit protection. See Figure 5 for a "Short-Circuit Load Current versus R_{SC} " curve.

- Note 3. In cases where long leads are used at the input or output of the regulator, bypass networks $R_A C_A$ and $R_B C_B$ might be necessary to eliminate parasitic oscillation.

With no load, it is possible for a charge to develop on C_O due to leakage currents. R'_L is recommended to insure a minimum load current of 1 mA.

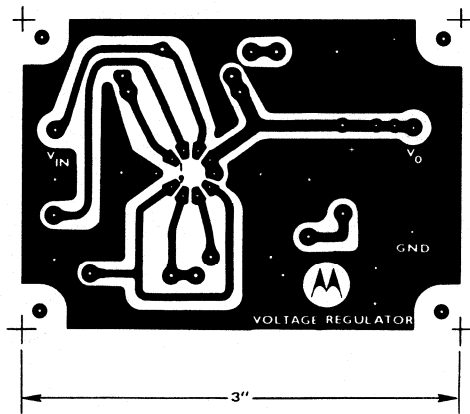
- Note 4. It is recommended that Pin 2 (shut-down control) be grounded when not in use. When used, drive current to Pin 2 must be limited to 10 mA maximum.

FIGURE 33 – Schematic of Complete Regulator Showing Both Necessary and Optional Components



*G-Package Pin 10 is ground, R package Case is ground.

FIGURE 34 – Typical Printed Circuit Board Layout



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**MC1563
MC1463**

Specifications and Applications Information

MONOLITHIC NEGATIVE VOLTAGE REGULATOR

The MC1563/MC1463 is a "three terminal" negative regulator designed to deliver continuous load current up to 500 mA dc and provide a maximum negative input voltage of -40 Vdc. Output current capability can be increased to greater than 10 A dc through use of one or more external transistors.

Specifications and performance of the MC1563/MC1463 Negative Voltage Regulator are nearly identical to the MC1569/MC1469 Positive Voltage Regulator. For systems requiring both a positive and negative power supply, these devices are excellent for use as complementary regulators and offer the advantage of operating with a common input ground.

The MC1563R/MC1463R case can be mounted directly to a grounded heat sink which eliminates the need for an insulator.

- Case is at Ground Potential (R package)
- Electronic "Shutdown" and Short-Circuit Protection
- Low Output Impedance - 20 Milliohms typ
- High Power Capability - 9.0 Watts
- Excellent Temperature Stability - $TCV_0 = \pm 0.002\%/^{\circ}C$ Typ
- High Ripple Rejection - 0.002% typ
- 500 mA Current Capability

**NEGATIVE-POWER-SUPPLY
VOLTAGE REGULATOR
INTEGRATED CIRCUIT
SILICON EPITAXIAL PASSIVATED**

Pin 4 electrically connected to case through substrate.



G SUFFIX
METAL PACKAGE
CASE 602A



R SUFFIX
METAL PACKAGE
CASE 614

FIGURE 1 - TYPICAL CIRCUIT CONNECTION
 $-3.5 \leq V_0 \leq -37$ |Vdc, $1 \leq I_L \leq 500$ mA

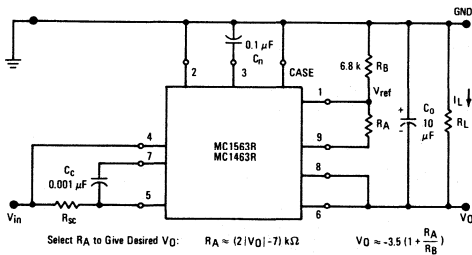
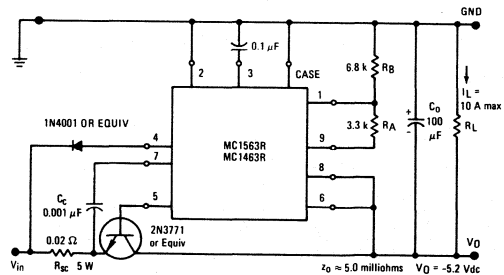
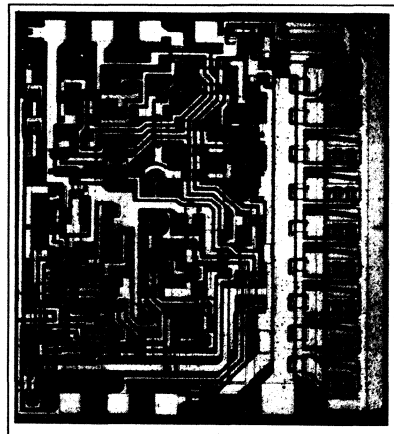
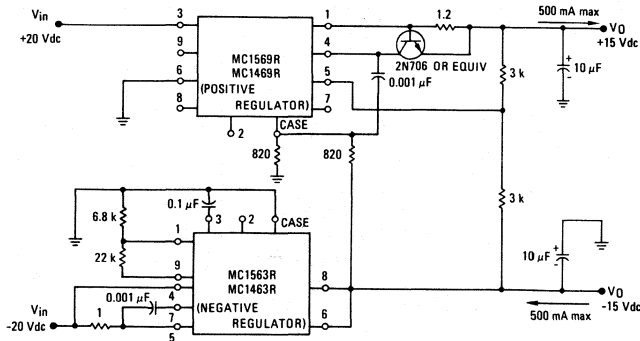


FIGURE 2 - TYPICAL NPN CURRENT BOOST CONNECTION
($V_0 = 5.2$ Vdc, $I_L = 10$ A dc [max])



**FIGURE 3 - ±15 V, ±400 mA COMPLEMENTARY TRACKING
VOLTAGE REGULATOR**



See Packaging Information Section for outline dimensions.

See current MCC1563/1463 data sheet for standard linear chip information.

MC1563, MC1463 (continued)

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit | | | |
|--|--------------------------------------|-------------------------------------|-------------------|------|-------|-------|
| Input Voltage | V _{in} | -35 | Vdc | | | |
| | | -40 | | | | |
| Peak Load Current | I _L pk | G Package | mA | | | |
| | | R Package | | | | |
| Current, Pin 2 | I _{pin 2} | 250 | mA | | | |
| | | 10 | | | | |
| Power Dissipation and Thermal Characteristics | T _A = 25°C | P _D | 0.68 | 2.4 | Watts | |
| | | 1/φ _{JA} | 5.44 | 16 | | mW/°C |
| | T _C = 25°C | Thermal Resistance, Junction to Air | φ _{JA} | 184 | 62 | °C/W |
| | | Derate above T _C = 25°C | 1/φ _{JC} | 14.4 | 61 | mW/°C |
| | Thermal Resistance, Junction to Case | P _D | 1.8 | 9.0 | Watts | |
| | | φ _{JC} | 69.4 | 17 | | °C/W |
| Operating and Storage Junction Temperature Range | T _J , T _{stg} | -65 to +175 | °C | | | |

OPERATING TEMPERATURE RANGE

| Ambient Temperature | Symbol | Value | Unit |
|---------------------|----------------|-------------|------|
| MC1463 MC1563 | T _A | 0 to +75 | °C |
| | | -55 to +125 | |

ELECTRICAL CHARACTERISTICS (I_L = 100 mAdc, T_C = +25°C unless otherwise noted.)

| Characteristic | Fig. | Note | Symbol* | MC1563 | | | MC1463 | | | Unit |
|---|------|------|----------------------------------|--------|--------|-------|--------|--------|-------|------------------|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage (T _A = T _{low} ① to T _{high} ②) | 4 | 1 | V _{in} | -8.5 | - | -40 | -9.0 | - | -35 | Vdc |
| Output Voltage Range | 4 | - | V _O | -3.6 | - | -37 | -3.8 | - | -32 | Vdc |
| Reference Voltage (Pin 1 to Ground) | 4 | - | V _{ref} | -3.4 | -3.5 | -3.6 | -3.2 | -3.5 | -3.8 | Vdc |
| Minimum Input-Output Voltage Differential (R _{sc} = 0) | 4 | 2 | V _{in} - V _O | - | 1.5 | 2.7 | - | 1.5 | 3.0 | Vdc |
| Bias Current (Standby Current) (I _L = 1.0 mAdc, I _B = I _{in} - I _L) | 4 | - | I _B | - | 7.0 | 11 | - | 7.0 | 14 | mAdc |
| Output Noise (C _n = 0.1 μF, f = 10 Hz to 5.0 MHz) | 4 | - | v _n | - | 120 | - | - | 120 | - | μV(rms) |
| Temperature Coefficient of Output Voltage | 4 | 3 | TCV _O | - | ±0.002 | - | - | ±0.002 | - | %/°C |
| Operating Load Current Range (R _{sc} = 0.3 ohm) R Package (R _{sc} = 2.0 ohms) G Package | 4 | - | I _L | 1.0 | - | 500 | 1.0 | - | 500 | mAdc |
| | | | | 1.0 | - | 200 | 1.0 | - | 200 | |
| Input Regulation | 6 | 4 | Reg _{in} | - | 0.002 | 0.015 | - | 0.003 | 0.030 | %/V _O |
| Load Regulation (T _J = Constant [1.0 mA ≤ I _L ≤ 20 mA]) (T _C = +25°C [1.0 mA ≤ I _L ≤ 50 mA]) R Package G Package | 7 | 5 | Reg _L | - | 0.4 | 1.6 | - | 0.7 | 2.4 | mV |
| | | | | - | 0.005 | 0.05 | - | 0.005 | 0.05 | % |
| | | | | - | 0.01 | 0.13 | - | 0.01 | 0.13 | |
| Output Impedance (f = 1.0 kHz) | 8 | - | z _o | - | 20 | 80 | - | 35 | 120 | milliohms |
| Shutdown Current (V _{in} = -35 Vdc) | 9 | - | I _{sd} | - | 7.0 | 15 | - | 14 | 50 | μAdc |

*Symbols conform to JEDEC Bulletin No. 1 where applicable.

① T_{low} = 0°C for MC1463
= -55°C for MC1563

② T_{high} = +75°C for MC1463
= +125°C for MC1563

MC1563, MC1463 (continued)

Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode.

Note 2. This parameter states that the MC1563/MC1463 will regulate properly with the input-output voltage differential $|V_{in} - V_O|$ as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with $|V_{in} - V_O|$ as low as 1.5 Vdc as shown in the typical column.

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min}) (100)}{\Delta T_A (V_O @ T_A = +25^\circ\text{C})}$$

where $\Delta T_A = +180^\circ\text{C}$ for the MC1563
 $+75^\circ\text{C}$ for the MC1463

The output-voltage adjusting resistors (R_A and R_B) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. Input regulation is the percentage change in output voltage per volt change in the input voltage and is expressed as

$$\text{Input Regulation} = \frac{v_o}{V_O (v_{in})} 100 (\%/V_O)$$

where v_o is the change in the output voltage V_O for the input change v_{in} .

The following example illustrates how to compute maximum output voltage change for the conditions given:

$$\begin{aligned} \text{Reg}_{in} &= 0.015\%/V_O \\ V_O &= 10 \text{ Vdc} \\ v_{in} &= 1.0 \text{ V(rms)} \\ v_o &= \frac{(\text{Reg}_{in})(v_{in})(V_O)}{100} \\ &= \frac{(0.015)(1.0)(10)}{100} \\ &= 0.0015 \text{ V(rms)} \end{aligned}$$

Note 5. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{V_O|_{I_L = 1.0 \text{ mA}} - V_O|_{I_L = 50 \text{ mA}}}{V_O|_{I_L = 1.0 \text{ mA}}} \times 100$$

TEST CIRCUITS

($I_L = 100 \text{ mA}$ dc, $T_C = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 4 - GENERAL TEST CIRCUIT

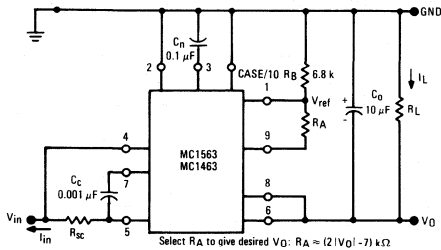


FIGURE 5 - LOAD TRANSIENT RESPONSE

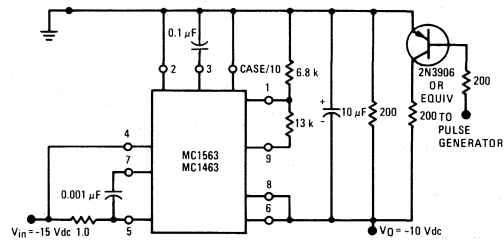


FIGURE 6 - INPUT REGULATION

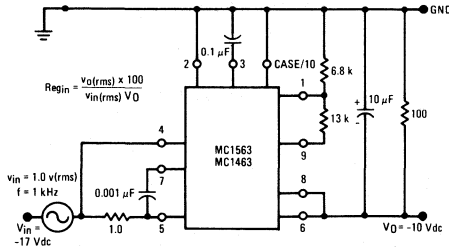


FIGURE 7 - LOAD REGULATION

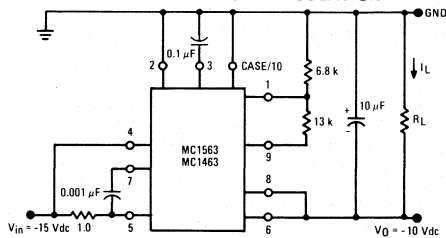


FIGURE 8 - OUTPUT IMPEDANCE

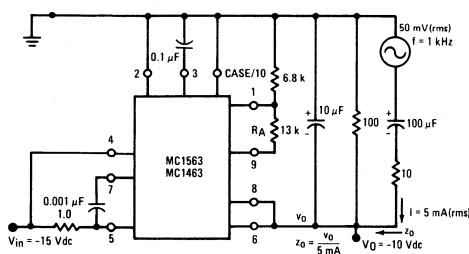
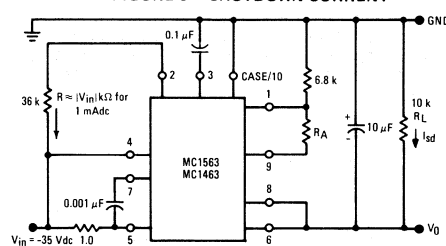


FIGURE 9 - SHUTDOWN CURRENT



GENERAL DESIGN INFORMATION

1. Output Voltage, V_O

- a) Output Voltage is set by resistors R_A and R_B (see Figure 10). Set $R_B = 6.8$ k ohms and determine R_A from the graph of Figure 11 or from the equation:

$$R_A \approx (2 |V_O| - 7) \text{ k}\Omega$$

- b) Output voltage can be varied by making R_A adjustable as shown in Figures 10 and 11.
- c) Output voltage, V_O , is determined by the ratio of R_A and R_B therefore optimum temperature performance can be achieved if R_A and R_B have the same temperature coefficient.
- d) $V_O = V_{ref} (1 + \frac{R_A}{R_B})$; therefore the tolerance on output voltage is determined by the tolerance of V_{ref} and R_A and R_B .

2. Short-Circuit Current, I_{sc}

Short-Circuit Current, I_{sc} is determined by R_{sc} . R_{sc} may be chosen with the aid of Figure 12 when using the typical circuit connection of Figure 10. See Figure 29 for current limiting during NPN current boost.

3. Compensation, C_c

A $0.001 \mu\text{F}$ capacitor (C_c , see Figure 10), will provide adequate compensation in most applications, with or without current boost. Smaller values of C_c will reduce stability and larger values of C_c will degrade pulse response and output impedance versus frequency. The physical location of C_c should be close to the MC1563/MC1463 with short lead lengths.

4. Noise Filter Capacitor, C_n

A $0.1 \mu\text{F}$ capacitor, C_n , from pin 3 to ground will typically reduce the output noise voltage to $120 \mu\text{V(rms)}$. The value of C_n can be increased or decreased, depending on the noise voltage requirements of a particular application. A minimum value of $0.001 \mu\text{F}$ is recommended.

5. Output Capacitor, C_o

The value of C_o should be at least $10 \mu\text{F}$ in order to provide good stability.

6. Shutdown Control

One method of turning "OFF" the regulator is to draw 1 mA from pin 2 (See Figure 9.) This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting. As the magnitude of the input-threshold voltage at pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at pin 2 will cause automatic shutdown for high junction temperatures (see Figure 37). This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard logic levels of MECL, MRTL, MDTL or MTTL can also be used to turn the regulator "ON" or "OFF" (see Figures 32 and 33).

7. Remote Sensing

The connection to pin 8 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on z_o can be greatly reduced (see Figure 35).

FIGURE 10 – TYPICAL CIRCUIT CONNECTION

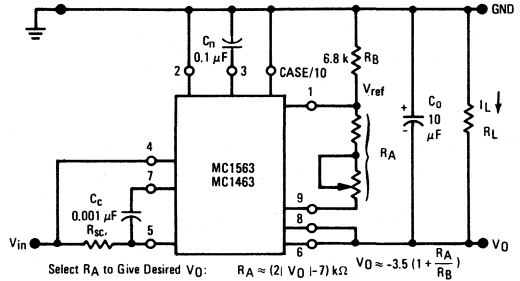


FIGURE 11 – R_A versus V_O

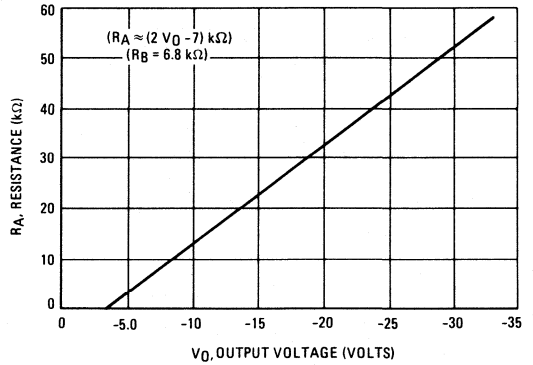
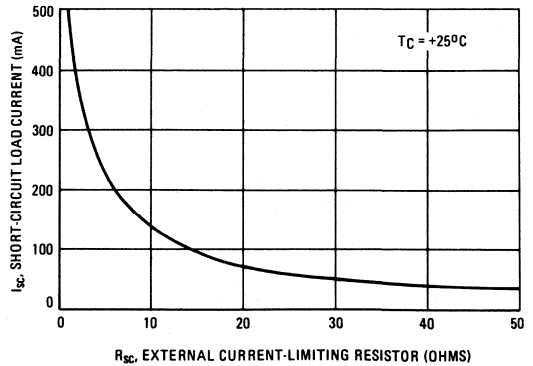


FIGURE 12 – I_{sc} versus R_{sc}



TYPICAL CHARACTERISTICS

Unless otherwise noted: $C_n = 0.1 \mu\text{F}$, $C_c = 0.001 \mu\text{F}$, $C_o = 10 \mu\text{F}$, $T_C = +25^\circ\text{C}$,
 $V_{in}(\text{nom}) = -15 \text{ Vdc}$, $V_O(\text{nom}) = -10 \text{ Vdc}$, $I_L = 100 \text{ mAdc}$

FIGURE 13 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

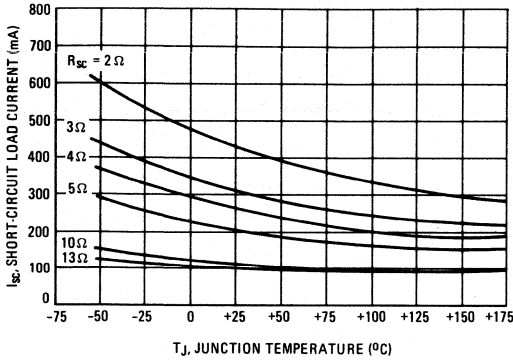


FIGURE 14 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE

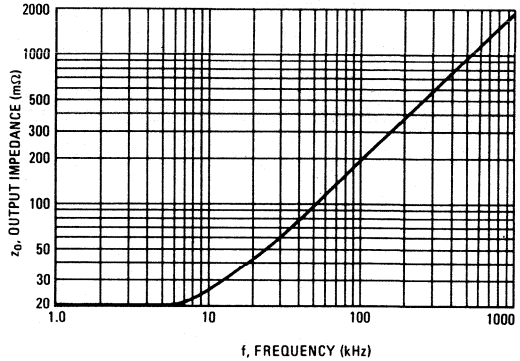


FIGURE 15 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

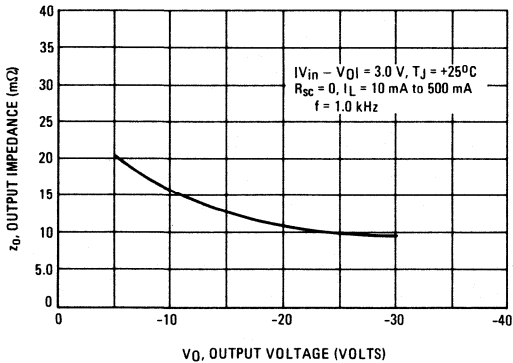


FIGURE 16 – OUTPUT IMPEDANCE versus R_{sc}

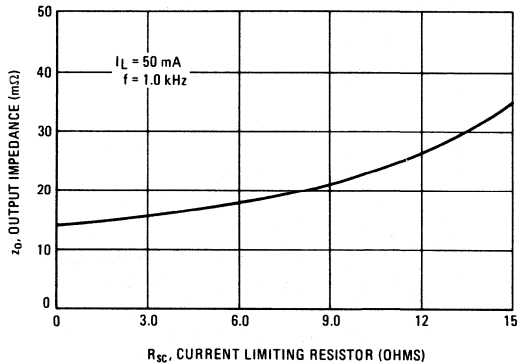


FIGURE 17 – FREQUENCY DEPENDENCE OF INPUT REGULATION

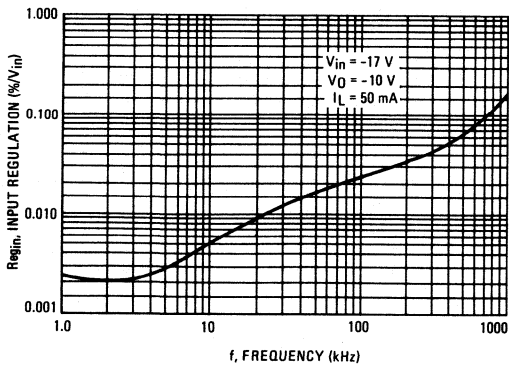
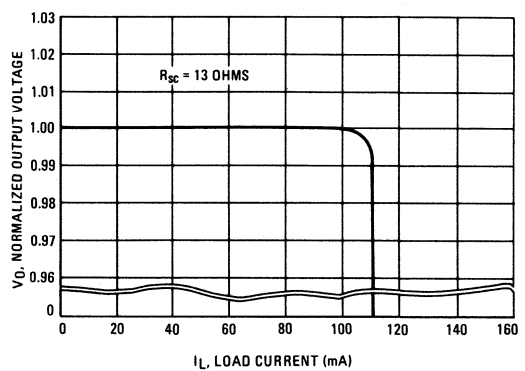


FIGURE 18 – CURRENT LIMITING CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

FIGURE 19 – BIAS CURRENT versus INPUT VOLTAGE

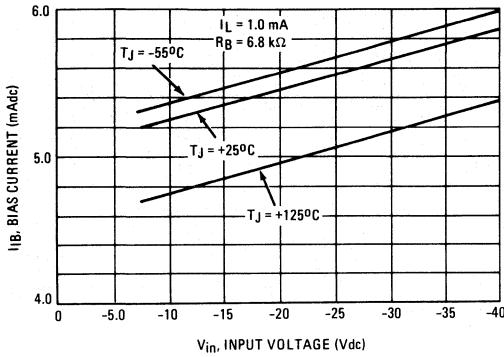


FIGURE 20 – EFFECTS OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

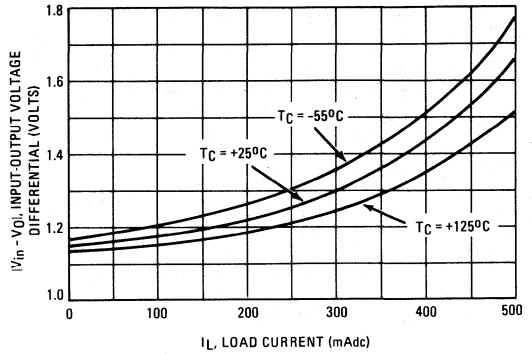


FIGURE 21 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

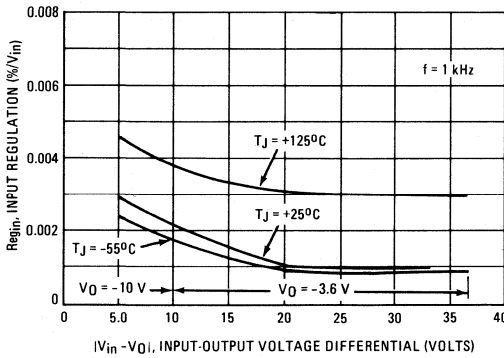


FIGURE 22 – INPUT TRANSIENT RESPONSE

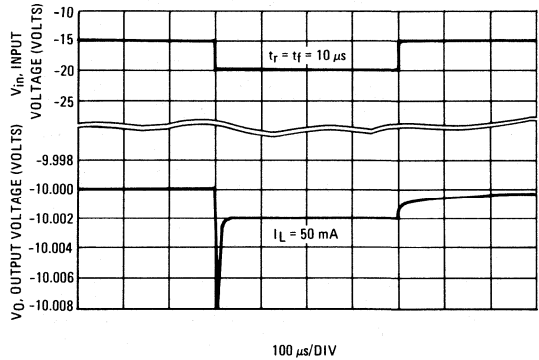


FIGURE 23 – LOAD TRANSIENT RESPONSE

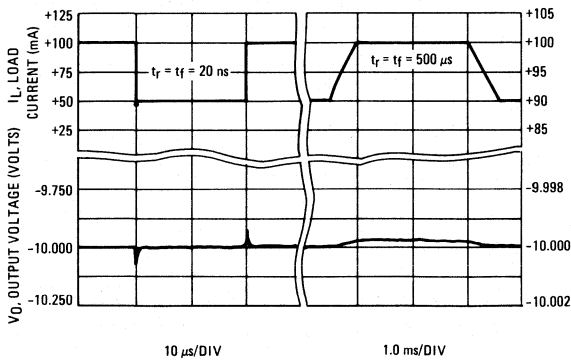
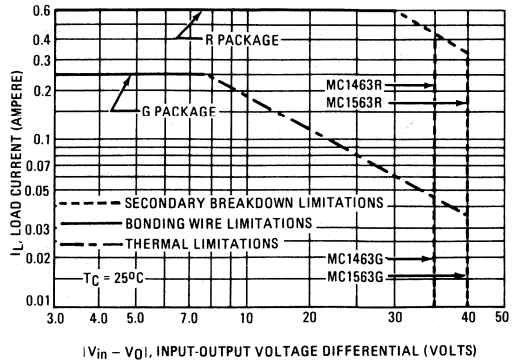


FIGURE 24 – DC OPERATING AREA



OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1563 (MC1463) negative voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE INDEX

| | Specification Pg. No. | | Specification Pg. No. |
|--------------------------------------|-----------------------|---|-----------------------|
| Theory of Operation | 7 | Remote Sensing | 12 |
| NPN Current Boosting | 9 | An Adjustable Zero-Temperature-Coefficient Voltage Source | 13 |
| PNP Current Boosting | 10 | Thermal Shutdown | 13 |
| Positive and Negative Power Supplies | 11 | Thermal Considerations | 13 |
| Shutdown Techniques | 11 | PC Board Layout and Information | 15 |
| Voltage Boosting | 12 | | |

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 25, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 26. The gain-determining resistors may be external, enabling a wide range of output voltages. This

is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1563) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1563 negative voltage regulator.

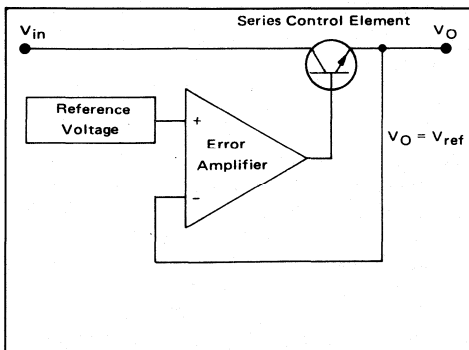


FIGURE 25 - Series Voltage Regulator

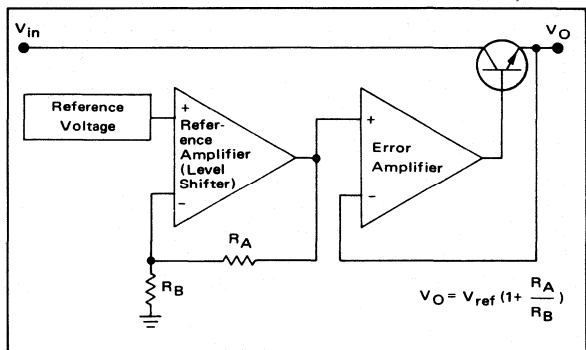
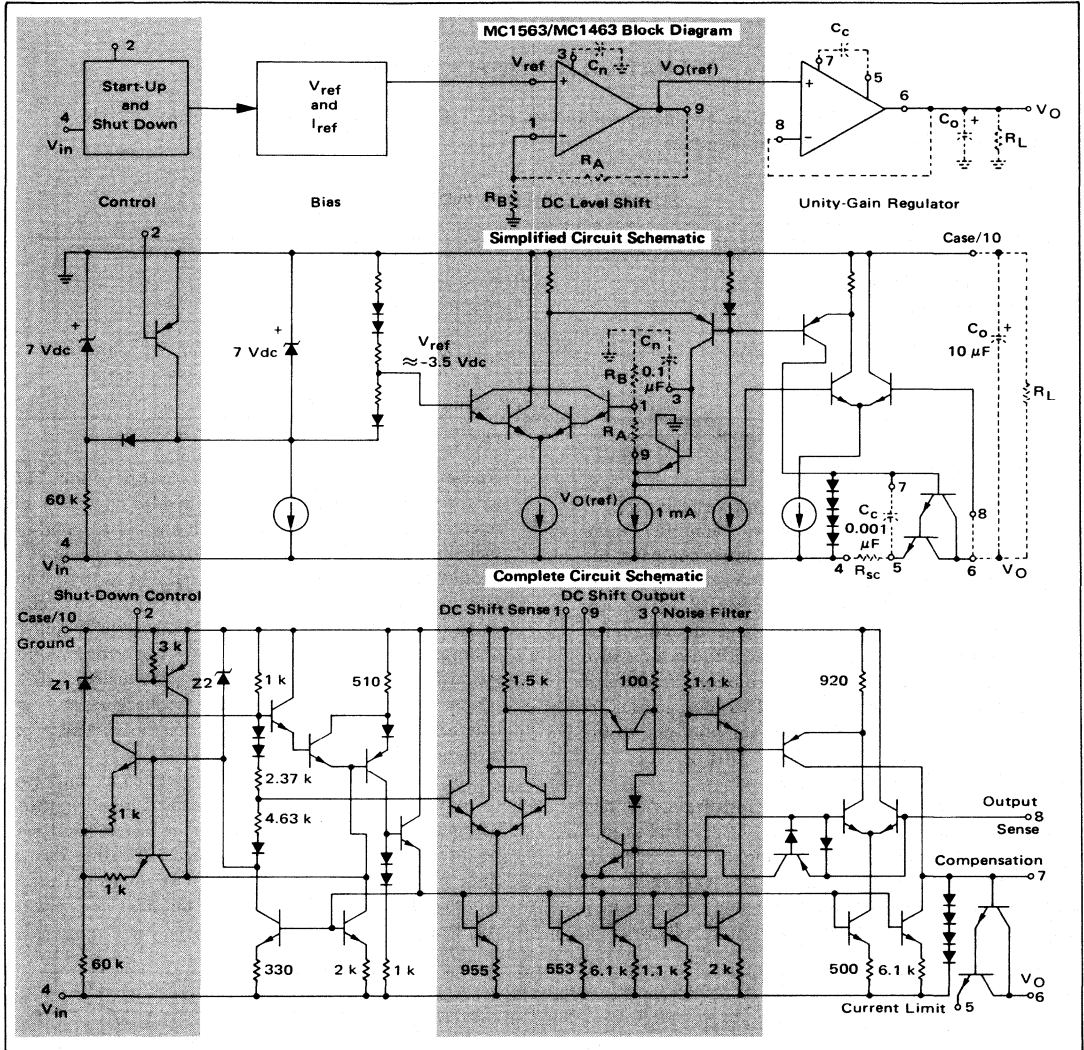


FIGURE 26 - The "Regulator-Within-A-Regulator" Approach

FIGURE 27
(Recommended External Circuitry is Depicted With Dotted Lines.)



MC1563 (MC1463) Operation

Figure 27 shows the MC1563 (MC1463) Negative Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated

input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

MC1563, MC1463 (continued)

The shutdown control, in effect, consists of a PNP transistor across the reference zener diode. When this transistor is turned "ON", via pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shutdown. During shutdown the current drain of the complete IC regulator drops to $V_{in}/60\text{ k}\Omega$ or $500\text{ }\mu\text{A}$ for a -30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately -3.5 Vdc with a typical temperature coefficient of $0.002\%/^{\circ}\text{C}$. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R_A and R_B) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_n , is introduced externally into the level shift network (via pin 3) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is $0.1\text{ }\mu\text{F}$ and should have a voltage rating in excess of the desired output voltage. Smaller capacitors ($0.001\text{ }\mu\text{F}$ minimum) may be used but will cause a slight increase in output noise. Larger values of C_n will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

The output of the shift amplifier is fed internally to the noninverting input of the output error amplifier. The

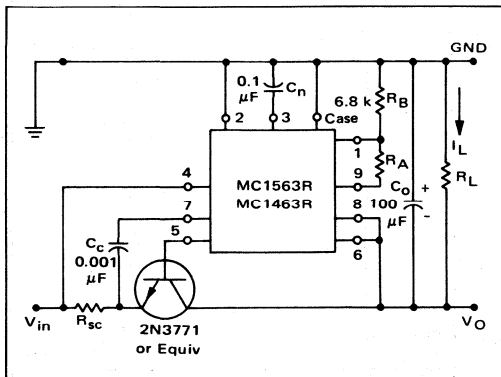


FIGURE 28 – Typical NPN Current Boost Connection

inverting input to this amplifier is the Output Sense connection (pin 8) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{sc} , is connected in the emitter of this transistor to sample the full load current. This connection enables a four-diode string to limit the drive current to the power transistors in a conventional manner.

Stability and Compensation

As has been seen, the MC1563 employs two amplifiers, each using negative feedback. This implies the possibility of frequency instability due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (pin 7) and pin 5. The recommended value of $0.001\text{ }\mu\text{F}$ will insure stability and still provide acceptable transient response (see Figure 23). It is also necessary to use an output capacitor, C_o , (typically $10\text{ }\mu\text{F}$) directly from the output (pin 6) to ground. When an external transistor is used to boost the current, $C_o = 100\text{ }\mu\text{F}$ is recommended (see Figure 28).

NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 2 or 28, are recommended. The circuit shown in Figure 28 can supply up to approximately 4.0 amperes (subject to safe area limitations). At higher currents the V_{BE} of the pass transistor may itself exceed the threshold of the current limit even for $R_{sc} = 0$. Figure 2 illustrates the use of an additional external diode from pin 4 for higher current operation or for pass transistors exhibiting higher V_{BE} 's. It will probably be necessary to determine R_{sc} experimentally for each case where a pass transistor is used because V_{BE} varies from device to device.

The circuit of Figure 28 when set up for a -10 V output

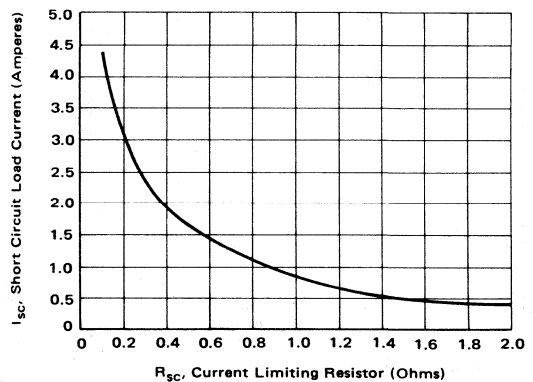


FIGURE 29 – I_{sc} versus R_{sc} (reference Figure 28)

MC1563, MC1463 (continued)

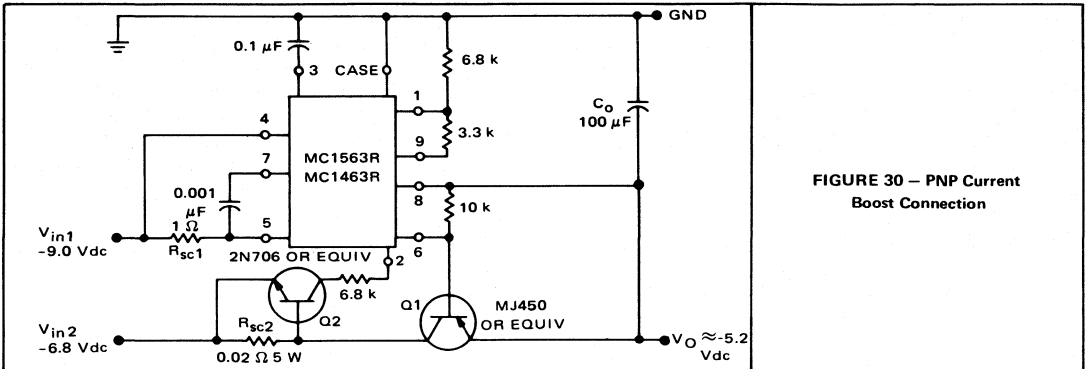


FIGURE 30 – PNP Current Boost Connection

($R_A = 13\text{ k}\Omega$) supply and operating with a -15 V input, with a R_{SC} of $0.1\ \Omega$, will yield a change in output voltage of only 26 mV over a load current range of from 1 mA to 3.5 A . This corresponds to a dc output impedance of only 7.5 milliohms or a percentage load regulation of 0.26% for a full 3.5-ampere load current change. Figure 29, indicates how the short circuit current varies with the value of R_{SC} for this circuit.

PNP CURRENT BOOSTING

A PNP power transistor can also be used to boost the load current capabilities. To improve the efficiency of the PNP boost configuration, particularly for small output voltages, the circuit of Figure 30, is recommended. An auxiliary -9 volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 10-ampere regulator of Figure

30 this represents a savings of 22 watts when compared with operating the regulator from the single -9 V supply. It can supply current to 10 amperes while requiring an input voltage to the collector of the pass transistor of -6.8 volts minimum. The pass transistor is limited to 10 amperes by the added short-circuit current network in its emitter (R_{SC2}) and the IC regulator is limited to 500 mA in the conventional manner (R_{SC1}). The MJ450 exhibits a minimum h_{FE} of 20 at 10 amperes , thus requiring only 500 mA from the MC1563R. Regulation of this circuit is comparable to that of the NPN boost configuration.

For higher output voltages the additional unregulated power supply is not required. The collector of the PNP boost transistor can tie directly to pin 5 and the internal current limit circuit will provide short-circuit protection using R_{SC} (see Figure 12). Transistor Q2 and R_{SC2} will not be required and pin 2 should be returned to ground.

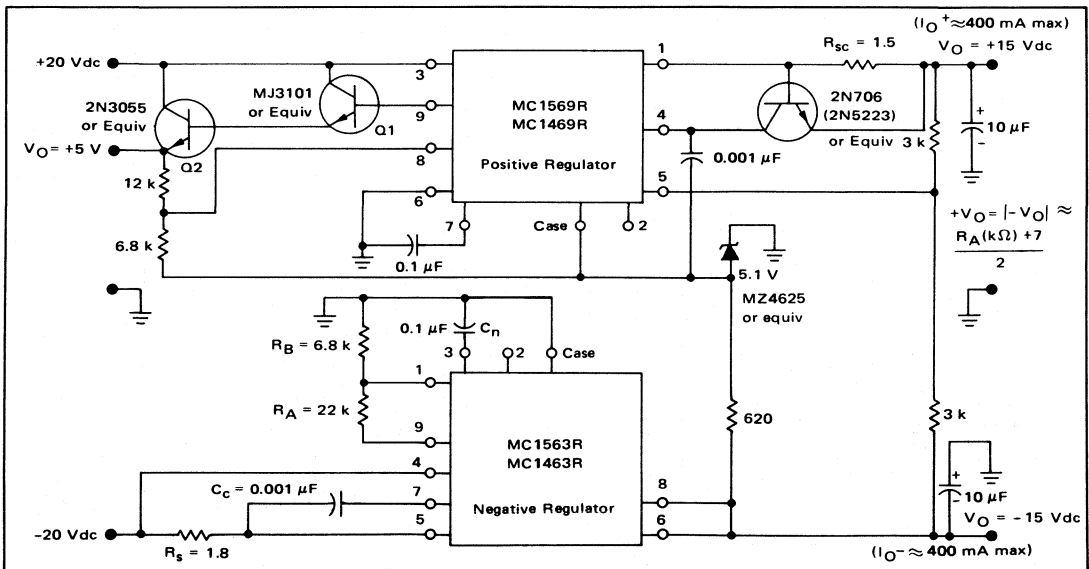
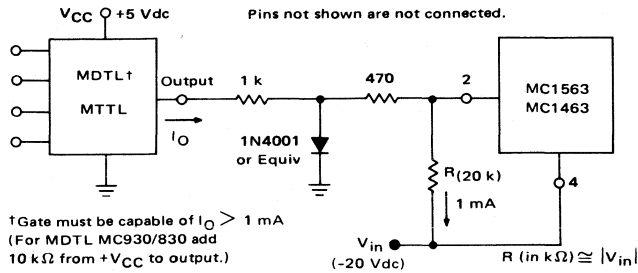


FIGURE 31 – A ±15 Vdc Complementary Tracking Regulator With Auxiliary +5.0 V Supply

FIGURE 32 – Saturated Logic Level Shutdown Circuit



POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1563 is driven from a floating source it is possible to use it as a positive regulator by grounding the negative output terminal. The MC1563 may also be used with the MC1569 to provide completely independent positive and negative power regulators with comparable performance. When used in this manner a silicon diode such as the 1N4001 must be connected as a clamp on the output with the cathode to ground and the anode to the negative output voltage. This is to prevent the positive voltage in the system from forcing the output to a positive value and preventing the MC1563 from starting up.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 3 and 31 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (pin 6 of the MC1569) and using the other side (pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3 k-ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at pin 5 will be zero. When the voltage at pin 5 equals zero, +|V_O| must equal -|V_O|.

For the configuration shown in Figure 31, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5-volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5-volt supply, as shown,

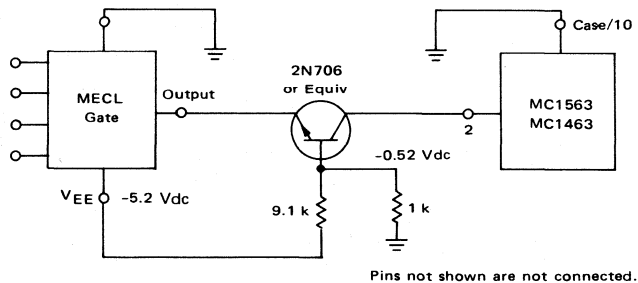
is not short-circuit protected). The -15-volt supply varies less than 0.1 mV over a zero to -300 mAdc current range and the +15-volt supply tracks this variation. The +15-volt supply varies 20 mV over the zero to +300-mAdc load current range. The +5-volt supply varies less than 5 mV for $0 \leq I_L \leq 200$ mA with the other two voltages remaining unchanged. See MC1561 data sheet (DS9104 R3), or MC1569 data sheet (DS9152 R2) for information concerning latch-up when using plus and minus regulations.

SHUTDOWN TECHNIQUES

Pin 2 of the MC1563 is provided for the express purpose of shutting the regulator "OFF". Referring to the schematic, it can be seen that pin 2 goes to the base of a PNP transistor; which, if turned "ON", will deny current to all the biasing current sources. This action causes the output to go to essentially zero volts and the only current drawn by the IC regulator will be the small start current through the 60 k-ohm start resistor ($V_{in}/60$ k Ω). This feature provides additional versatility in the applications of the MC1563. Various sub-systems may be placed in a "standby" mode to conserve power until actually needed. Or the power may be turned "OFF" in response to other occurrences such as over-heating, over-voltage, shorted output, etc.

As an illustration of the first case, consider a system consisting of both positive-supply logic (MTTL) and negative-supply logic (MECL). The MECL logic may be used in a high-speed arithmetic processor whose services are not continuously required. Substantial power may

FIGURE 33 – MECL Logic Level Shutdown Circuit



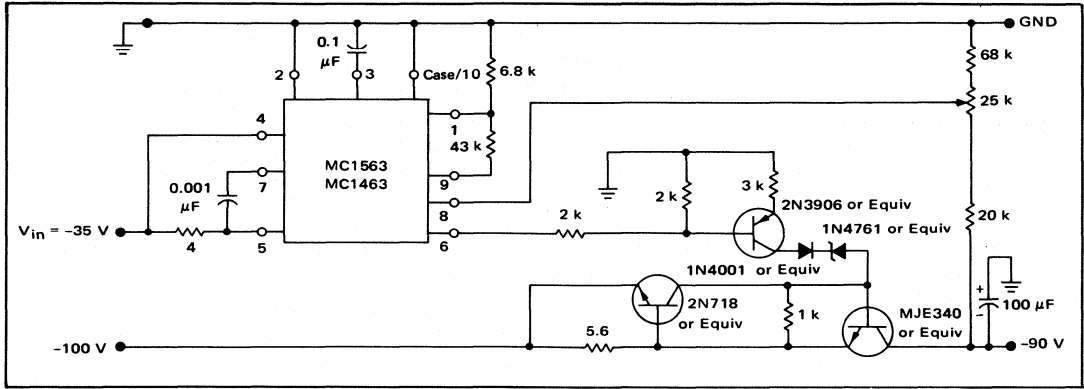


FIGURE 34 – Voltage Boosting Circuit

thus be conserved if the MECL circuitry remains unpowered except when needed. The negative regulator can be shutdown using any of the standard logic swings. For saturated logic control, Figure 32 shows a circuit that allows the normal positive output swing to cause the regulator to shutdown when the logic output is in the low voltage state. The negative output levels of a MECL gate can also be used for shutdown control as shown in Figure 33.

VOLTAGE BOOSTING

Some applications may require a high output voltage which may exceed the voltage rating of the MC1563. This must be solved by assuring that the IC regulator is operated within its limits. Three points in the regulator need to be considered:

1. The input voltage (pin 4),
2. the output voltage (pin 6) and,
3. the output sense lead (pin 8).

A reduced input voltage can be provided by using a separate supply. The output voltage may be zener-level shifted, and the sense line can tie to a portion of the output voltage through a resistive divider. The voltage boost circuit of Figure 34 uses this approach to provide a -90 volt supply. This circuit will exhibit regulation of 0.001% over a 100 mA load current range.

REMOTE SENSING

The MC1563 offers a remote sensing capability. This is important when the load is remote from the regulator, as the resistances of the interconnecting lines (V_{EE} and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 35 shows how remote sensing is accomplished using both a separate sense line from pin 8 and a separate ground line from the regulator to the remote load.

7

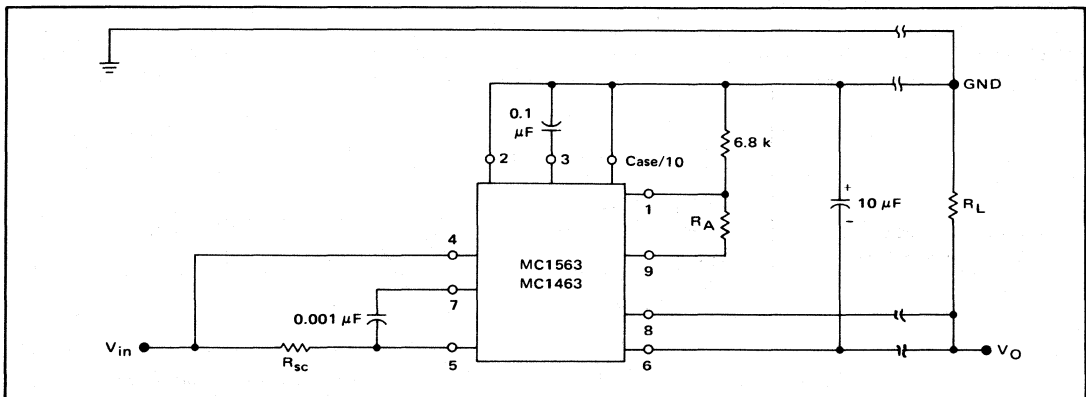


FIGURE 35 – Remote Sensing Circuit

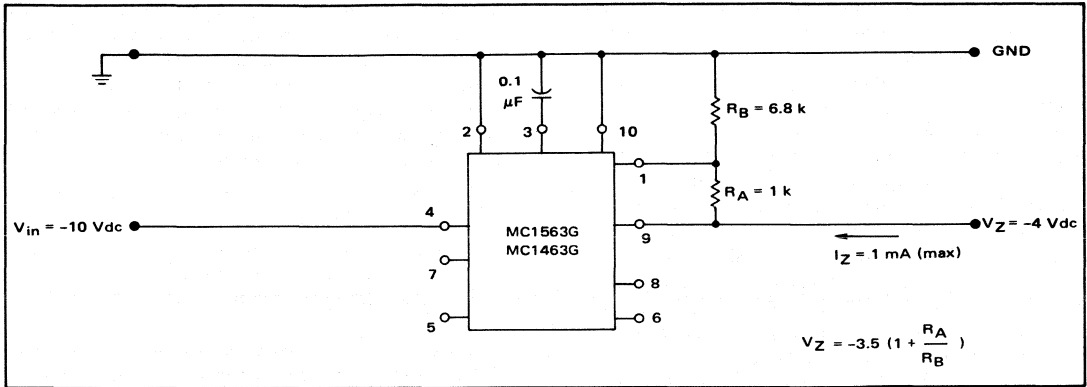


FIGURE 36 – An Adjustable “Zero-TC” Voltage Source

AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE

The MC1563, when used in conjunction with low-TC resistors, makes an excellent reference-voltage generator. If the -3.5 volt reference voltage of the IC regulator is a satisfactory value, then pins 1 and 9 can be tied together and no resistors are needed. This will provide a voltage reference having a typical temperature coefficient of 0.002%/°C. By adding two resistors, RA and RB, any voltage between -3.5 Vdc and -37 Vdc can be obtained with the same low TC (see Figure 36).

THERMAL SHUTDOWN

By setting a fixed voltage at pin 2, the MC1563 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor (-1.9 x

10⁻³V/°C). By setting -0.61 Vdc externally, at pin 2, the regulator will shutdown when the chip temperature reaches approximately 140°C. Figure 37 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

In the case where an external pass transistor is employed; its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 38. The case of the normally “OFF” thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application,

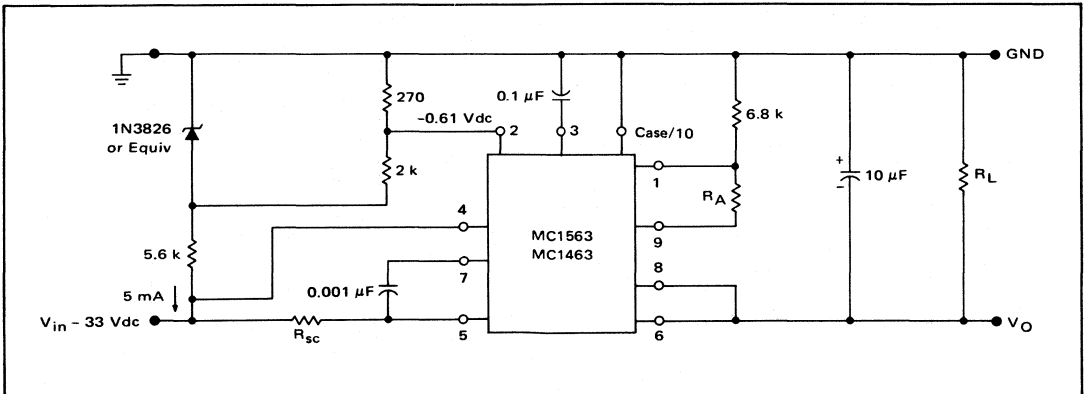


FIGURE 37 – Junction Temperature Limiting Shutdown Circuit

MC1563, MC1463 (continued)

the designer must use caution not to exceed the specified maximum junction temperature ($+175^{\circ}\text{C}$). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor*. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current (500 mA). Care should be taken not to exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 24).

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, T_A , or a change in the power dissipated in the IC regulator. The effects of ambient

*For more detailed information of methods used to compute junction temperature, see Motorola Application Note AN-226, Measurement of Thermal Properties of Semiconductors.

temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as $\pm 0.002\%/^{\circ}\text{C}$, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O , can be used to describe this effect and is typically $+0.03\%/watt$ for the MC1563R. For an example of the relative magnitudes of these effects, consider the following conditions:

Given: MC1563R
 with $V_{in} = -10\text{ Vdc}$
 $V_O = -5\text{ Vdc}$
 and $I_L = 100\text{ mA to } 200\text{ mA}$
 $(\Delta I_L = 100\text{ mA})$
 assume $T_A = +25^{\circ}\text{C}$
 TO-66 Type Case with heatsink

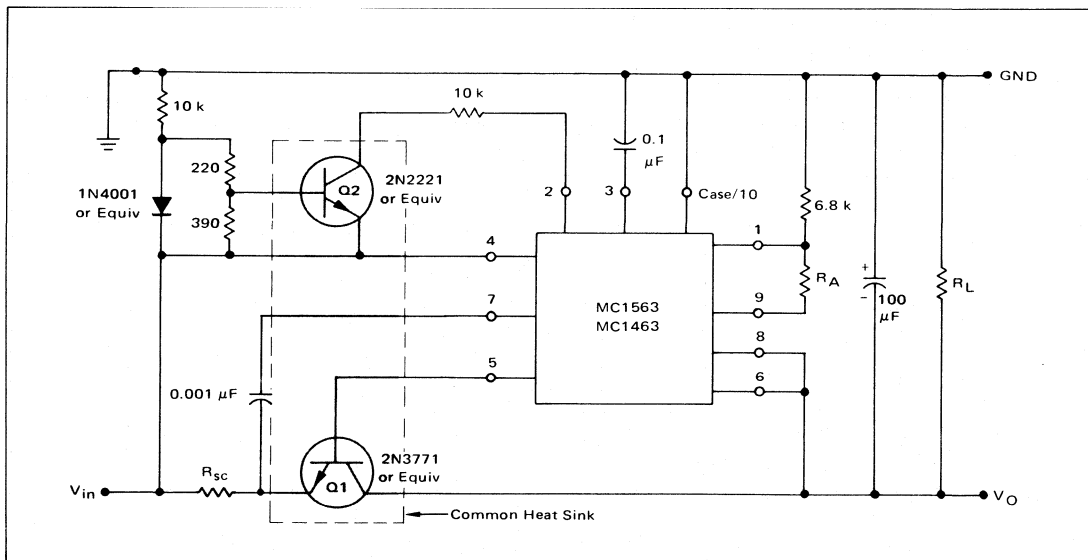


FIGURE 38 – Thermal Shutdown When Using External Pass Transistors

assume $\theta_{CS} = 0.2^{\circ}\text{C}/\text{W}$

and $\theta_{SA} = 2^{\circ}\text{C}/\text{W}$

It is desired to find the ΔV_O which results from this ΔI_L . Each of the three previously stated effects on V_O can now be separately considered.

1. ΔV_O due to ΔT_J

$$\Delta V_O = (V_O)(\Delta P_D)(TCV_O)(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

OR

$$\Delta V_O = (5 \text{ V})(5 \text{ V} \times 0.1 \text{ A})(\pm 0.002\%/^{\circ}\text{C})(19.2^{\circ}\text{C}/\text{W})$$

$$\Delta V_O \approx \pm 1.0 \text{ mV}$$

2. ΔV_O due to z_o

$$|\Delta V_O| = (-z_o)(I_L)$$

$$|\Delta V_O| = -(2 \times 10^{-2})(10^{-1}) = -2 \text{ mV}$$

3. ΔV_O due to gradient coefficient, GCV_O

$$|\Delta V_O| = (GCV_O)(V_O)(\Delta P_D)$$

$$|\Delta V_O| = (+3 \times 10^{-4}/\text{W})(5 \text{ volts})(5 \times 10^{-1} \text{ W})$$

$$|\Delta V_O| = +0.8 \text{ mV}$$

Therefore the total ΔV_O is given by

$$|\Delta V_O \text{ total}| = \pm 1.0 - 2.0 + 0.8 \text{ mV}$$

OR

$$-2.2 \text{ mV} \leq |\Delta V_O \text{ total}| \leq -0.2 \text{ mV}$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

Typical Printed Circuit Board Layout

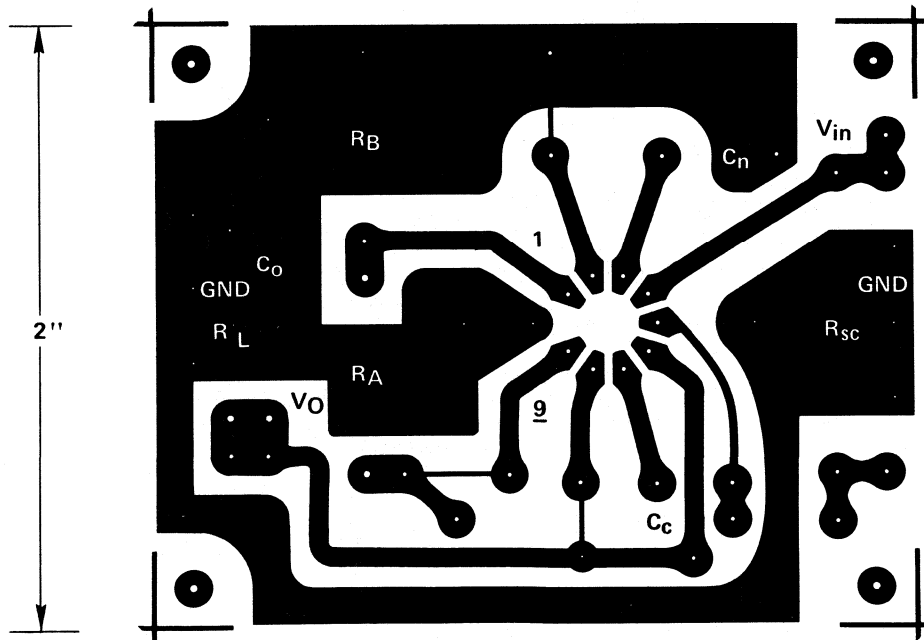
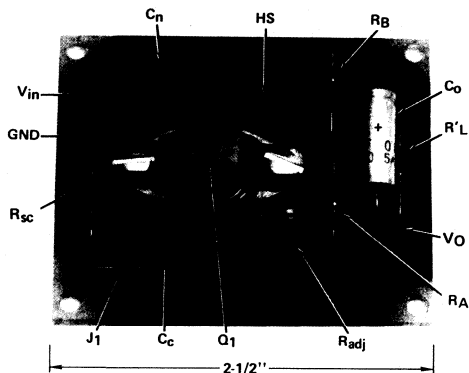


FIGURE 39 – Location of Components



Note 1:

When R_{adj} is used it is necessary to remove the copper which shorts out R_{adj} .

Note 2:

Extra holes are available in the circuit board to permit two resistors to be paralleled to obtain the desired value of R_{sc} .

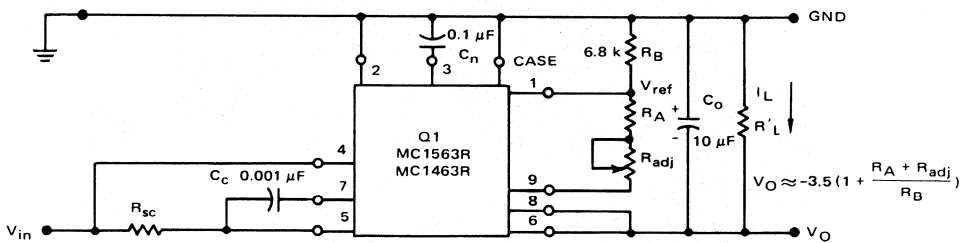
Note 3:

If pin 2 is used to shut down the regulator, remove the copper which shorts pin 2 to ground.

Note 4:

Remote sensing can be achieved by removing the copper which shorts pin 8 to pin 6 and connecting pin 8 directly to the "minus" load terminal. The circuit board ground should be connected to the unregulated power supply ground at the "plus" load terminal.

Typical Circuit Connection for Output Voltages Between -3.5 and -37 Volts



Select $R_A + R_{adj}$ to Give Desired V_O : $R_A + R_{adj} \approx (2|V_O| - 7) \text{ k}\Omega$ with $R_B = 6.8 \text{ k}\Omega$

PARTS LIST

| Component | Value | Description |
|-----------|---------------------|---|
| R_A | Select | } 1/4 or 1/2 watt carbon |
| R_B | 6.8 k | |
| R_{adj} | Select | |
| R_{sc} | Select | 1/2 watt carbon |
| R'_L | Select | For minimum current of 1 mA dc |
| C_o | 10 μF | Sprague 1500 Series, Dickson D10C series or equivalent |
| C_n | 0.1 μF | } Ceramic Disc – Centralab DDA104, or equivalent |
| C_c | 0.001 μF | |
| J_1 | | Jumper |
| Q1 | | MC1563R or MC1463R |
| *HS | | Heatsink Thermalloy #6168B or equivalent |
| *Socket | (Not Shown) | Robinson Nugent #0001306 or equivalent Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1 or equivalent |
| PC Board | | Circuit DOT, Inc. #PC1113 or equivalent 1155 W. 23rd St. Tempe, Arizona 85281 |

*Optional

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MC1566L MC1466L

MULTI-PURPOSE REGULATORS

Specifications and Applications Information

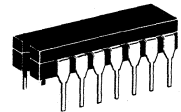
MONOLITHIC VOLTAGE AND CURRENT REGULATOR

This unique "floating" regulator can deliver hundreds of volts — limited only by the breakdown voltage of the external series pass transistor. Output voltage and output current are adjustable. The MC1466/MC1566 integrated circuit voltage and current regulator is designed to give "laboratory" power-supply performance.

- Voltage/Current Regulation with Automatic Crossover
- Excellent Line Voltage Regulation, 0.01% +1.0 mV
- Excellent Load Voltage Regulation, 0.01% +1.0 mV
- Excellent Current Regulation, 0.1% +1.0 mA
- Short-Circuit Protection
- Output Voltage Adjustable to Zero Volts
- Internal Reference Voltage
- Adjustable Internal Current Source

PRECISION WIDE-RANGE VOLTAGE and CURRENT REGULATOR EPIAXIAL PASSIVATED

CERAMIC PACKAGE
CASE 632
TO-116



TYPICAL APPLICATIONS

FIGURE 1 — 0-TO-15 VDC, 10-AMPERES REGULATOR

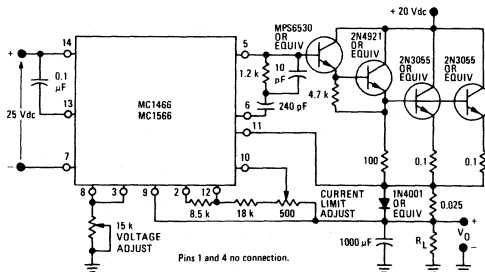


FIGURE 2 — 0-TO-40 VDC, 0.5-AMPERE REGULATOR

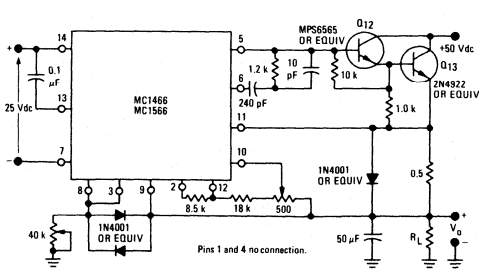


FIGURE 3 — 0-TO-250 VDC, 0.1-AMPERE REGULATOR

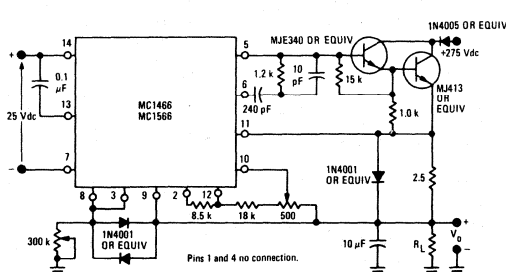
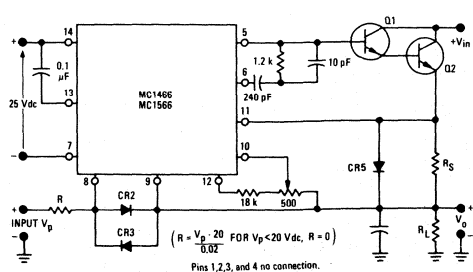


FIGURE 4 — REMOTE PROGRAMMING



(MC1566L — Pg. 1)

See Packaging Information Section for outline dimensions.

MC1566L, MC1466L (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|-------------------------------------|-------------------------|-------------|
| Auxiliary Voltage | V _{aux} | 30 35 | Vdc |
| Power Dissipation (Package Limitation) Derate above T _A = +50°C | P _D 1/θ _{JA} | 750 6.0 | mW mW/°C |
| Operating Temperature Range | T _A | 0 to +75 -55 to +125 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{aux} = +25 Vdc unless otherwise noted)

| Characteristic Definition | Characteristic | Symbol | Min | Typ | Max | Units |
|---------------------------|---|-------------------------------------|--------------|------------------------|--------------|-------|
| | Auxiliary Voltage (See Notes 1 & 2) (Voltage from pin 14 to pin 7) | V _{aux} | 21 20 | — — | 30 35 | Vdc |
| | Auxiliary Current | I _{aux} | — — | 9.0 7.0 | 12 8.5 | mAdc |
| | Internal Reference Voltage (Voltage from pin 12 to pin 7) | V _{IR} | 17.3 17.5 | 18.2 18.2 | 19.7 19 | Vdc |
| | Reference Current (See Note 3) | I _{ref} | 0.8 0.9 | 1.0 1.0 | 1.2 1.1 | mAdc |
| | Input Current-Pin 8 | I _g | — — | 6.0 3.0 | 12 6.0 | µAdc |
| | Power Dissipation | P _D | — — | — — | 360 300 | mW |
| | Input Offset Voltage, Voltage Control Amplifier (See Note 4) | V _{ioV} | 0 3.0 | 15 15 | 40 25 | mVdc |
| | Load Voltage Regulation (See Note 5) | ΔV _{ioV} | — — | 1.0 0.7 | 3.0 1.0 | mV |
| | Line Voltage Regulation (See Note 6) | ΔV _{ref} /V _{ref} | — — | 0.015 0.004 | 0.03 0.01 | % |
| | Temperature Coefficient of Output Voltage (T _A = 0 to +75°C) (T _A = -55 to +25°C) (T _A = +25 to +125°C) | TC _{V_O} | — — — | 0.01 0.006 0.004 | — — — | %/°C |
| | Input Offset Voltage, Current Control Amplifier (See Note 4) (Voltage from pin 10 to pin 11) | V _{ioI} | 0 3.0 | 15 15 | 40 25 | mVdc |
| | Load Current Regulation (See Note 7) | ΔI _L /I _L | — — | — — | 0.2 0.1 | % |
| | ΔI _{ref} | — — | — — | 1.0 1.0 | mAdc | |

Pins 1 and 4 no connection.

(MC1566L - Pg. 2)

MC1566L, MC1466L (continued)

NOTE 1:

The instantaneous input voltage, V_{aux} , must not exceed the maximum value of 30 volts for the MC1466 or 35 volts for the MC1566. The instantaneous value of V_{aux} must be greater than 20 volts for the MC1566 or 21 volts for the MC1466 for proper internal regulation.

NOTE 2:

The auxiliary supply voltage V_{aux} , must "float" and be electrically isolated from the unregulated high voltage supply, V_{in} .

NOTE 3:

Reference current may be set to any value of current less than 1.2 mA_{dc} by applying the relationship:

$$I_{ref} \text{ (mA)} = \frac{8.95}{R_1 \text{ (k}\Omega)}$$

NOTE 4:

A built-in offset voltage (15 mVdc nominal) is provided so that the power supply output voltage or current may be adjusted to zero.

NOTE 5:

Load Voltage Regulation is a function of two additive components, ΔV_{ioV} and ΔV_{ref} , where ΔV_{ioV} is the change in input offset voltage (measured between pins 8 and 9) and ΔV_{ref} is the change in voltage across R2 (measured between pin 8 and ground). Each component may be measured separately or the sum may be measured across the load. The measurement procedure for the test circuit shown is:

- With S1 open ($I_L = 0$) measure the value of $V_{ioV} (1)$ and $V_{ref} (1)$.
- Close S1, adjust R4 so that $I_L = 500 \mu A$ and note $V_{ioV} (2)$ and $V_{ref} (2)$.

Then $\Delta V_{ioV} = V_{ioV} (1) - V_{ioV} (2)$

% Reference Regulation =

$$\frac{[V_{ref} (1) - V_{ref} (2)]}{V_{ref} (1)} (100\%) = \frac{\Delta V_{ref}}{V_{ref}} (100\%)$$

Load Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}} (100\%) + \Delta V_{ioV}$$

NOTE 6:

Line Voltage Regulation is a function of the same two additive components as Load Voltage Regulation, ΔV_{ioV} and ΔV_{ref} (see note 5). The measurement procedure is:

- Set the auxiliary voltage, V_{aux} , to 22 volts for the MC1566 or the MC1466. Read the value of $V_{ioV} (1)$ and $V_{ref} (1)$.
- Change the V_{aux} to 28 volts for the MC1566 or the MC1466 and note the value of $V_{ioV} (2)$ and $V_{ref} (2)$. Then compute Line Voltage Regulation:

$$\Delta V_{ioV} = \Delta V_{ioV} (1) - V_{ioV} (2)$$

% Reference Regulation =

$$\frac{[V_{ref} (1) - V_{ref} (2)]}{V_{ref} (1)} (100\%) = \frac{\Delta V_{ref}}{V_{ref}} (100\%)$$

Line Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}} (100\%) + \Delta V_{ioV}$$

NOTE 7:

Load Current Regulation is measured by the following procedure:

- With S2 open, adjust R3 for an initial load current, $I_L (1)$, such that V_O is 8.0 Vdc.
- With S2 closed, adjust R_T for $V_O = 1.0$ Vdc and read $I_L (2)$. Then Load Current Regulation =

$$\frac{[I_L (2) - I_L (1)]}{I_L (1)} (100\%) + I_{ref}$$

where I_{ref} is 1.0 mA_{dc}, Load Current Regulation is specified in this manner because I_{ref} passes through the load in a direction opposite that of load current and does not pass through the current sense resistor, R_S .

FIGURE 5

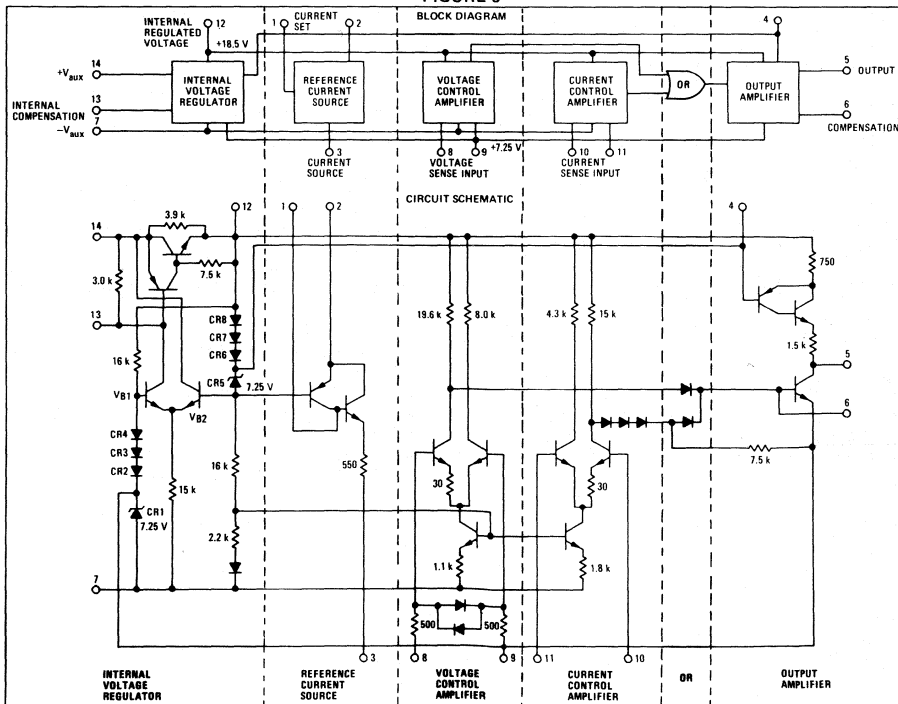
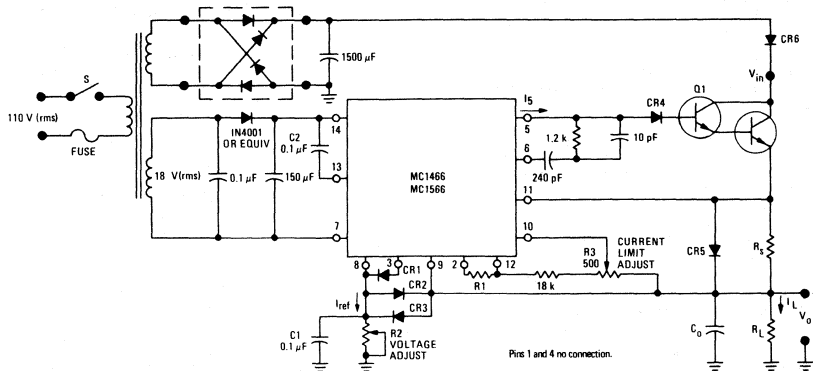


FIGURE 6 - TYPICAL CIRCUIT CONNECTION



NORMAL DESIGN PROCEDURE AND DESIGN CONSIDERATIONS

- Constant Voltage:**
 For constant voltage operation, output voltage V_O is given by:

$$V_O = (I_{ref}) (R_2)$$
 where R_2 is the resistance from pin 8 to ground and I_{ref} is the output current of pin 3.
 The recommended value of I_{ref} is 1.0 mAdc. Resistor R_1 sets the value of I_{ref} :

$$I_{ref} = \frac{8.5}{R_1}$$
 where R_1 is the resistance between pins 2 and 12.
- Constant Current:**
 For constant current operation:
 (a) Select R_S for a 250 mV drop at the maximum desired regulated output current, I_{max} .
 (b) Adjust potentiometer R_3 to set constant current output at desired value between zero and I_{max} .
- If V_{in} is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466/MC1566 during short-circuit or transient conditions.
- In applications where very low output noise is desired, R2 may be bypassed with C1 (0.1 µF to 2.0 µF). When R2 is bypassed, CR1 is necessary for protection during short-circuit conditions.
- CR5 is recommended to protect the MC1466/MC1566 from simultaneous pass transistor failure and output short-circuit.
- The RC network (10 pF, 240 pF, 1.2 k ohms) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if f_r of Q1 and Q2 is greater than 0.5 MHz.
- For remote sense applications, the positive voltage sense terminal (pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R2) is connected to the negative load terminal through a separate sense lead.
- C_O may be selected by using the relationship:

$$C_O = (100 \mu F) I_L(max)$$
 where $I_L(max)$ is the maximum load current in amperes.
- C2 is necessary for the internal compensation of the MC1466/MC1566.
- For optimum regulation, current out of pin 5, I_5 , should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:

$$\frac{I_{max}}{\beta_1 \beta_2} \leq 0.5 \text{ mAdc}$$
 where: I_{max} = maximum short-circuit load current (mAdc)
 β_1 = minimum beta of Q1
 β_2 = minimum beta of Q2
 Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5 \text{ mAdc}$ will result in a degradation in regulation.
- CR6 is recommended when $V_O > 150 \text{ Vdc}$ and should be rated such that Peak Inverse Voltage $> V_O$.

OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1566/MC1466 voltage and current regulator and also provides information on useful applications.

SUBJECT SEQUENCE

| |
|--|
| <p>Theory of Operation Applications Transient Failures Voltage/Current-Mode Indicator</p> |
|--|

THEORY OF OPERATION

The schematic of Figure 5 can be simplified by breaking it down into basic functions, beginning with a simplified version of the voltage reference, Figure 7. Zener diodes CR1 and CR5 with their associated forward biased diodes CR2 through CR4 and CR6 through CR8 form the stable reference needed to balance the differential amplifier. At balance ($V_{B1} = V_{B2}$), the output voltage, ($V_{12} - V_7$), is at a value that is twice the drop across either of the two diode strings: $V_{12} - V_7 = 2 (V_{CR1} + V_{CR2} + V_{CR3} + V_{CR4})$. Other voltages, temperature compensated or otherwise, are also derived from these diodes strings for use in other parts of the circuit.

The voltage controlled current source (Figure 8) is a PNP-NPN composite which, due to the high NPN beta,

yields a good working PNP from a lateral device working at a collector current of only a few microamperes. Its base voltage (V_{B2}) is derived from a temperature compensated portion of the diode string and consequently the overall current is dependent on the value of emitter resistor R1. Temperature compensation of the base emitter junction of Q3 is not important because approximately 9 volts exists between V_{B2} and V_{12} , making the ΔV_{BE} 's very small in percentage. Circuit reference voltage is derived from the product of I_R and R_R ; if I_R is set at 1 mA ($R_1 = 8.5 \text{ k}\Omega$), then R_R (in $\text{k}\Omega$) = V_O . Other values of current may be used as long as the following restraints are kept in mind: 1) package dissipation will be increased by about 11 mW/mA and 2) bias current for the voltage control amplifier is 3 μA , temperature dependent, and is extracted from the reference current. The reference current should

FIGURE 7 - REFERENCE VOLTAGE REGULATOR

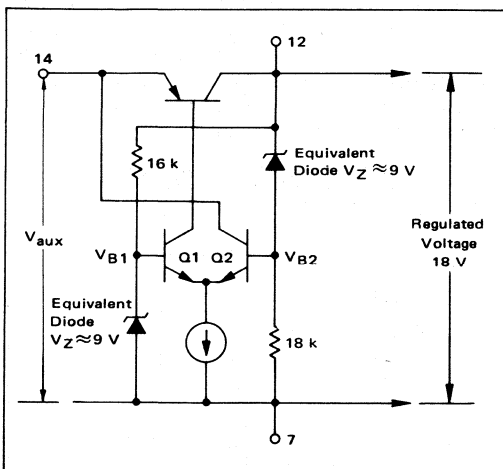
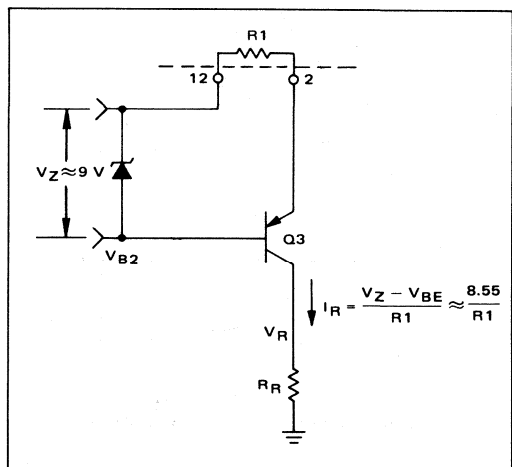


FIGURE 8 - VOLTAGE CONTROLLED CURRENT SOURCE



MC1566L, MC1466L (continued)

be at least two orders of magnitude above the largest expected bias current.

Loop amplification in the constant voltage mode is supplied by the voltage controlled amplifier (Figure 9), a standard high-gain differential amplifier. The inputs are diode-protected against differential overvoltages and an emitter degenerating resistor, R_{OS} , has been added to one of the transistors. For an emitter current in both Q5 and Q6 of 1/2 milliampere there will exist a preset offset voltage in this differential amplifier of 15 mV to insure that the output voltage will be zero when the reference voltage is zero. Without R_{OS} , the output voltage could be a few millivolts above zero due to the inherent offset. Since the load resistor is so large in this stage compared with the load (Q9) it will be more instructive to look at the gain on a transconductance basis rather than voltage gain. Transconductance of the differential stage is defined for small signals as:

$$g_m = \frac{1}{2r_e + R_E} \quad (1)$$

where

$$r_e \approx \frac{0.026}{I_E} \text{ and}$$

R_E = added emitter degenerating resistance.

For $I_E = 0.5 \text{ mA}$,

$$g_m = \frac{1}{104 + 30} = \frac{1}{134} = 7.5 \text{ mA/volt.} \quad (2)$$

FIGURE 9 – VOLTAGE CONTROL AMPLIFIER

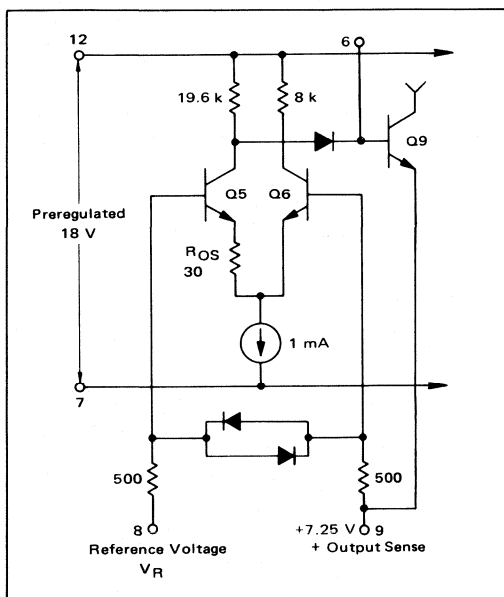
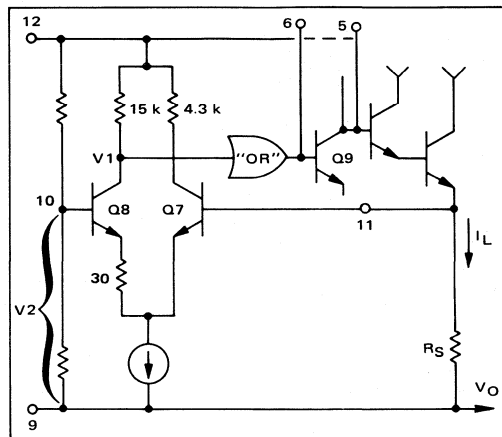


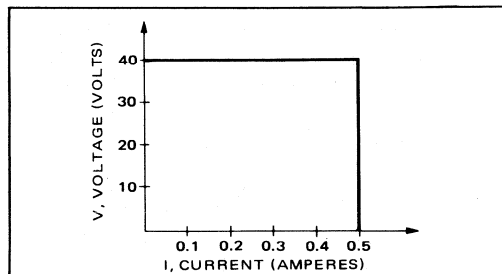
FIGURE 10 – CURRENT CONTROL CIRCUIT



This level is further boosted by the output stage such that in the constant voltage mode overall transconductance is about 300 mA/volt.

A second differential stage nearly identical to the first stage, serves as the current control amplifier (Figure 10). The gain of this stage insures a rapid crossover from the constant voltage to constant current modes and provides a convenient point to control the maximum deliverable load current. In use, a reference voltage derived from the preregulator and a voltage divider is applied to pin 10 while the output current is sampled across R_S by pin 11. When $I_L R_S$ is 15 mV below the reference value, voltage V_1 begins to rapidly rise, eventually gaining complete control of Q9 and limiting output current to a value of V_2/R_S . If V_2 is derived from a variable source, short circuit current may be controlled over the complete output current capability of the regulator. Since the constant-voltage to constant-current change-over requires only a few millivolts the voltage regulation maintains its quality to the current limit and accordingly shows a very sharp "knee" (1% +1 mA, Figure 11). Note that the regulator can switch back into the constant voltage mode if the output voltage reaches a value greater than V_R . Operation through zero milliamperes is guaranteed by the inclusion of another emitter offsetting resistor.

FIGURE 11 – V_1 CURVE FOR 0-TO-40 V, 0.5-AMPERE REGULATOR



MC1566L, MC1466L (continued)

Transistor Q9 and five diodes comprise the essential parts of the output stage (Figure 12). The diodes perform an "OR" function which allows only one mode of operation at a time - constant current or constant voltage. However, an additional stage (Q9) must be included to invert the logic and make it compatible with the driving requirements of series pass transistors as well as provide additional gain. A 1.5 mA collector current source sets the maximum deliverable output current and boosts the output impedance to that of the current source.

Note that the negative (substrate) side of the MC1566/MC1466 is 7.25 volts lower than the output voltage, and the reference regulator guarantees that the positive side is 11 volts above the output. Thus the IC remains at a voltage (relative to ground) solely dependent on the output, "floating" above and below V_O . V_{CE} across Q9 is only two or three V_{BE} 's depending on the number of transistors used in the series pass configuration.

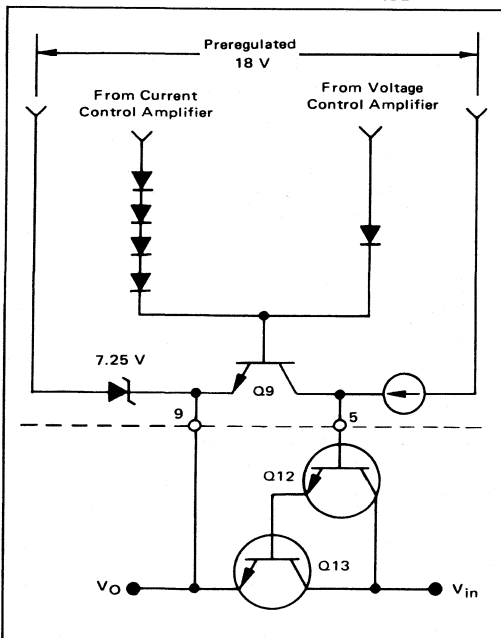
Performance characteristics of the regulator may be approximately calculated for a given circuit (Figure 2). Assuming that the two added transistors (Q12 and Q13) have minimum beta's of 20, then the overall regulator transconductance will be:

$$g_{mT} = (400) 300 \text{ mA/volt} = 120 \text{ A/volt.} \quad (3)$$

For a change in current of 500 mA the output voltage will drop only:

$$\Delta V = \frac{0.5}{120} = 4.2 \text{ mV.} \quad (4)$$

FIGURE 12 - MC1566 OUTPUT STAGE



The analysis thus far does not consider changes in V_R due to output current changes. If I_L increases by 500 mA the collector current of Q9 decreases by 1.25 mA, causing the collector current of Q5 to increase by 30 μA . Accordingly, I_R will be decreased by $\approx 0.30 \mu\text{A}$ which will drop the output by 0.03%. This figure may be improved considerably by either using high beta devices as the pass transistors, or by increasing I_R . Note again, however, that the maximum power rating of the package must be kept in mind. For example if $I_R = 4 \text{ mA}$, power dissipation is

$$P_D = 20 \text{ V} (8 \text{ mA}) + (11 \text{ V} \times 3 \text{ mA}) = 193 \text{ mW.} \quad (5)$$

This indicates that the circuit may be safely operated up to 118°C using 20 volts at the auxiliary supply voltage. If, however, the auxiliary supply voltage is 35 volts,

$$P_D = 35 \text{ V} (8 \text{ mA}) + 26 \text{ V} (3 \text{ mA}) = 358 \text{ mW.} \quad (6)$$

which dictates that the maximum operating temperature must be less than 91°C to keep package dissipation within specified limits.

Line voltage regulation is also a function of the voltage change between pins 8 and 9, and the change of V_{ref} . In this case, however, these voltages change due to changes in the internal regulator's voltages, which in turn are caused by changes in V_{aux} . Note that line voltage regulation is not a function of V_{in} . Note also that the instantaneous value of V_{aux} must always be between 20 and 35 volts.

Figure 6 shows six external diodes (CR1 to CR6) added for protective purposes. CR1 should be used if the output voltage is less than 20 volts and CR2, CR3 are absent. For V_O higher than 20 volts, CR1 should be discarded in favor of CR2 and CR3. Diode CR4 prevents IC failure if the series pass transistors develop collector-base shorts while the main power transistor suffers a simultaneous open emitter. If the possibility of such a transistor failure mode seems remote, CR4 may be deleted. To prevent instantaneous differential and common-mode breakdown of the current sense amplifier, CR5 must be placed across the current limit resistor R_S .

Load transients occasionally produce a damaging reversal of current flow from output to input $V_O > 150$ volts (which will destroy the IC). Diode CR6 prevents such reversal and renders the circuit immune from destruction for such conditions, e.g., adding a large output capacitor after the supply is turned "on". Diodes CR1, CR2, CR3, and CR5 may be general purpose silicon units such as 1N4001 or equivalent whereas CR4 and CR6 should have a peak inverse voltage rating equal to V_{in} or greater.

APPLICATIONS

Figure 2 shows a typical 0-to-40 volts, 0.5-ampere regulator with better than 0.01% performance. The RC network between pins 5 and 6 and the capacitor between pins 13 and 14 provide frequency compensation for the MC1566/MC1466. The external pass transistors are used to boost load current, since the output current of the regulator is less than 2 mA.

MC1566L, MC1466L (continued)

Figure 1 is a 0-to-15 volts, 10-ampere regulator with the pass transistor configuration necessary to boost the load current to 10 amperes. Note that C_O has been increased to 1000 μF following the general rule:

$$C_O = 100 \mu\text{F/A } I_L$$

The prime advantage of the MC1566/MC1466 is its use as a high voltage regulator, as shown in Figure 3. This 0-to-250 volts 0.1-ampere regulator is typical of high voltage applications, limited only by the breakdown and safe areas of the output pass transistors.

The primary limiting factor in high voltage series regulators is the pass transistor. Figure 13 shows a safe area curve for the MJ413. Looking at Figure 3, we see that if the output is shorted, the transistor will have a collector current of 100 mA, with a V_{CE} approximately equal to 260 volts. Thus this point falls on the dc line of the safe area curve, insuring that the transistor will not enter secondary breakdown.

In this respect (Safe Operating Area) the foldback circuit of Figure 14 is superior for handling high voltages and yet is short-circuit protected. This is due to the fact that load current is diminished as output voltage drops (V_{CE} increases as V_O drops) as seen in Figure 15. By careful design the load current at a short, I_{SC} can be made low enough such that the combined V_{CE} (V_{in}) and I_{SC} still falls within the dc safe operating area of the transistor. For the illustrated design (Figure 14), an input voltage of 210 volts is com-

patible with a short-circuit current of 100 mA. Yet current foldback allows us to design for a maximum regulated load current of 500 mA. The pertinent design equations are:

$$\text{Let } R_2 \text{ (k}\Omega\text{)} = V_O$$

$$\alpha = \frac{0.25}{V_O} \left[\frac{I_k}{I_{SC}} - 1 \right]$$

$$R_1 \text{ (k}\Omega\text{)} = \frac{\alpha}{1 - \alpha} V_O$$

$$R_{SC} = \frac{0.25}{(1 - \alpha) I_{SC}}$$

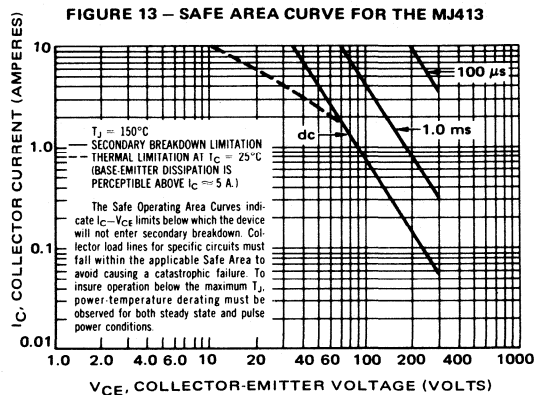
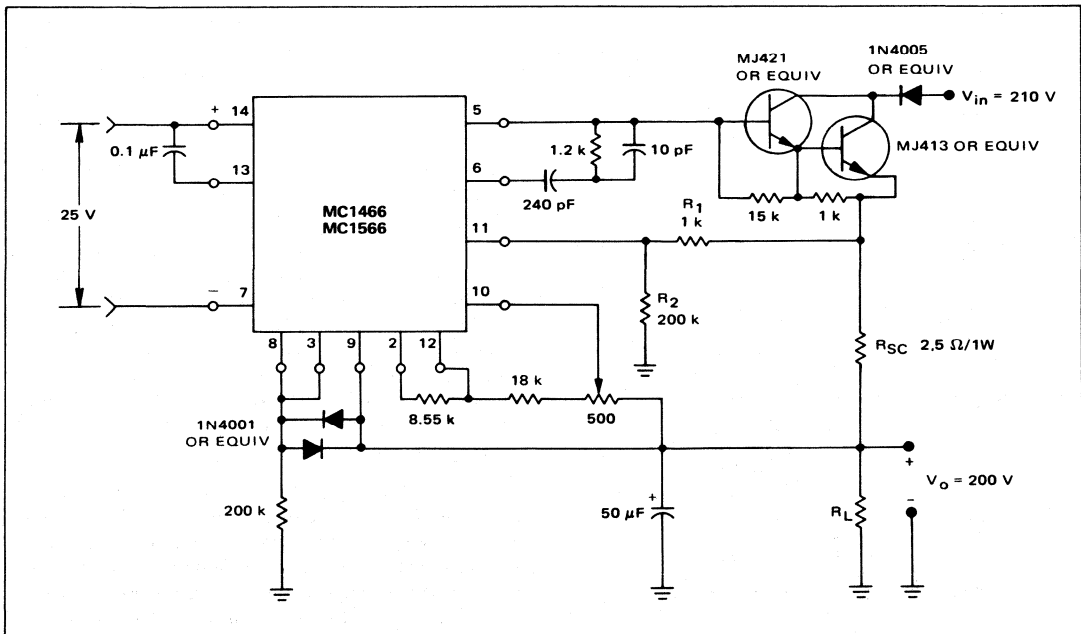


FIGURE 14 — A 200 V, 0.5-AMPERE REGULATOR WITH CURRENT FOLDBACK



MC1566L, MC1466L (continued)

The terms I_{SC} and I_K correspond to the short-circuit current and maximum available load current as shown in Figure 15.

FIGURE 15 – TYPICAL FOLDBACK PERFORMANCE

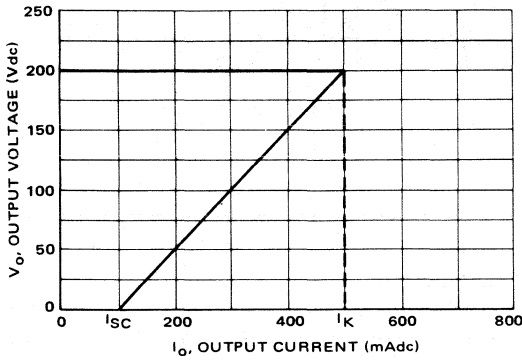


Figure 16 shows a remote sense application which should be used when high current or long wire lengths are used. This type of wiring is recommended for any application where the best possible regulation is desired. Since the sense lines draw only a small current, large voltage drops do not destroy the excellent regulation of the MC1566/MC1466.

TRANSIENT FAILURES

In industrial areas where electrical machinery is used the normal ac line often contains bursts of voltage running

from hundreds to thousands of volts in magnitude and only microseconds in duration. Under some conditions this energy is dissipated across the internal zener connected between pins 9 and 7. This transient condition may produce a total failure of the regulator device without any apparent explanation. This type of failure is identified by absence of the 7-volt zener (CR1) between pin 9 and pin 7. To prevent this failure mode, two solutions have been successfully applied. The first method involves the use of an external zener and resistor that shunt more of the transient energy around the IC (Figure 17). The second method is a transient suppression network consisting of capacitors that equalize high frequency components across both the auxiliary and main supply. Figure 18 illustrates the use of five capacitors for the full wave rectified main supply and Figure 19 uses six capacitors when a full wave bridge is used.

VOLTAGE/CURRENT – MODE INDICATOR

There may be times when it is desirable to know when the MC1566/MC1466 is in the constant current mode or constant voltage mode. A mode indicator can be easily added to provide this feature. Figure 20 shows how a PNP transistor has replaced a protection diode between pins 8 and 9 of Figure 2. When the MC1566/MC1466 goes from constant voltage mode to constant current mode, V_o will drop below V_g and the PNP transistor will turn on. The 1-mA current supplied by pin 8 will now be shunted to ground through R_1 in parallel with R_2 , which provides a control voltage, V_C . This voltage V_C can then control a Schmitt trigger which drives front panel lamps to indicate “constant current” or “constant voltage.”

FIGURE 16 – REMOTE SENSE

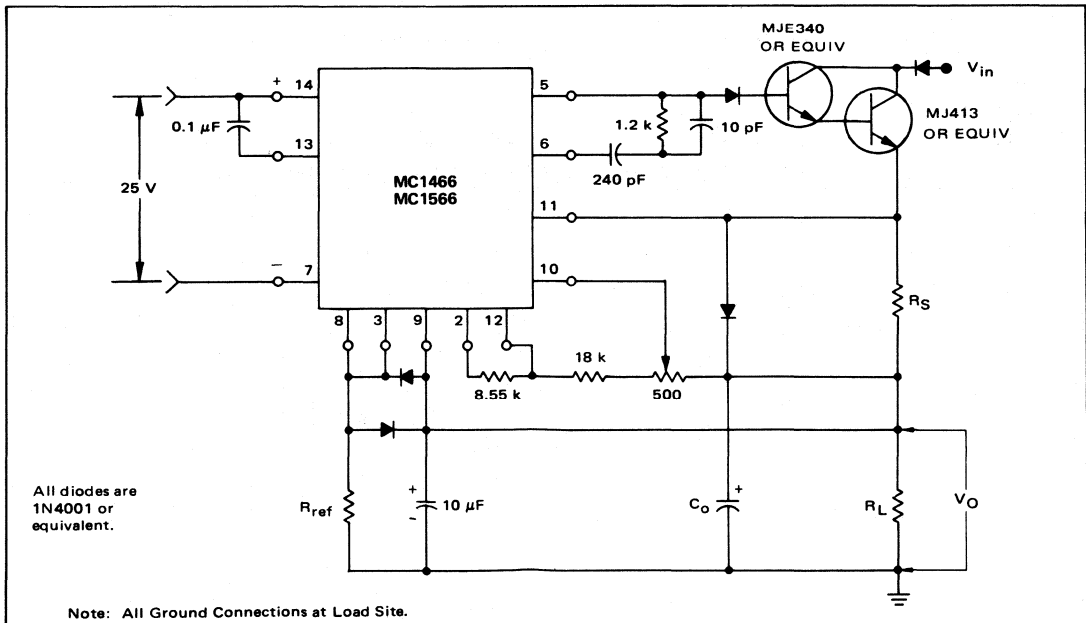


FIGURE 17 – A 0-TO-250 VOLT, 0.1-AMPERE REGULATOR

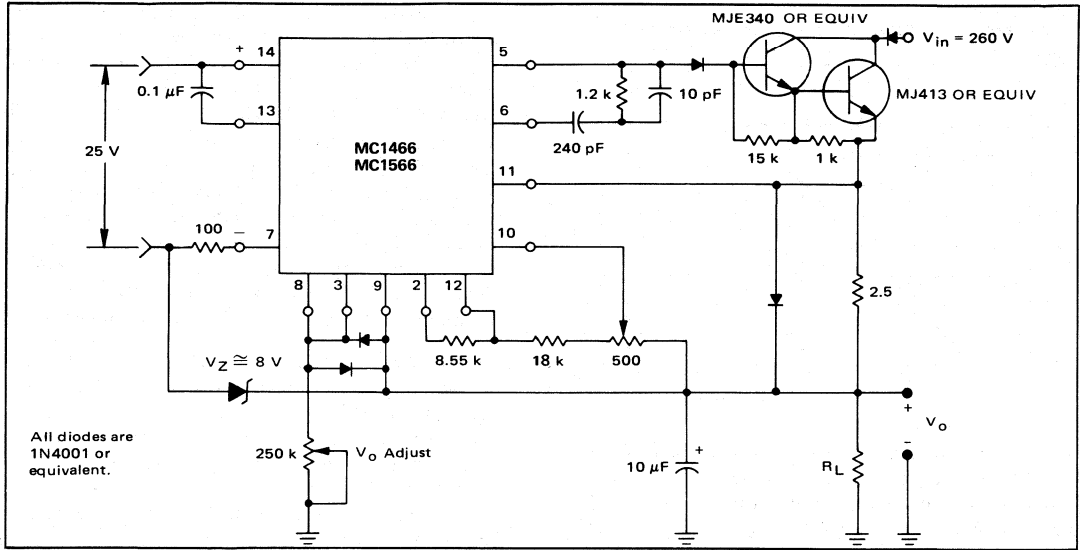


FIGURE 18 – HALF-WAVE RECTIFIER WITH TRANSIENT SUPPRESSION

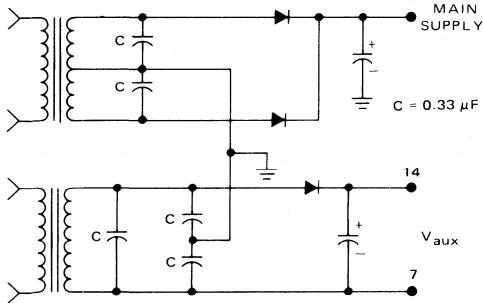


FIGURE 19 – FULL-WAVE RECTIFICATION WITH TRANSIENT SUPPRESSION

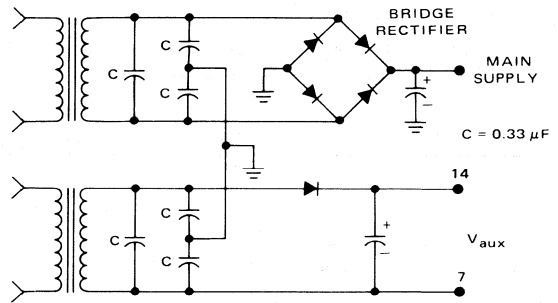
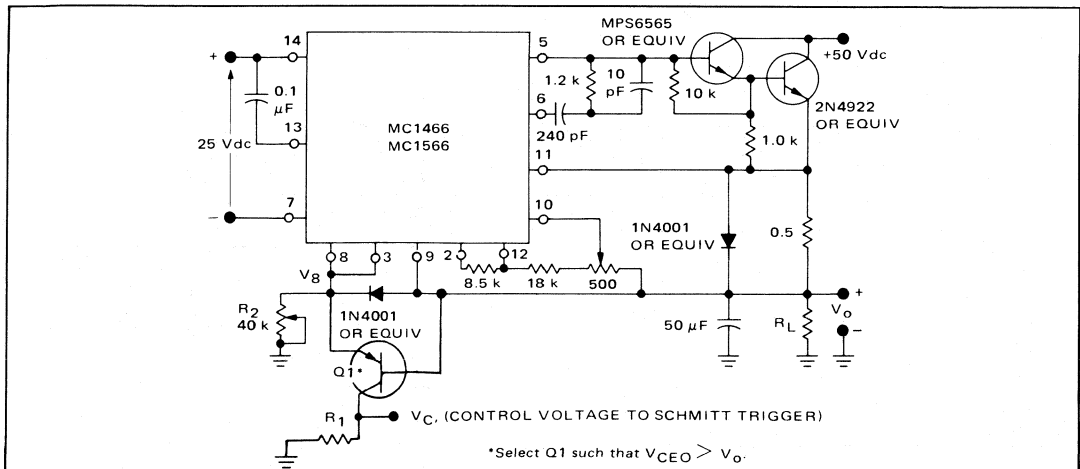


FIGURE 20 – 0-TO-40 Vdc, 0.5-AMPERE REGULATOR WITH MODE INDICATOR



MC1568 MC1468

DUAL VOLTAGE REGULATORS

DUAL ± 15 -VOLT REGULATOR

The MC1568/MC1468 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100 mA. Internally, the device is set for ± 15 -volt outputs but a single external adjustment can be used to change both outputs simultaneously from 14.5 to 20 volts. Input voltages up to ± 30 volts can be used and there is provision for adjustable current limiting. The device is available in three package types to accommodate various power requirements.

- Internally set to ± 15 V Tracking Outputs
- Output Currents to 100 mA
- Outputs Balanced to within 1% (MC1568)
- Line and Load Regulation of 0.06%
- 1% Maximum Output Variation due to Temperature Changes
- Standby Current Drain of 3.0 mA
- Externally Adjustable Current Limit
- Remote Sensing Provisions
- Case is at Ground Potential (R suffix package)

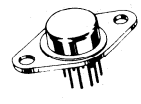
DUAL ± 15 -VOLT TRACKING REGULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



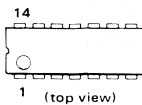
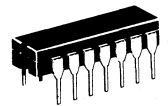
(bottom view)

CASE 603-3
METAL PACKAGE
G SUFFIX

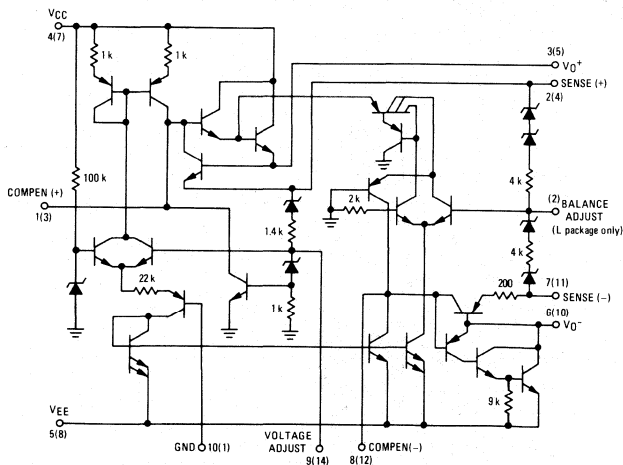


CASE 614
METAL PACKAGE
R SUFFIX

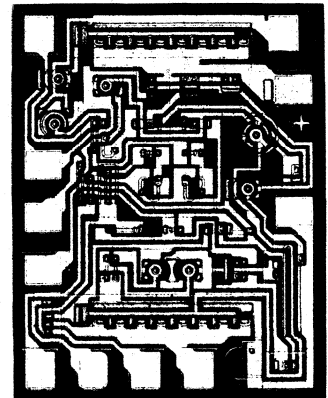
CASE 632
CERAMIC PACKAGE
TO-116
L SUFFIX



(top view)



Pin numbers adjacent to terminals are for the G and R suffix packages only. Pin numbers in parentheses are for the L suffix package only. Pin 10 is ground for the G suffix package only. For the R package, the case is ground.



MC1568, MC1468 (continued)

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

| Rating | Symbol | Value | | | Unit |
|--|--|------------------|------------------|------------------|------------------------|
| Input Voltage | V _{CC} , V _{EE} | 30 | | | Vdc |
| Peak Load Current | I _{PK} | 100 | | | mA |
| Power Dissipation and Thermal Characteristics T _A = +25°C Derate above T _A = +25°C Thermal Resistance, Junction to Air T _C = +25°C Derate above T _C = +25°C Thermal Resistance, Junction to Case | P _D 1/θ _{JA} θ _{JA} | G Package | R Package | L Package | Watts mW/°C °C/W |
| | | 0.8 | 2.4 | 1.0 | |
| | | 5.4 | 16 | 6.7 | |
| | P _D 1/θ _{JC} θ _{JC} | 185 | 62 | 150 | Watts mW/°C °C/W |
| | | 2.1 | 9.0 | 2.5 | |
| | | 14 | 61 | 20 | |
| 70 | 17 | 50 | | | |
| Storage Junction Temperature Range | T _J , T _{stg} | -65 to +175 | | | °C |
| Minimum Short-Circuit Resistance | R _{SC} (min) | 4.0 | | | Ohms |

OPERATING TEMPERATURE RANGE

| Ambient Temperature | T _A | °C |
|---------------------|-------------------------|----|
| MC1468 MC1568 | 0 to +75 -55 to +125 | |

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 V, V_{EE} = -20 V, C1 = C2 = 1500 pF, C3 = C4 = 1.0 μF, R_{SC}⁺ = R_{SC}⁻ = 4.0 Ω, I_L⁺ = I_L⁻ = 0, T_C = +25°C unless otherwise noted.) (See Figure 1.)

| Characteristic | Symbol* | MC1568 | | | MC1468 | | | Unit |
|--|----------------------------------|--------|-----|------|--------|-----|------|---------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage | V _O | 14.8 | 15 | 15.2 | 14.5 | 15 | 15.5 | Vdc |
| Input Voltage | V _{in} | - | - | 30 | - | - | 30 | Vdc |
| Input-Output Voltage Differential | V _{in} - V _O | 2.0 | - | - | 2.0 | - | - | Vdc |
| Output Voltage Balance | V _{Bal} | - | ±50 | ±150 | - | ±50 | ±300 | mV |
| Line Regulation Voltage (V _{in} = 18 V to 30 V) (T _{low} ^① to T _{high} ^②) | Reg _{in} | - | - | 10 | - | - | 10 | mV |
| | | - | - | 20 | - | - | 20 | |
| Load Regulation Voltage (I _L = 0 to 50 mA, T _J = constant) (T _A = T _{low} to T _{high}) | Reg _L | - | - | 10 | - | - | 10 | mV |
| | | - | - | 30 | - | - | 30 | |
| Output Voltage Range (See Figures 2 and 12) | V _{OR} | 14.5 | - | 20 | 14.5 | - | 20 | Vdc |
| Ripple Rejection (f = 120 Hz) | RR | - | 75 | - | - | 75 | - | dB |
| Output Voltage Temperature Stability (T _{low} to T _{high}) | TSV _O | - | 0.3 | 1.0 | - | 0.3 | 1.0 | % |
| Short-Circuit Current Limit (R _{SC} = 10 ohms) | I _{SC} | - | 60 | - | - | 60 | - | mA |
| Output Noise Voltage (BW = 100 Hz - 10 kHz) | V _N | - | 100 | - | - | 100 | - | μV(RMS) |
| Positive Standby Current (V _{in} = +30 V) | I _B ⁺ | - | 2.4 | 4.0 | - | 2.4 | 4.0 | mA |
| Negative Standby Current (V _{in} = -30 V) | I _B ⁻ | - | 1.0 | 3.0 | - | 1.0 | 3.0 | mA |
| Long-Term Stability | ΔV _O /Δt | - | 0.2 | - | - | 0.2 | - | %/k Hr |

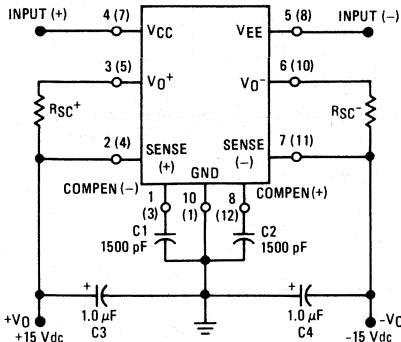
① T_{low} = 0°C for MC1468
= -55°C for MC1568

② T_{high} = +75°C for MC1468
= +125°C for MC1568

*Symbols conform to JEDEC Engineering
Bulletin No. 1 when applicable.

TYPICAL APPLICATIONS

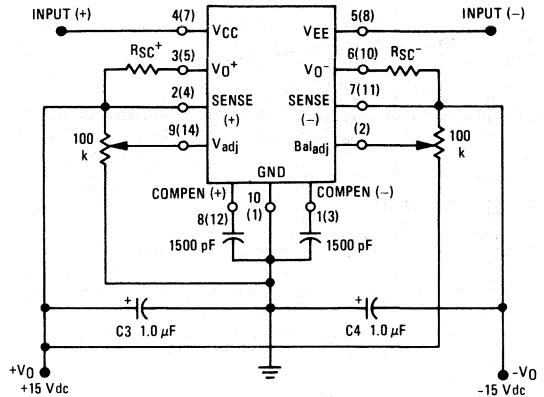
FIGURE 1 - BASIC 50-mA REGULATOR



C1 and C2 should be located as close to the device as possible. A 0.1 μF ceramic capacitor may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors.

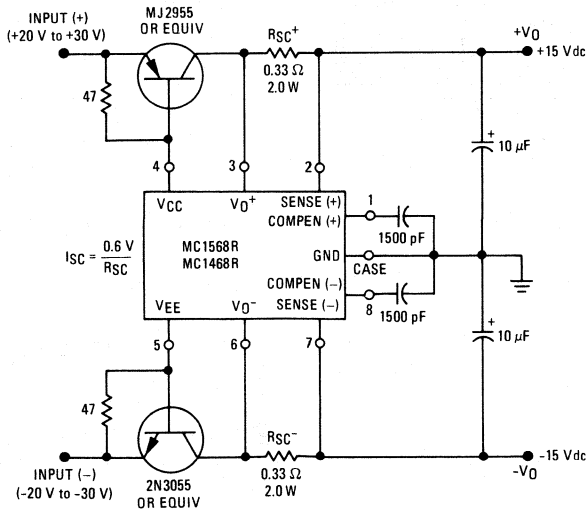
C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation, it may be necessary to bypass C4 with a 0.1 μF ceramic disc capacitor.

FIGURE 2 - VOLTAGE ADJUST AND BALANCE ADJUST CIRCUIT



Balance adjust available in MC1568L, MC1468L ceramic dual in-line package only.

FIGURE 3 - ±1.5-AMPERE REGULATOR (Short-Circuit Protected, with Proper Heatsinking)



$$I_{SC} = \frac{0.6 \text{ V}}{R_{SC}}$$

TYPICAL CHARACTERISTICS

($V_{CC} = +20\text{ V}$, $V_{EE} = -20\text{ V}$, $V_O = \pm 15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 4 – LOAD REGULATION

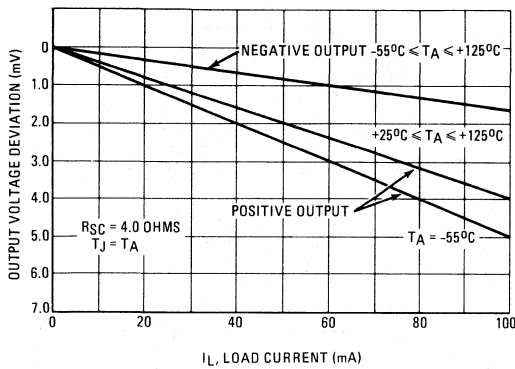


FIGURE 5 – REGULATOR DROPOUT VOLTAGE

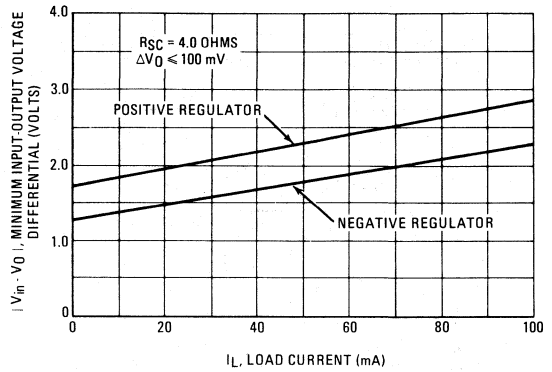


FIGURE 6 – MAXIMUM CURRENT CAPABILITY

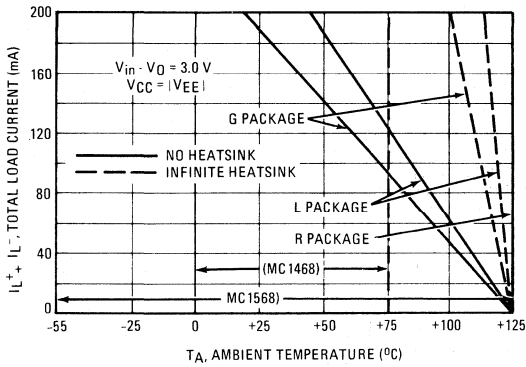


FIGURE 7 – MAXIMUM CURRENT CAPABILITY

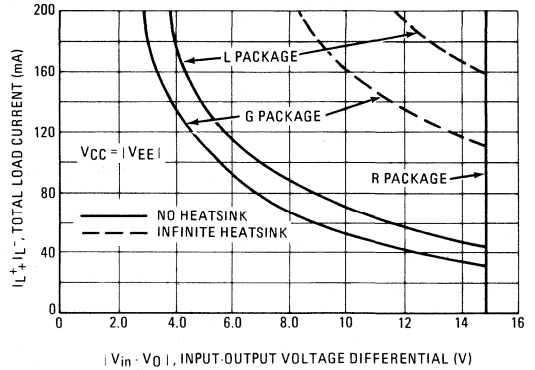


FIGURE 8 – I_{SC} versus R_{SC}

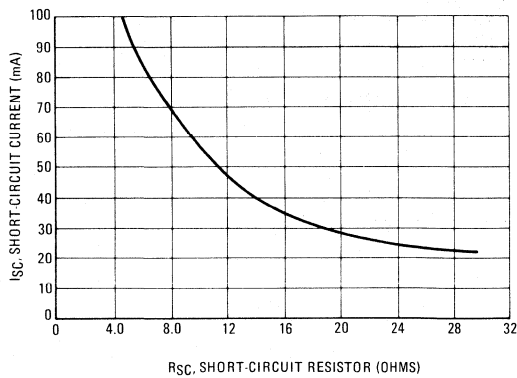
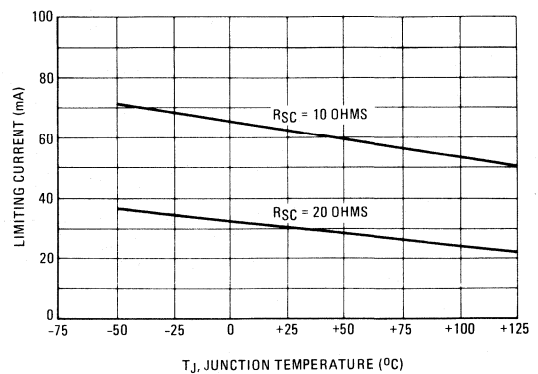


FIGURE 9 – CURRENT-LIMITING CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)
 ($V_{CC} = +20\text{ V}$, $V_{EE} = -20\text{ V}$, $V_O = \pm 15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 10 – STANDBY CURRENT DRAIN

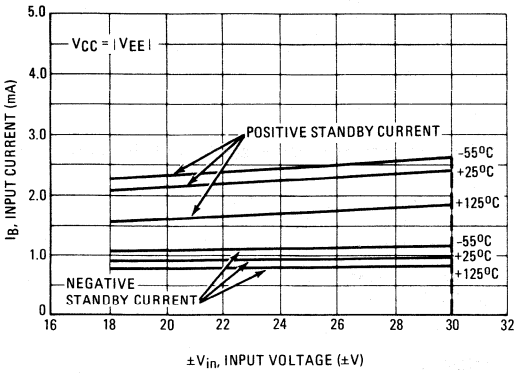


FIGURE 11 – STANDBY CURRENT DRAIN

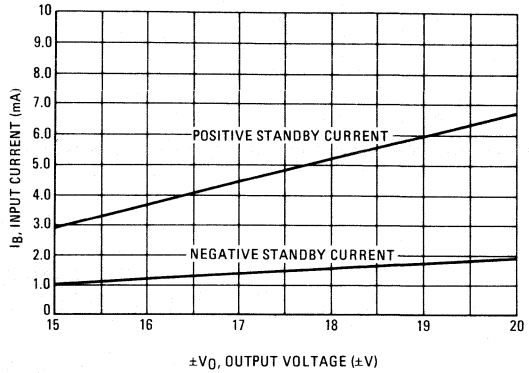


FIGURE 12 – TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE

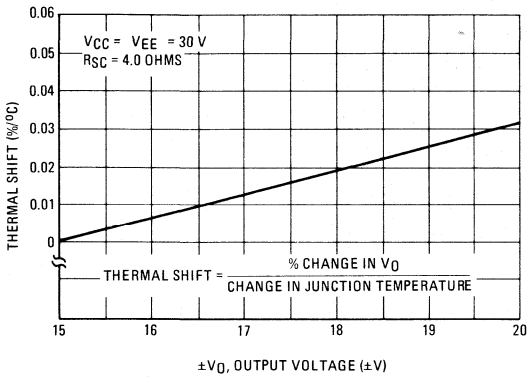


FIGURE 13 – LOAD TRANSIENT RESPONSE

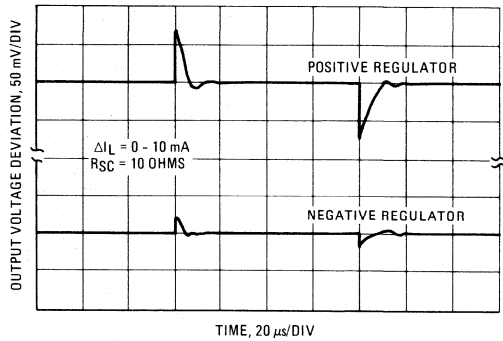


FIGURE 14 – LINE TRANSIENT RESPONSE

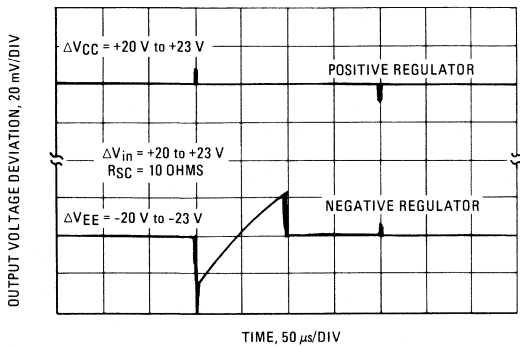
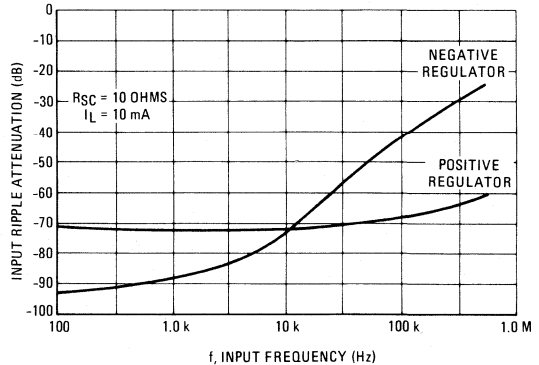


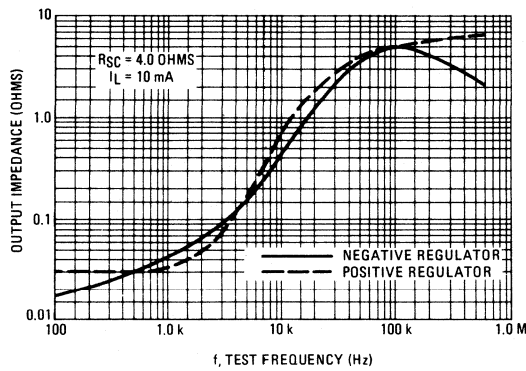
FIGURE 15 – RIPPLE REJECTION



TYPICAL CHARACTERISTICS (continued)

($V_{CC} = +20\text{ V}$, $V_{EE} = -20\text{ V}$, $V_O = \pm 15\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 16 – OUTPUT IMPEDANCE



POSITIVE VOLTAGE REGULATORS

MC1569 MC1469

Specifications and Applications Information

MONOLITHIC VOLTAGE REGULATOR

The MC1569/MC1469 is a positive voltage regulator designed to deliver continuous load current up to 500 mAdc. Output voltage is adjustable from 2.5 Vdc to 37 Vdc. The MC1569 is specified for use within the military temperature range (-55 to +125°C) and the MC1469 within the 0 to +70°C temperature range.

For systems requiring a positive regulated voltage, the MC1569 can be used with performance nearly identical to the MC1563 negative voltage regulator. Systems requiring both a positive and negative regulated voltage can use the MC1569 and MC1563 as complementary regulators with a common input ground.

- Electronic "Shut-Down" Control
- Excellent Load Regulation (Low Output Impedance - 20 milliohms typ)
- High Power Capability: up to 17.5 Watts
- Excellent Temperature Stability: $\pm 0.002\% / ^\circ\text{C}$ typ
- High Ripple Rejection: 0.002 %/V typ

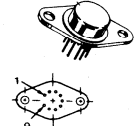
POSITIVE VOLTAGE REGULATOR INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED



(Bottom View)

CASE 602A
METAL PACKAGE
G SUFFIX



CASE 614
METAL PACKAGE
R SUFFIX

FIGURE 1 - TYPICAL CIRCUIT CONNECTION
($3.5 \leq V_O \leq 37$ Vdc, $1 \leq I_L \leq 500$ mA)

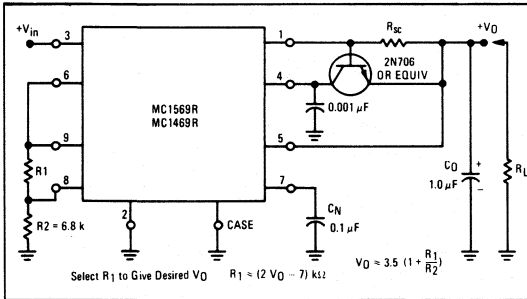


FIGURE 2 - TYPICAL NPN CURRENT BOOST CONNECTION
($V_O = 5.0$ Vdc, $I_L = 10$ Adc [max])

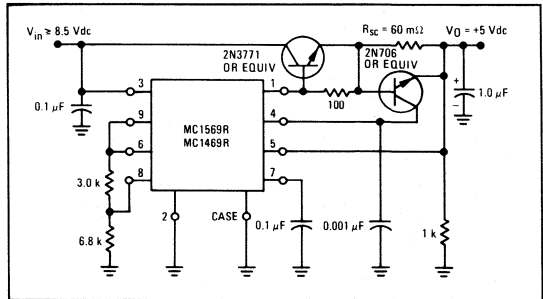
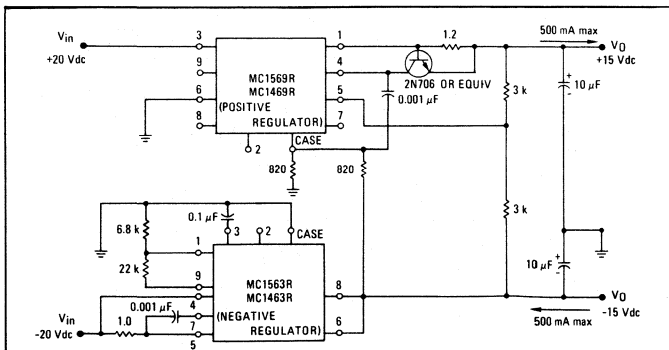
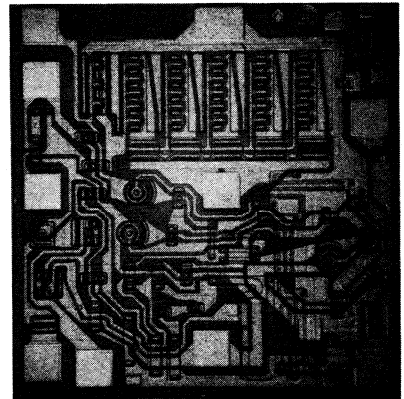


FIGURE 3 - ± 15 V, ± 400 mA COMPLEMENTARY TRACKING
VOLTAGE REGULATOR



The index to the content of this data sheet appears on page 20.
See current MCC1569/1469 data sheet for standard linear chip information.
See Packaging Information Section for outline dimensions.



MC1569, MC1469 (continued)

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

| Rating | Symbol | Value | | Unit | |
|---|--------------------------------------|-------------------|-----------|------|-------|
| Input Voltage MC1469 MC1569 | V _{in} | 35 40 | | Vdc | |
| Peak Load Current | I _{PK} | G Package | R Package | mA | |
| | | 250 | 600 | | |
| Current, Pin 2 | I _{pin 2} | 10 | 10 | mA | |
| Current, Pin 9 | I _{pin 9} | 5.0 | 5.0 | | |
| Power Dissipation and Thermal Characteristics | T _A = +25°C | P _D | 0.68 | 3.0 | Watts |
| | Derate above T _A = +25°C | 1/θ _{JA} | 5.44 | 24 | mW/°C |
| | Thermal Resistance, Junction to Air | θ _{JA} | 184 | 41.6 | °C/W |
| | T _C = +25°C | P _D | 1.8 | 17.5 | Watts |
| | Derate above T _C = +25°C | 1/θ _{JC} | 14.4 | 140 | mW/°C |
| | Thermal Resistance, Junction to Case | θ _{JC} | 69.4 | 7.15 | °C/W |
| Operating and Storage Junction Temperature | T _J , T _{stg} | -65 to +150 | | °C | |

OPERATING TEMPERATURE RANGE

| Ambient Temperature | T _A | °C |
|---------------------|----------------|-------------------------|
| MC1469 MC1569 | | 0 to +75 -55 to +125 |

ELECTRICAL CHARACTERISTICS

(T_C = +25°C unless otherwise noted) (Load Current = 100 mA for "R" Package device, unless otherwise noted)
= 10 mA for "G" Package device,

| Characteristic | Fig. | Note | Symbol * | MC1569 | | | MC1469 | | | Unit |
|---|------|------|----------------------------------|------------|----------------------|---------------------|------------|----------------------|---------------------|------------------|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage (T _A = T _{low} ① to T _{high} ②) | 4 | 1 | V _{in} | 8.5 | — | 40 | 9.0 | — | 35 | Vdc |
| Output Voltage Range | 4,5 | | V _O | 2.5 | — | 37 | 2.5 | — | 32 | Vdc |
| Reference Voltage (Pin 8 to Ground) | 4 | | V _{ref} | 3.4 | 3.5 | 3.6 | 3.2 | 3.5 | 3.8 | Vdc |
| Minimum Input-Output Voltage Differential (R _{sc} = 0) | 4 | 2 | V _{in} - V _O | — | 2.1 | 2.7 | — | 2.1 | 3.0 | Vdc |
| Bias Current (I _L = 1.0 mAdc, R ₂ = 6.8 k ohms, I _{IB} = I _{in} · I _L) | 4 | | I _{IB} | — | 4.0 | 9.0 | — | 5.0 | 12 | mAdc |
| Output Noise (C _N = 0.1 μF, f = 10 Hz to 5.0 MHz) | 4 | | v _N | — | 0.150 | — | — | 0.150 | — | mV (rms) |
| Temperature Coefficient of Output Voltage | 4 | 3 | TCV _O | — | ±0.002 | — | — | ±0.002 | — | %/°C |
| Operating Load Current Range (R _{sc} ≤ 0.3 ohms) R Package (R _{sc} ≤ 2.0 ohms) G Package | 4 | | I _L | 1.0 1.0 | — | 500 200 | 1.0 1.0 | — | 500 200 | mAdc |
| Input Regulation | 6 | 4 | Reg _{in} | — | 0.002 | 0.015 | — | 0.003 | 0.030 | %/V _O |
| Load Regulation (T _J = Constant [1.0 mA ≤ I _L ≤ 20 mA]) (T _C = +25°C [1.0 mA ≤ I _L ≤ 50 mA]) R Package G Package | 7 | 5 | Reg _{load} | — | 0.4 0.005 0.01 | 1.6 0.05 0.13 | — | 0.7 0.005 0.01 | 2.4 0.05 0.13 | mV % |
| Output Impedance (C _c = 0.001 μF, R _{sc} = 1.0 ohm, f = 1.0 kHz, V _{in} = +14 Vdc, V _O = +10 Vdc) | 8 | 6 | z _O | — | 20 | 80 | — | 35 | 120 | milliohms |
| Shutdown Current (V _{in} = +35 Vdc) | 9 | | I _{sd} | — | 70 | 150 | — | 140 | 500 | μAdc |

① T_{low} = 0°C for MC1469
= -55°C for MC1569

② T_{high} = +75°C for MC1469
= +125°C for MC1569

*Symbols conform to JEDEC Engineering Bulletin No. 1
when applicable.

Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode. For output voltages greater than approximately 5.5 Vdc the minimum "total instantaneous input voltage" must increase to the extent that it will always exceed the output voltage by at least the "input-output voltage differential".

Note 2. This parameter states that the MC1569/MC1469 will regulate properly with the input-output voltage differential ($V_{in} - V_O$) as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with ($V_{in} - V_O$) as low as 2.1 Vdc as shown in the typical column. (See Figure 21.)

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$MC1569, TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min}) (100)}{(180^\circ\text{C}) (V_O @ 25^\circ\text{C})} = \%/^\circ\text{C}$$

$$MC1469, TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min}) (100)}{(75^\circ\text{C}) (V_O @ 25^\circ\text{C})} = \%/^\circ\text{C}$$

The output-voltage adjusting resistors (R1 and R2) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. Input regulation is the percentage change in output

voltage per volt change in the input voltage and is expressed as

$$\text{Input Regulation} = \frac{v_O}{V_O (v_{in})} 100 (\%/V_O),$$

where v_O is the change in the output voltage V_O for the input change v_{in} .

The following example illustrates how to compute maximum output voltage change for the conditions given:

$$\begin{aligned} \text{Reg}_{in} &= 0.015 \%/V_O \\ V_O &= 10 \text{ Vdc} \\ v_{in} &= 1.0 \text{ V(rms)} \\ v_O &= \frac{(\text{Reg}_{in}) (v_{in}) (V_O)}{100} \\ &= \frac{(0.015) (1.0) (10)}{100} \\ &= 0.0015 \text{ V(rms)} \end{aligned}$$

Note 5. Load regulation is specified for small ($\leq 17^\circ\text{C}$) changes in junction temperature. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{[V_O]_{I_L = 1.0 \text{ mA}} - [V_O]_{I_L = 50 \text{ mA}}}{V_O |_{I_L = 1.0 \text{ mA}}} \times 100$$

TEST CIRCUITS

FIGURE 4 - CONNECTION FOR $V_O \geq 3.5 \text{ Vdc}$

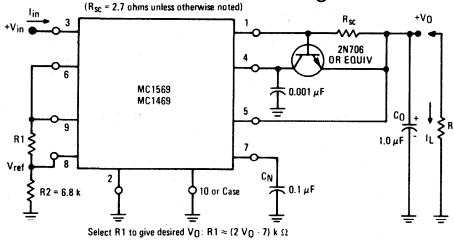


FIGURE 5 - CONNECTION FOR $2.5 \text{ Vdc} \geq V_O \leq 3.5 \text{ Vdc}$

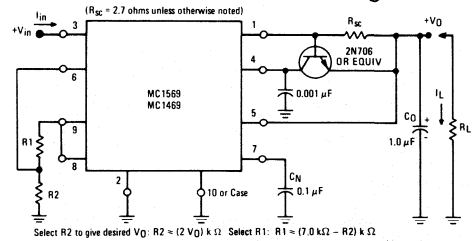


FIGURE 6 - INPUT REGULATION

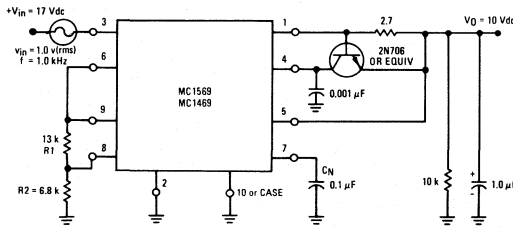


FIGURE 7 - LOAD REGULATION

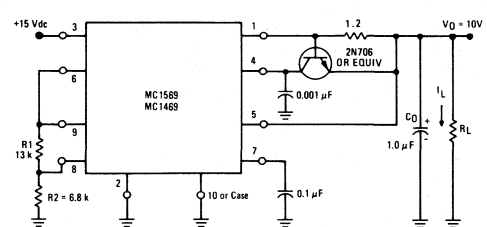


FIGURE 8 - OUTPUT IMPEDANCE

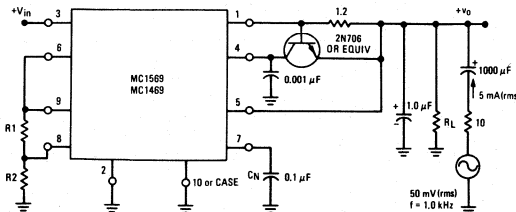
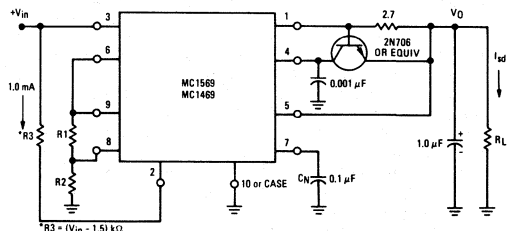


FIGURE 9 - SHUTDOWN CURRENT



GENERAL DESIGN INFORMATION

1. Output Voltage, V_O
 - a) For $V_O \geq 3.5$ Vdc — Output voltage is set by resistors R1 and R2 (see Figure 4). Set R2 = 6.8 k ohms and determine R1 from the graph of Figure 10 or from the equation:

$$R1 \approx (2 V_O - 7) \text{ k}\Omega$$
 - b) For $2.5 \leq V_O \leq 3.5$ Vdc — Output voltage is set by resistors R1 and R2 (see Figure 5). Resistors R1 and R2 can be determined from the graph of Figure 11 or from the equations:

$$R2 \approx 2 (V_O) \text{ k}\Omega$$

$$R1 \approx (7 \text{ k}\Omega - R2) \text{ k}\Omega$$

- c) Output voltage, V_O , is determined by the ratio of R1 and R2, therefore optimum temperature performance can be achieved if R1 and R2 have the same temperature coefficient.
 - d) Output voltage can be varied by making R1 adjustable as shown in Figure 43.
 - e) If $V_O = 3.5$ Vdc (to supply MRTL* for example), tie pins 6, 8 and 9 together. R1 and R2 are not needed in this case.
2. Short Circuit Current, I_{sc}
Short Circuit Current, I_{sc} , is determined by R_{sc} . R_{sc} may be chosen with the aid of Figure 12 or the expression:

$$R_{sc} \approx \frac{0.6 \text{ ohm}}{I_{sc}}$$

where I_{sc} is measured in amperes. This expression is also valid when current is boosted as shown in Figures 2, 29 and 30.

3. Compensation, C_c
A 0.001 μF capacitor, C_c , from pin 4 to ground will provide adequate compensation in most applications, with or without current boost. Smaller values of C_c will reduce stability and larger values of C_c will degrade pulse response and output impedance versus frequency. The physical location of C_c should be close to the MC1569/MC1469 with short lead lengths.
4. Noise Filter Capacitor, C_N
A 0.1 μF capacitor, C_N , from pin 7 to ground will typically reduce the output noise voltage to 150 μV (rms). The value of C_N can be increased or decreased, depending on the noise voltage requirements of a particular application. A minimum value of 0.001 μF is recommended.
5. Output Capacitor, C_O
The value of C_O should be at least 1.0 μF in order to provide good stability. The maximum value recommended is a function of current limit resistor R_{sc} :

$$C_O \text{ max} \approx \frac{250 \mu\text{F}}{R_{sc}}$$

where R_{sc} is measured in ohms. Values of C_O greater than this will degrade the pulse response characteristics and increase the settling time.

6. Shut-Down Control
One method of turning "OFF" the regulator is to apply a dc voltage at pin 2. This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting (see Figures 34, 39 and 40). As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at Pin 2 will cause automatic shut-down for high junction temperatures (see Figure 39). This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard logic levels of MRTL, MDTL or MTTL can also be used to turn the regulator "ON" or "OFF".

7. Remote Sensing

The connection to pin 5 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on z_O can be greatly reduced (see Figure 37).

FIGURE 10 — R1 versus V_O ($V_O \geq 3.5$ Vdc, See Figure 4)

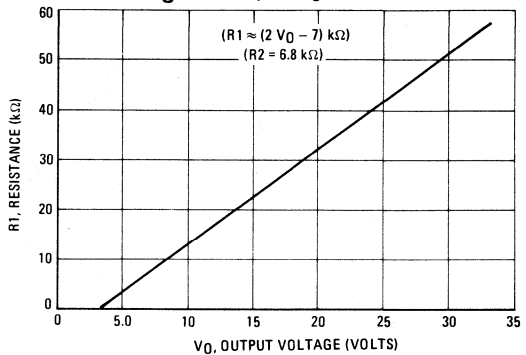


FIGURE 11 — R1 and R2 versus V_O ($2.5 \leq V_O \leq 3.5$ Vdc, See Figure 5)

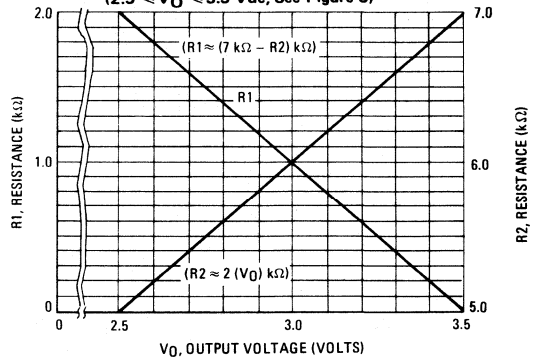
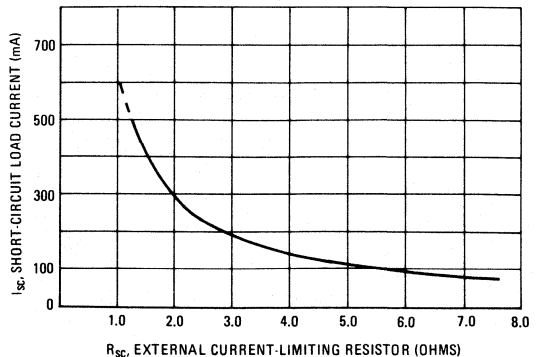


FIGURE 12 — I_{sc} versus R_{sc}



TYPICAL CHARACTERISTICS

Unless otherwise noted: $C_N = 0.1 \mu\text{F}$, $C_C = 0.001 \mu\text{F}$, $C_O = 1.0 \mu\text{F}$, $T_C = +25^\circ\text{C}$,
 $V_{in \text{ nom}} = +9.0 \text{ Vdc}$, $V_O \text{ nom} = +5.0 \text{ Vdc}$,
 $I_L > 200 \text{ mA}$ for R package only.

FIGURE 13 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

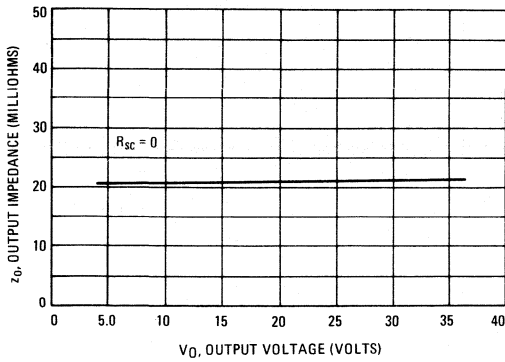


FIGURE 14 – OUTPUT IMPEDANCE versus R_{sc}

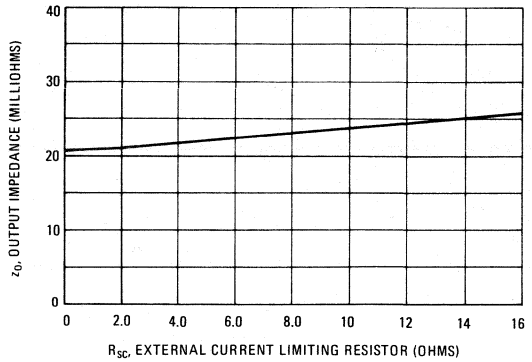


FIGURE 15 – FREQUENCY DEPENDENCE OF INPUT REGULATION, C_O = 10 μF

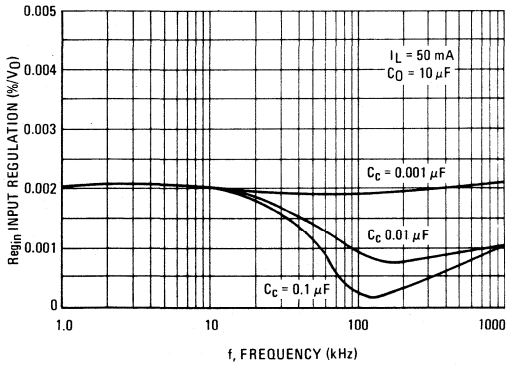


FIGURE 16 – FREQUENCY DEPENDENCE OF INPUT REGULATION, C_O = 2.0 μF

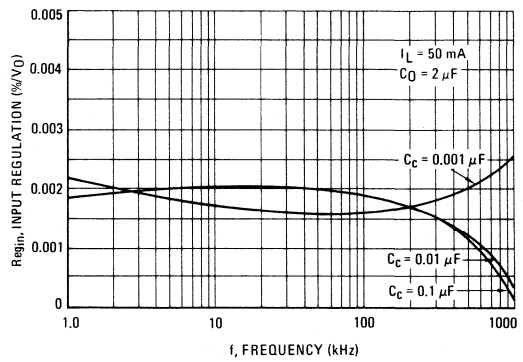


FIGURE 17 – CURRENT-LIMITING CHARACTERISTICS

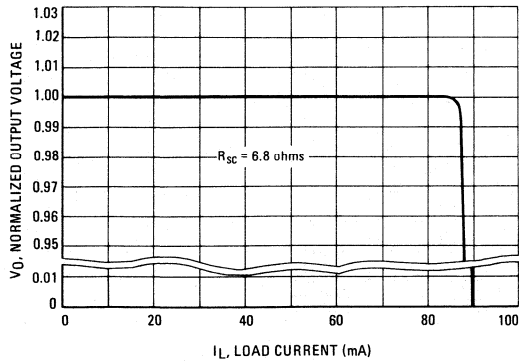
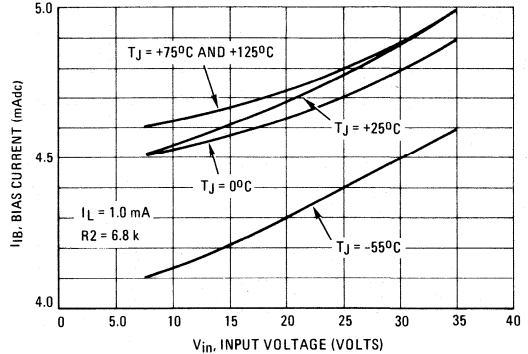


FIGURE 18 – BIAS CURRENT versus INPUT VOLTAGE



TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted: $C_N = 0.1 \mu F$, $C_C = 0.001 \mu F$, $C_O = 1.0 \mu F$, $T_C = +25^\circ C$,
 $V_{in \text{ nom}} = +9.0 \text{ Vdc}$, $V_O \text{ nom} = +5.0 \text{ Vdc}$,
 $I_L > 200 \text{ mA}$ for R package only.

FIGURE 19 – EFFECT OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

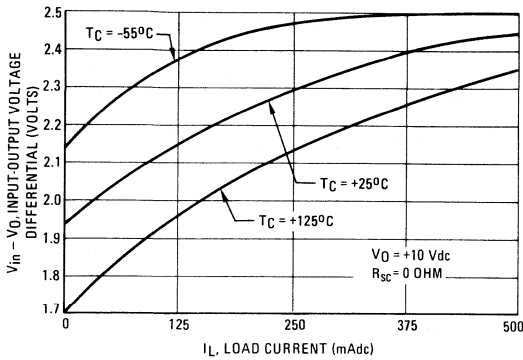


FIGURE 20 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

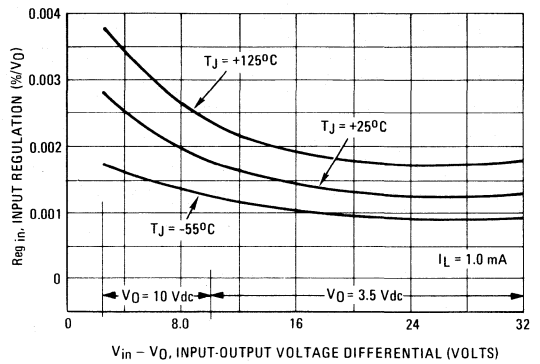


FIGURE 21 – INPUT TRANSIENT RESPONSE

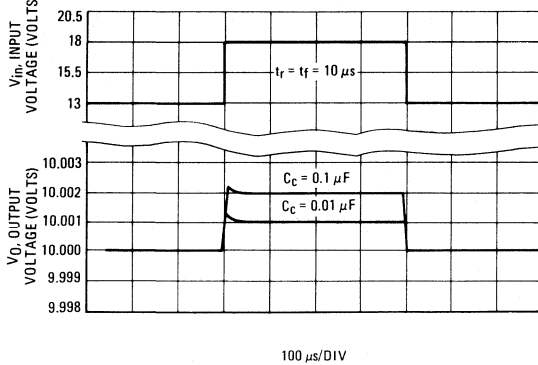


FIGURE 22 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

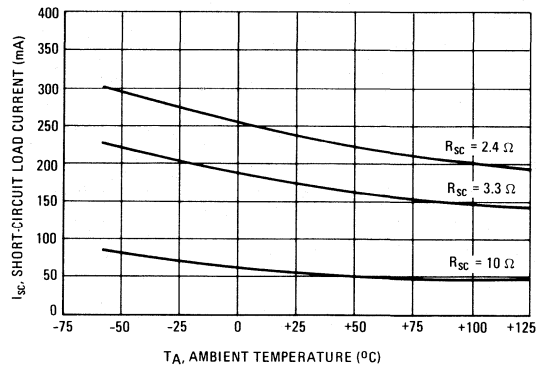


FIGURE 23 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, $C_O = 10 \mu F$

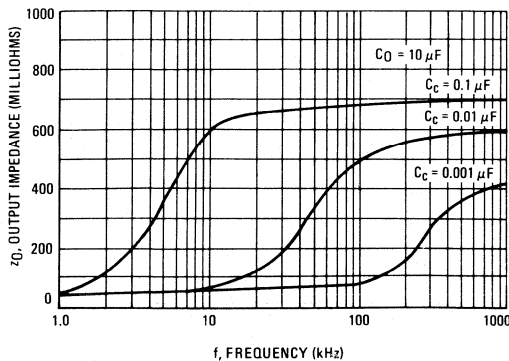
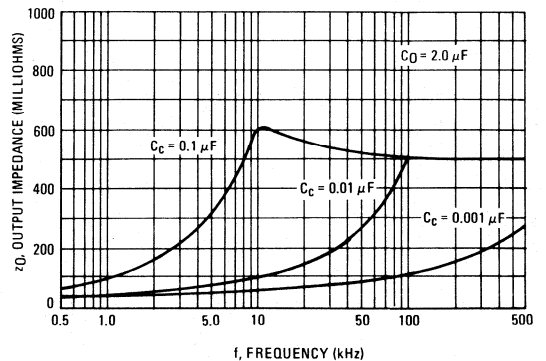


FIGURE 24 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, $C_O = 2.0 \mu F$



7

OPERATIONS AND APPLICATIONS

This section describes the operation and design of the MC1569 positive voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE

| | | |
|--|--|--|
| Theory of Operation NPN Current Boosting PNP Current Boosting Switching Regulator Positive and Negative Power Supplies | Shutdown Techniques Voltage Boosting Remote Sensing An Adjustable-Zero-Temperature-Coefficient Voltage Source | Thermal Shutdown Thermal Considerations Latch-Up |
|--|--|--|

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 25, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 26. The gain-determining resistors may be external, enabling a wide range of output voltages. This

is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1569) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1569 positive-voltage regulator.

FIGURE 25 - SERIES VOLTAGE REGULATOR

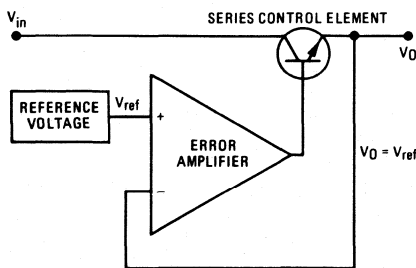


FIGURE 26 - THE "REGULATOR-WITHIN-A-REGULATOR" APPROACH

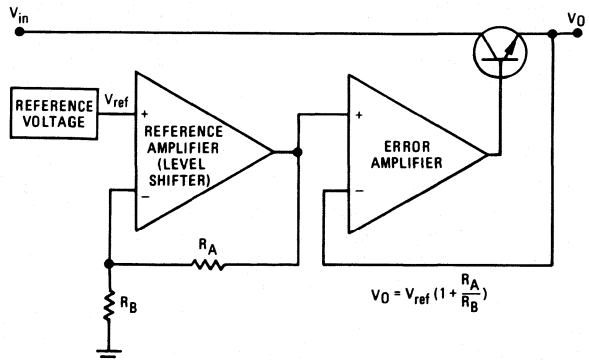
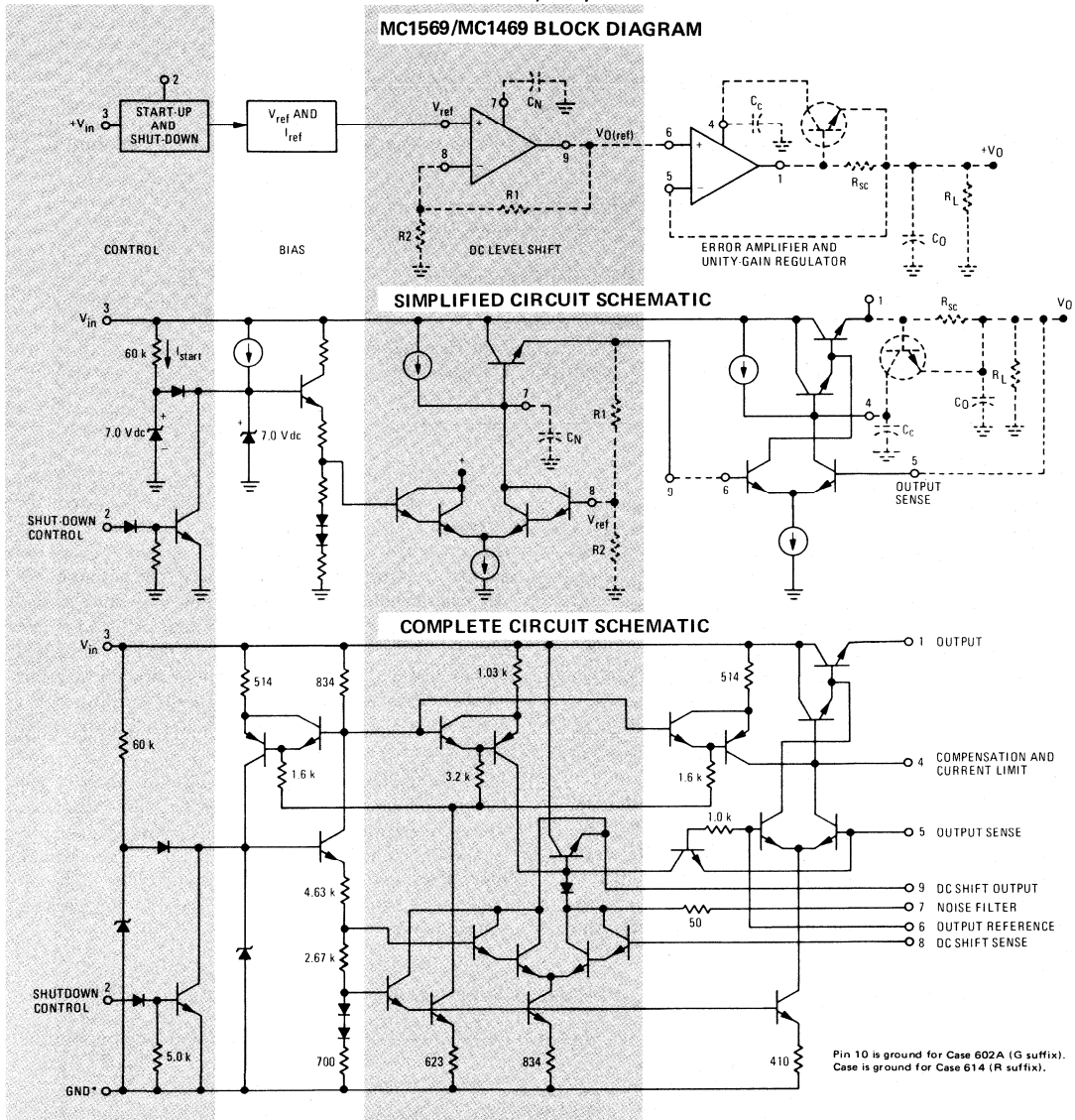


FIGURE 27
(Recommended External Circuitry is Depicted With Dotted Lines.)



MC1569 Operation

Figure 27 shows the MC1569 Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated

input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

7

The shutdown control consists of an NPN transistor across the reference zener diode. When this transistor is turned "ON", via pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shut-down. During shutdown the current drain of the complete IC regulator drops to $V_{in}/60\text{ k}\Omega$ or $500\text{ }\mu\text{A}$ for a 30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately 3.5 Vdc with a typical temperature coefficient of $0.002\text{ }\%/^{\circ}\text{C}$. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R1 and R2) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_N , is introduced externally into the level shift network (via pin 7) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is $0.1\text{ }\mu\text{F}$ and should have a voltage rating in excess of the desired output voltage. Smaller capacitors ($0.001\text{ }\mu\text{F}$ minimum) may be used but will cause a slight increase in output noise. Larger values of C_N will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

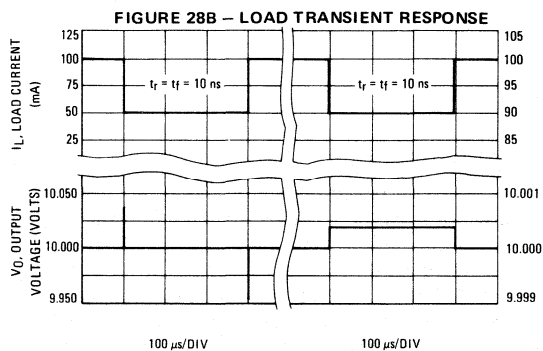
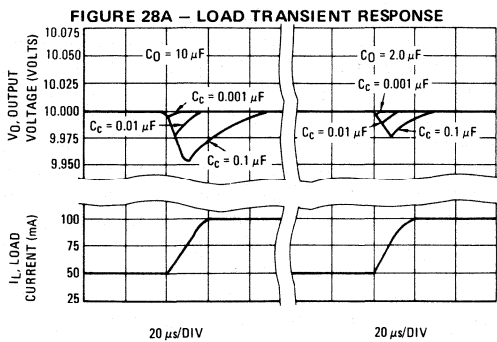
The output of the level shift amplifier (pin 9) is fed to the noninverting input (pin 6) of the output error amplifier. The inverting input to this amplifier is the Output Sense connection (pin 5) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{SC} , is connected in the emitter of this transistor to sample the full load current. By placing an external low-level NPN transistor across R_{SC} as shown in Figure 27, output current can be limited to a predetermined value:

$$I_L \text{ max} \approx \frac{0.6}{R_{SC}} \text{ or } R_{SC} = \frac{0.6}{I_L \text{ max}}$$

where $I_L \text{ max}$ is the maximum load current (amperes) and R_{SC} is the value of the current limiting resistor (ohms).

Stability and Compensation

As has been seen, the MC1569 employs two amplifiers, each using negative feedback. This implies the possibility of instability due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (pin 4) and ground. The recommended value of $0.001\text{ }\mu\text{F}$ will insure stability and still provide acceptable transient response (see Figure 28, A and B). It is also necessary to use an output capacitor, C_O (typically $1.0\text{ }\mu\text{F}$) from the output, V_O , to ground. When an external transistor is used to boost the current, $C_O = 1.0\text{ }\mu\text{F}$ is also recommended (see Figure 2).



TYPICAL NPN CURRENT BOOST CONNECTIONS

FIGURE 29A - 5 VOLT 5-AMPERE REGULATOR

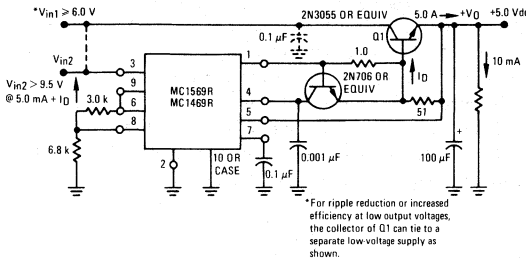


FIGURE 29B - 5-VOLT 5-AMPERE REGULATOR

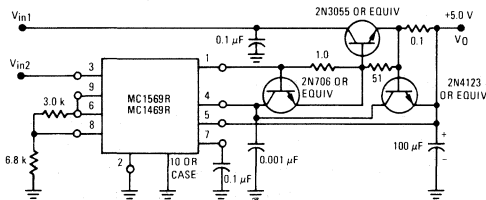
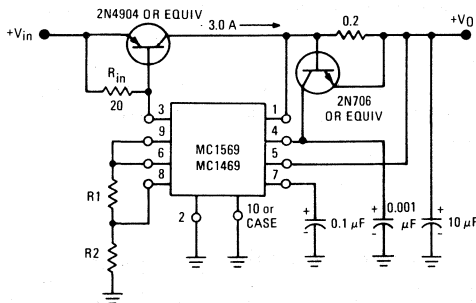


FIGURE 30 - PNP CURRENT BOOST CONNECTION



NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 2 or 29 are recommended. The transistor shown in Figure 29A, the 2N3055 can supply currents to 5.0 amperes (subject, of course, to the safe area limitations). To improve the efficiency of the NPN

boost configuration, particularly for small output voltages, the circuit of Figure 29 is recommended. An auxiliary 9.5-volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 5.0 ampere regulator of Figure 29 this represents a savings of 17.5 watts when compared with operating the regulator from the single 9.5 V supply. It can supply current to 5.0 amperes while requiring an input voltage to the collector of the pass transistor of 6.0 volts minimum. The pass transistor is limited to 5.0 amperes by the added short-circuit current network in its emitter (R_{SC}), (Figure 29B).

PNP CURRENT BOOSTING

A typical PNP current boost circuit is shown in Figure 30. Voltages from 2.5 Vdc to 37 Vdc and currents of many amperes can be obtained with this circuit.

Since the PNP transistor must not be turned on by the MC1569 bias current (I_{IB}) the resistor R_{in} must meet the following condition

$$R_{in} < \frac{V_{BE}}{I_{IB}}$$

where V_{BE} is the base-to-emitter voltage required to turn on the PNP pass transistor, (typically 0.6 Vdc for silicon and 0.2 Vdc for germanium).

For germanium pass transistors, a silicon diode may be placed in series with the emitter to provide an additional voltage drop. This allows a larger value of R_{in} than would be possible if the diode were omitted. The diode will, however, be required to carry the maximum load current.

SELF-OSCILLATING SWITCHING REGULATOR

In all of the current boosting circuits shown thus far it has been assumed that the input-output voltage differential can be minimized to obtain maximum efficiency in both the external pass element as well as the MC1569. This may not be possible in applications where only a single supply voltage is available and high current levels preclude zener diode pre-regulating approaches. In such applications a switching-mode voltage regulator is highly desirable since the pass device is either ON or OFF. The theoretical efficiency of an ideal switching regulator is 100%. Realizable efficiencies of 90% are within the realm of possibility thus obviating the need for large power dissipating components. The output voltage will contain a ripple component; however, this can be made quite small if the switching frequency is made relatively high so filtering techniques are effective. Figure 31 shows a functional diagram for a self-oscillating voltage regulator. The comparator-driver will sense the voltage across the inductor, this voltage being related to the load current, I_L , by

MC1569, MC1469 (continued)

$$L \frac{dI_L}{dt} = V.$$

For a first approximation this can be assumed to be a linear relationship.

Initially, V_O will be low and Q1 will be ON. The voltage at the non-inverting input will approach $\beta_1 V_{in}$, when:

$$\beta_1 V_{in} = \frac{V_{ref} R_a}{R_a + R_b} + \frac{V_c R_b}{R_a + R_b}.$$

When this output voltage is reached the comparator will switch, turning Q1 OFF. The diode, CR1, will now become forward biased and will supply a path for the inductor current. This current and the sense voltage will start to decrease until the output voltage reaches

$$\beta_2 V_{in} = \frac{V_{ref} R_a}{R_a + R_b}$$

where the comparator will again switch turning Q1 ON, and the cycle repeats. Thus the output voltage is approximately V_{ref} plus a ripple component.

The frequency of oscillation can be shown to be

$$f = \frac{V_O (V_{in} - V_O)}{L V_C I(\max) - I_O} \quad (1)$$

where

$I(\max)$ = The maximum value of inductor current

I_O = The minimum inductor current.

Normally this frequency will be in the range of approximately 2 kHz to 6 kHz. In this range, inductor values can be small and are compatible with the switching times of the pass transistor and diode. The switching time of the comparator is quite fast since positive feedback aids both turn-on and turn-off times. The limiting factors are the diode and pass transistor rise and fall times which should be quite fast or efficiency will suffer.

Figure 32 shows a self oscillating switching regulator which in many respects is similar to the PNP current boost previously discussed. The 6.8 kΩ resistor in conjunction with R1 sets the reference voltage, V_{ref} . Q1 and CR1 are selected for fast switching times as well as the necessary power dissipation ratings. Since a linear inductor is assumed, the inductor cannot be allowed to saturate at maximum load currents and should be chosen accordingly. If core saturation does occur, peak transistor and diode currents will be large and power dissipation will increase.

FIGURE 31 — BASIC SELF-OSCILLATING SWITCHING REGULATOR

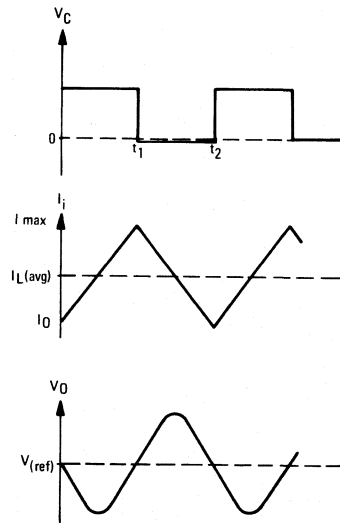
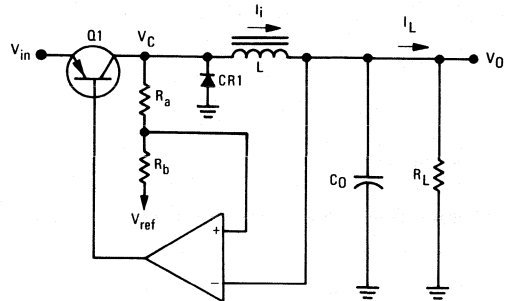
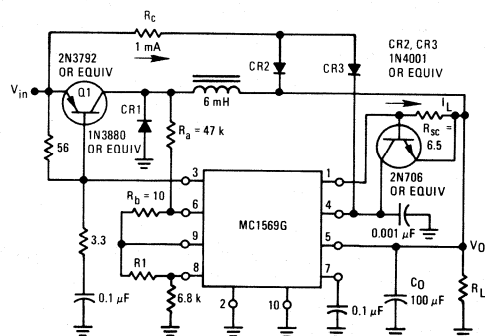


FIGURE 32 — MC1569 SELF-OSCILLATING SWITCHING REGULATOR



As a design center is required for a practical circuit, assume the following requirements:

$$V_{in} = +28 \text{ Volts}$$

$$V_O = +10 \text{ Volts}$$

$$\Delta V_O = 50 \text{ mV}$$

$$f \approx 5 \text{ kHz}$$

$$I(\text{max}) = 1.125 \text{ A}$$

$$I_O = 1 \text{ A}$$

$$\Delta V \approx V_{in} \frac{R_b}{R_a} \quad (2)$$

Using Equation (1), the inductor value can be found:

$$L = \frac{(28-10)}{2(1.125-1)} \frac{10}{28} \left(\frac{1}{5 \times 10^3} \right) \\ \approx 7 \text{ mH.}$$

For the test circuit, a value of 6 mH was selected. Using for a first approximation

$$C_O = \frac{(V_{in} - V_O)(V_O)}{8L f^2 V_{in} (\Delta V)} \\ = \frac{(28 - 10)10}{8(7 \times 10^{-3})(5 \times 10^3)^2 (28)(50 \times 10^{-3})} \\ \approx 95 \mu\text{F.}$$

As shown, a value of 100 μF was selected. Since little current is required at pin 6, R_a can be large. Assume $R_a = 47 \text{ k}\Omega$ and then use Equation (2) to determine R_b :

$$50 \times 10^{-3} = \frac{28}{47 \text{ k}\Omega} R_b \\ R_b = \frac{47}{28} 50 \approx 85\Omega.$$

Since the internal impedance presented by pin 9 is on the order of 60Ω , a value of $R_b = 10\Omega$ is adequate.

Diodes CR2, CR3, and R_c may be added to prevent saturation of the error amplifier to increase switching

speed. When the output stage of the error amplifier approaches saturation, CR2 becomes forward biased and clamps the error amplifier. Resistor R_c should be selected to supply a total of 1 mA dc to CR2 and CR3.

To show correlation between the predicted and tested specifications the following data was obtained:

$$V_{in} = +28 (\pm 1\%) \text{ Volts}$$

$$V_O = +10 \text{ Volts}$$

$$\Delta V_O = 60 \text{ mV}$$

$$f = 7 \text{ kHz}$$

$$@ I_L = 1 \text{ A}$$

which checks quite well with the predicted values. R_b can be adjusted to minimize the ripple component as well as to trim the operating frequency. Also this frequency will change with varying loads as is normal with this type of circuit. Pin 2 can still be used for shut-down if so desired. R_{sc} should be set such that the ratio of load current to base drive current is 10:1 in this case $I_1 \approx 100 \text{ mA}$ and $R_{sc} = 6.5\Omega$.

POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1569 is driven from a floating source it is possible to use it as a negative regulator by grounding the positive output terminal. The MC1569 may also be used with the MC1563 to provide completely independent positive and negative voltage regulators with comparable performance.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 3 and 33 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (pin 6 of the MC1569) and using the other side (pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3-k ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at pin 5 will be zero. When the voltage at pin 5 equals zero, $+V_O$ must equal $-V_O$.

For the configuration shown in Figure 33, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5-volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5-volt supply, as shown,

as the resistance of the interconnecting lines (V_O and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 37 shows how remote sensing is accomplished using both a separate sense line from pin 8 and a separate ground line from the regulator to the remote load.

AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE.

The MC1569, when used in conjunction with low TC resistors, makes an excellent reference-voltage generator. If the 3.5 volt reference voltage of the IC regulator is a satisfactory value, then pins 8 and 9 can be tied together and no resistors are needed. This will provide a voltage

reference having a typical temperature coefficient of 0.002%/°C. By adding two resistors, R1 and R2, any voltage between 3.5 Vdc and 37 Vdc can be obtained with the same low TC (see Figure 38).

THERMAL SHUTDOWN

By setting a fixed voltage at pin 2, the MC1569 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor and the diode in series with pin 2 ($-3.4 \times 10^{-3}V/°C$). By setting 1.0 Vdc externally at pin 2, the regulator will shutdown when the chip temperature reaches approximately +140°C. Figure 39 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

FIGURE 37 – REMOTE SENSING CIRCUIT

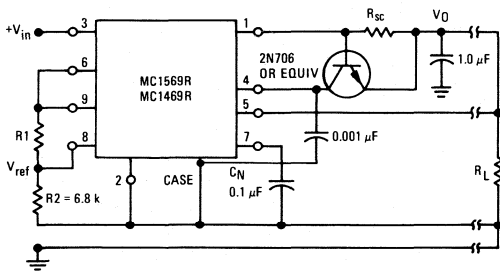


FIGURE 38 – AN ADJUSTABLE "ZERO-TC" VOLTAGE SOURCE

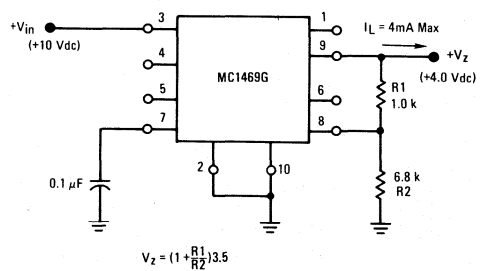


FIGURE 39 – JUNCTION TEMPERATURE LIMITING SHUTDOWN CIRCUIT

FIGURE 39A – USING A ZERO TC REFERENCE

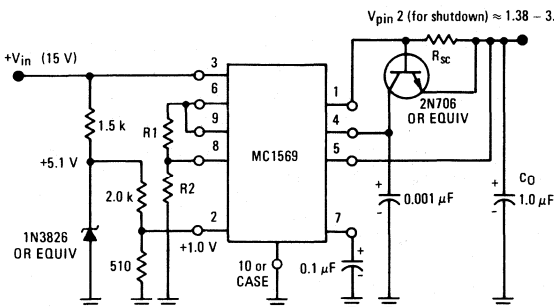


FIGURE 39B – USING A TA REFERENCE

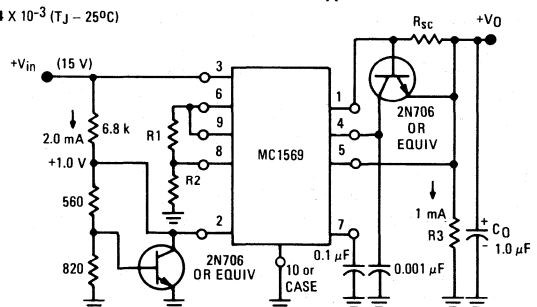
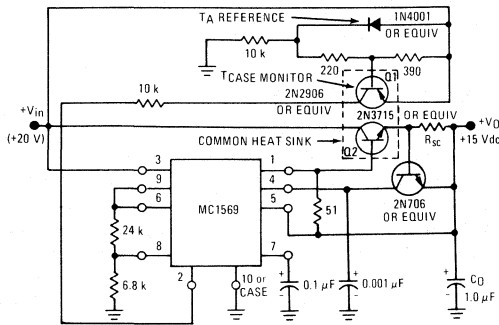


FIGURE 40 – THERMAL SHUTDOWN WHEN USING EXTERNAL PASS TRANSISTORS



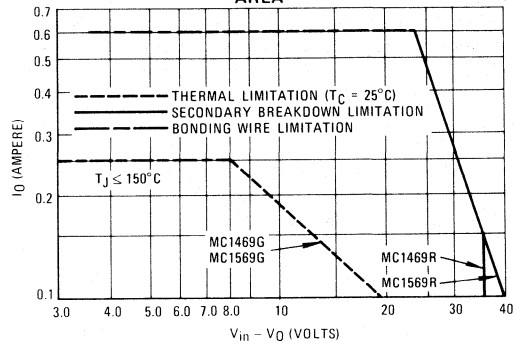
In the case where an external pass transistor is employed, its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 40. The case of the normally "OFF" thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application, the designer must use caution not to exceed the specified maximum junction temperature (+150°C). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor*. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current. Care should be taken not to

*For more detailed information of methods used to compute junction temperature, see Motorola Application Note AN-226, Measurement of Thermal Properties of Semiconductors.

FIGURE 41 – DC SAFE OPERATING AREA



exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 41).

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, TA, or a change in the power dissipated in the IC regulator. The effects of ambient temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as ±0.002%/°C, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O, can be used to describe this effect and is typically -0.06%/watt for the MC1569. For an example of the relative magnitudes of these effects, consider the following conditions:

Given MC1569

with V_{in} = 10 Vdc

V_O = 5 Vdc

and $I_L = 100 \text{ mA to } 200 \text{ mA}$

$$(\Delta I_L = 100 \text{ mA})$$

assume $T_A = +25^\circ\text{C}$

TO-66 Case with heatsink

assume $\theta_{CS} = 0.2^\circ\text{C/W}$

and $\theta_{SA} = 2^\circ\text{C/W}$

$\theta_{JC} = 7.15^\circ\text{C/W}$ (from maximum ratings table)

It is desired to find the ΔV_O which results from this ΔI_L . Each of the three previously stated effects on V_O can now be separately considered.

1. ΔV_O due to ΔT_J

$$\Delta V_O = (V_O)(\Delta P_D)(TCV_O)(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

OR

$$\Delta V_O = (5V)(5 \text{ V} \times 0.1 \text{ A})(\pm 0.002\%/^\circ\text{C})(9.35^\circ\text{C/W})$$

$$\Delta V_O \approx \pm 0.5 \text{ mV}$$

2. ΔV_O due to z_o

$$|\Delta V_O| = (-z_o)(I_L)$$

$$|\Delta V_O| = -(2 \times 10^{-2})(10^{-1}) = -2 \text{ mV}$$

3. ΔV_O due to gradient coefficient, GCV_O

$$|\Delta V_O| = (GCV_O)(V_O)(\Delta P_D)$$

$$|\Delta V_O| = (-6 \times 10^{-4}/\text{W})(5 \text{ volts})(5 \times 10^{-1} \text{ W})$$

$$|\Delta V_O| = -1.6 \text{ mV}$$

Therefore the total ΔV_O is given by

$$|\Delta V_O \text{ total}| = \pm 0.5 - 2.0 - 1.6 \text{ mV}$$

OR

$$-4.1 \text{ mV} \leq |V_O \text{ total}| \leq -3.1 \text{ mV}$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

TYPICAL PRINTED CIRCUIT BOARD LAYOUT

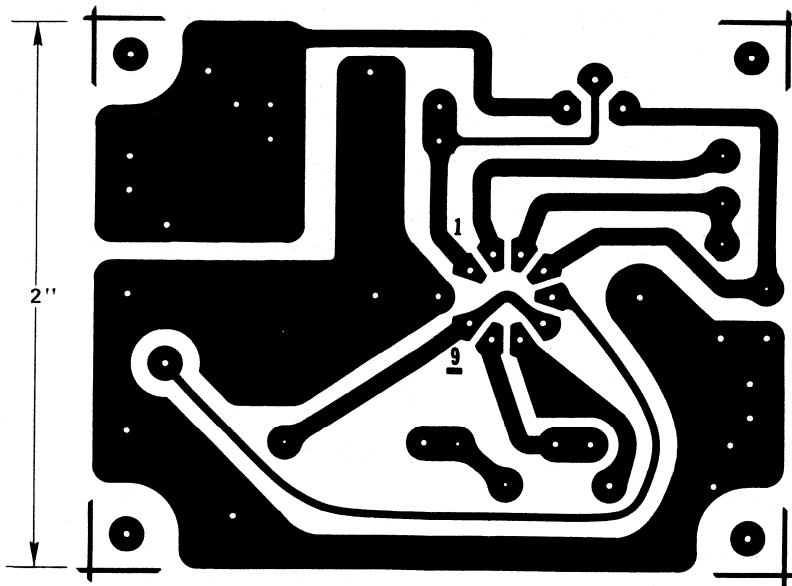


FIGURE 42 – LOCATION OF COMPONENTS

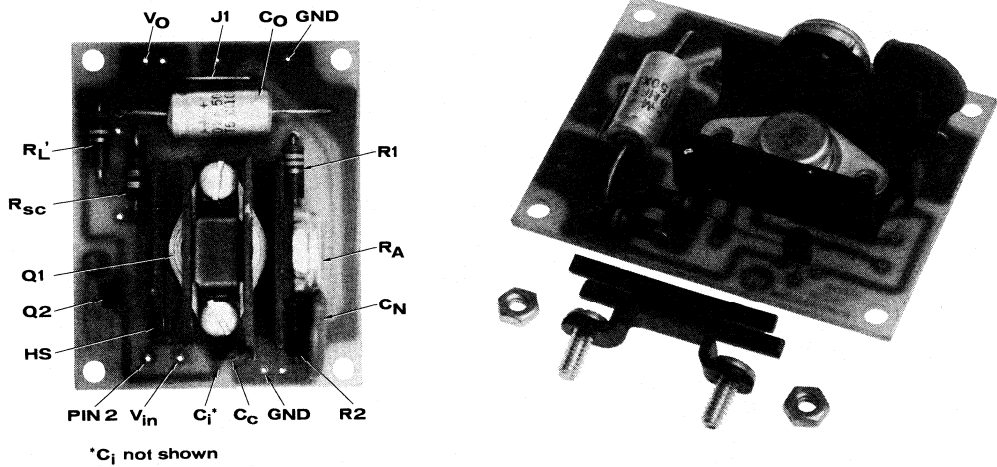
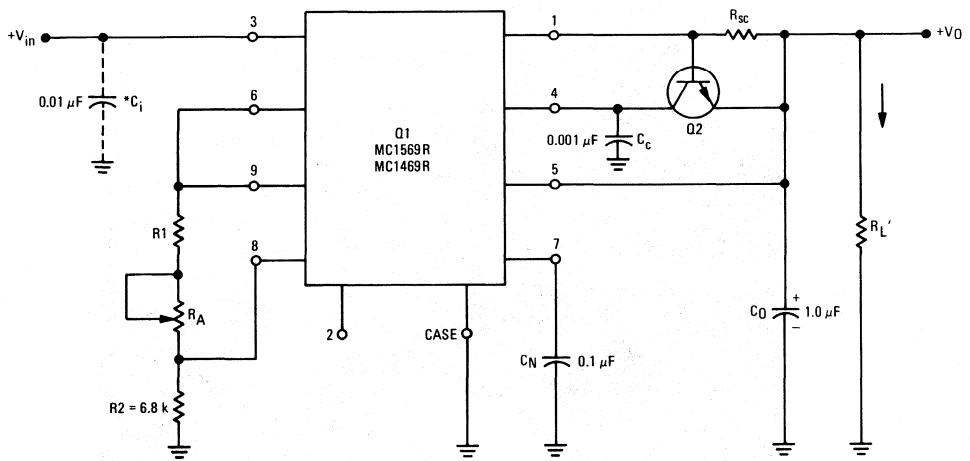


FIGURE 43 – CIRCUIT SCHEMATIC FOR PRINTED CIRCUIT BOARD (Pg. 17)
 $3.5 \text{ V} \leq V_O \leq 37 \text{ V}$, $1 \text{ mA} \leq I_L \leq 500 \text{ mA}$



Select R1 to give desired V_O: $R1 = (2 V_O - 7) \text{ k}\Omega$

*C_i – May be required if long input leads are used.

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MC1580L

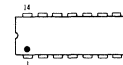
MONOLITHIC DUAL LINE DRIVER/RECEIVER

The output current of the MC1580L switches in response to a differential input voltage. A wide common-mode input and output voltage range makes this device ideal for transmission of digital information in a noisy environment. Typical applications include driving a twisted-pair transmission line, line sharing, voltage comparator, and logic level translation.

- High Input and Output Impedance – 5.0 k ohms at 10 MHz typ
- Low Propagation Delay – 18 ns max
- Wide Common-Mode Input and Output Voltage Range – ± 3.5 V Input min and $-3.0/+9.0$ V Output min
- Input Gating Ability
- Bias Driver for MECL Applications, plus Interfacing Capability with MRTL, MDTL, and M TTL
- Compatible with Other Devices of the Line Driver/Receiver Series

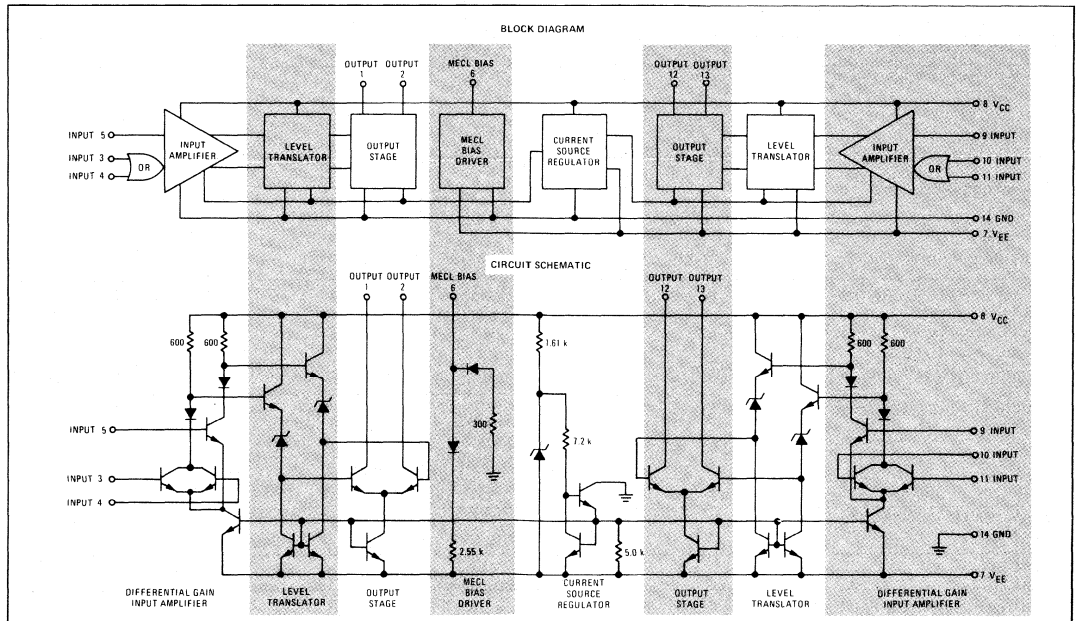
DUAL LINE DRIVER/RECEIVER INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED



(top view)

Ceramic Package
Case 632
(TO-116)



See Packaging Information Section for outline dimensions.

MC1580L (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|--------------------------|--------------|----------------------------|
| Power Supply Voltage | V_{CC} V_{EE} | +7.0 -7.0 | Vdc |
| Differential-Mode Input Signal Voltage | V_{in} | ± 7.0 | Volts |
| Common-Mode Input Signal Voltage | CMV_{in} | ± 10 | Volts |
| Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above $T_A = +25^\circ\text{C}$ | P_D $1/\theta_{JA}$ | 575 3.85 | mW mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +175 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS (Each Line Driver/Receiver, $V_{CC} = +5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|--------|--|-------------------|------------------------|---------------------|------------------------------|
| Operating Supply Currents | 1 | I_{CC} I_{EE} | - | 5.0 25 | 8.0 30 | mA |
| Input Leakage Current | 1 | I_R | - | 0.01 | 0.1 | μA |
| Input Current $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 1 | I_{in} | - | 0.04 0.02 0.01 | 0.2 0.1 0.1 | mA |
| Output Leakage Current | 1 | I_{CEX} | - | 0.8 | 5.0 | μA |
| Output Load Current $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 1 | I_{OL} | 6.5 6.9 6.8 | 8.1 8.6 8.5 | 9.8 10.4 10.2 | mA |
| Output Load Current Match $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 6 | ΔI_{OL} | - | 0.25 0.2 0.15 | 0.5 0.5 0.5 | mA |
| Power Supply Operating Range | | V_{CC} V_{EE} | +4.75 -4.75 | +5.0 -5.0 | +6.00 -6.00 | Vdc |
| MECL Bias Voltage ($V_{EE} = -5.2\text{ Vdc}$) | | V_{BB} | -1.11 | -1.175 | -1.24 | Vdc |
| Input Voltage Transition Width* $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | | V_{TR} | - | 30 35 40 | 50 50 50 | mV |
| Switching Times Propagation Delay Time | 2 | t_{pd+} t_{pd-} | - | 13 13 | 18 18 | ns |
| Rise Time | | t_r | - | 11 | - | |
| Fall Time | | t_f | - | 7.0 | - | |
| Parallel Impedance ($f = 5.0\text{ MHz}$) Input Capacitance Input Resistance Output Capacitance Output Resistance | | C_p (in) R_p (in) C_p (out) R_p (out) | - | 9.0 8.0 10 10 | - - - - | pF k ohms pF k ohms |
| Common-Mode Voltage Range (-55 to +125 $^\circ\text{C}$) Input | 3 | $CMVR_{in}$ | +3.5 -3.5 | +4.4 -4.2 | - - | Volts |
| Output | 4 | $CMVR_{out}$ | +9.0 -3.0 | +10 -3.3 | - - | |
| Common-Mode Voltage Gain $f = 60\text{ MHz}$ | 5 | $ACMV$ | - | -40 | - | dB |
| Power Dissipation | | P_D | - | 150 | 180 | mW |

*Measurement taken from points of Unity Gain.

Ground unused output pins and their corresponding inputs to assure correct device biasing.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – TERMINAL CURRENTS

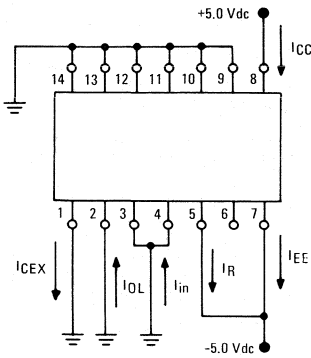


FIGURE 2 – TRANSIENT RESPONSE

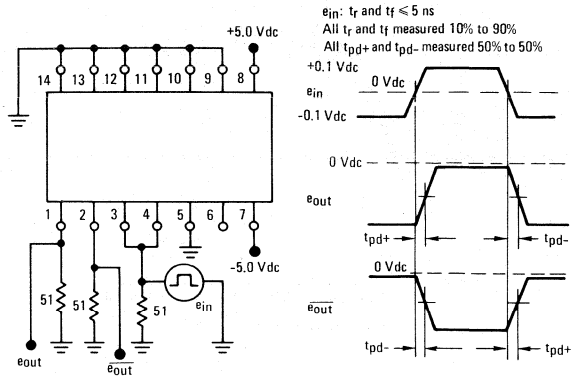


FIGURE 3 – COMMON-MODE INPUT VOLTAGE RANGE

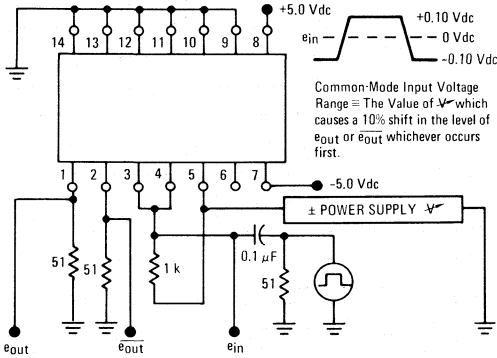


FIGURE 4 – COMMON-MODE OUTPUT VOLTAGE RANGE

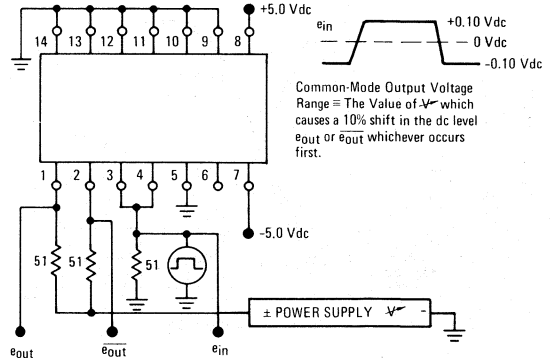


FIGURE 5 – COMMON-MODE VOLTAGE GAIN

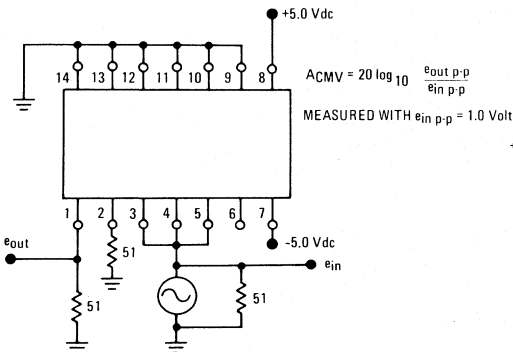
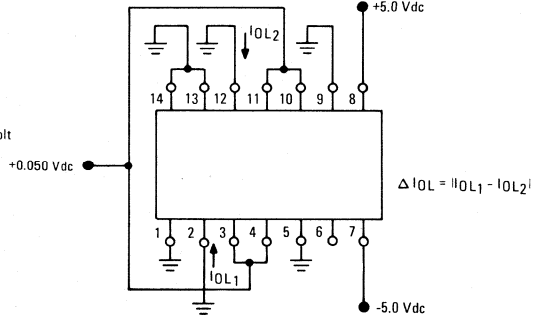


FIGURE 6 – OUTPUT CURRENT MATCH



TYPICAL CHARACTERISTICS

FIGURE 7 – OUTPUT LOAD CURRENT versus SUPPLY OPERATING VOLTAGE AND TEMPERATURE

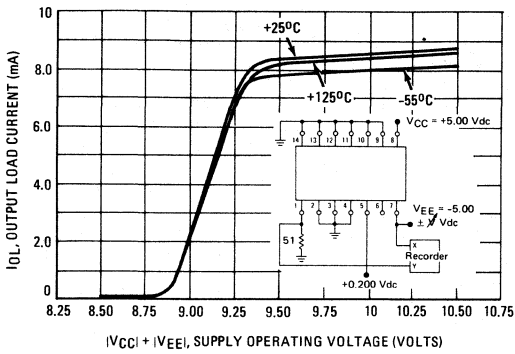


FIGURE 8 – EXPANDED OUTPUT LOAD CURRENT versus SUPPLY OPERATING VOLTAGE AT +25°C

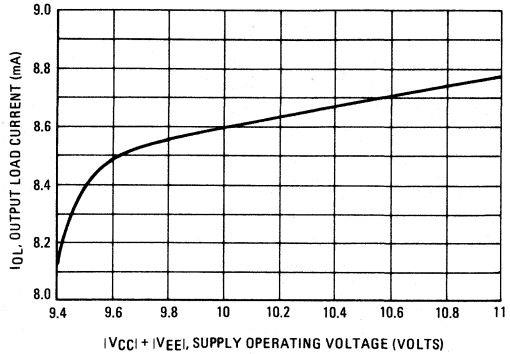


FIGURE 9 – OUTPUT LOAD CURRENT versus DIFFERENTIAL INPUT VOLTAGE AND TEMPERATURE

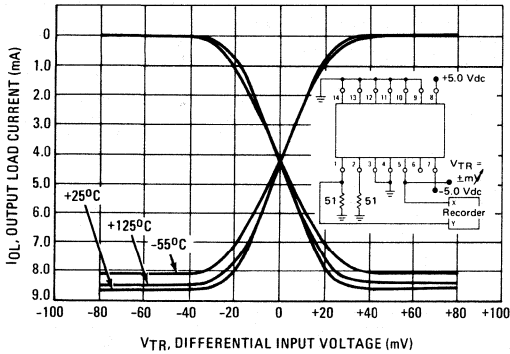


FIGURE 10 – PROPAGATION DELAY versus DIFFERENTIAL INPUT VOLTAGE

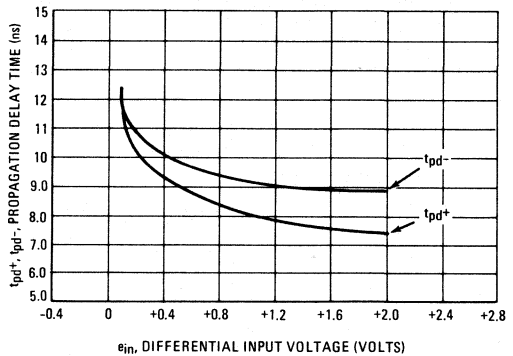
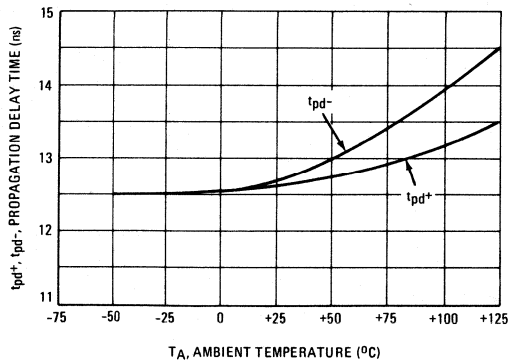


FIGURE 11 – PROPAGATION DELAY versus AMBIENT TEMPERATURE



7

TYPICAL CHARACTERISTICS (continued)

FIGURE 12 – INPUT IMPEDANCE versus FREQUENCY

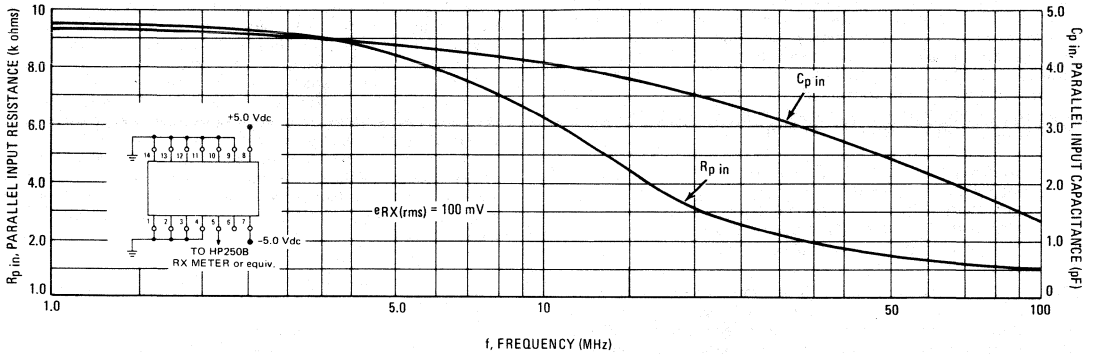


FIGURE 13 – OUTPUT IMPEDANCE versus FREQUENCY

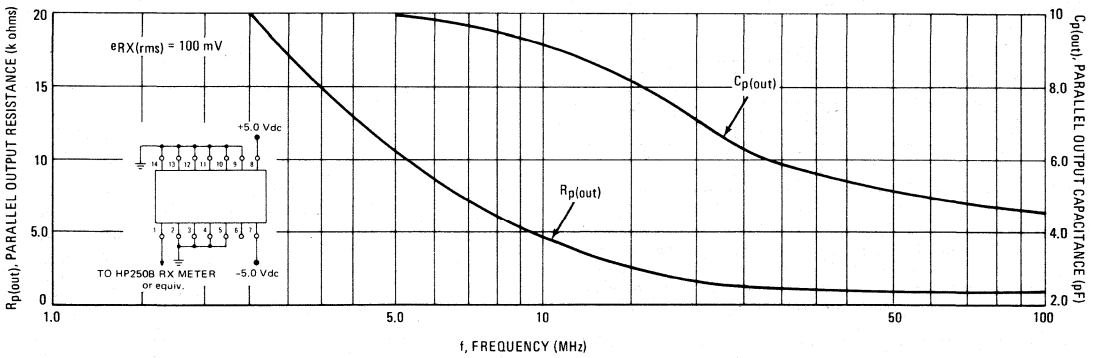
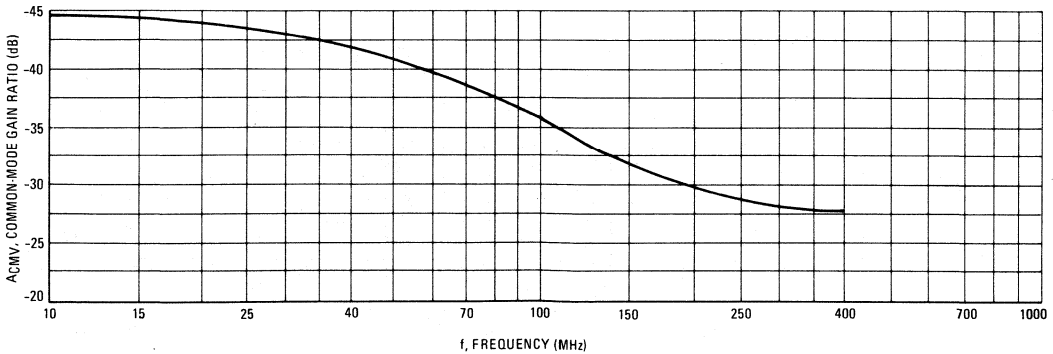


FIGURE 14 – COMMON-MODE GAIN RATIO versus FREQUENCY



APPLICATIONS INFORMATION

Line Driver/Receiver Family Characteristics

The Motorola line driver/receiver series provides interface circuits for driving digital data transmission lines e.g., coaxial cable or twisted pair. The digital data transmission is via a balanced differential mode. The line drivers and receivers are designed to provide high common-mode noise rejection, present high impedances to the transmission line and have low propagation times. A feature of the drivers is the capability to operate in a party-line mode whereby a number of drivers can be connected to a single line. This series provides drivers and receivers compatible with MRTL, MDTL, M TTL and MECL. The five circuits of the family are:

- MC1580L Dual Line Driver/Receiver
- MC1581L Dual MECL Receiver
- MC1582L Dual MDTL/M TTL Driver
- MC1583L Dual Receiver (Open Collector)
- MC1584L Dual Receiver (Active Pullup)

Figure 15 indicates line drivers and receivers recommended for interfacing with each of the various digital logic families. The MC1580L serves as a basic building block and can be used as a driver or receiver with any of the indicated digital logic families by adding the appropriate external components.

FIGURE 15

| Digital Logic Family | Driver | Receiver |
|----------------------|--------------------|--------------------|
| MECL | MC1580L | MC1581L |
| MDTL | MC1582L | MC1583L MC1584L |
| M TTL | MC1582L | MC1583L MC1584L |
| MRTL | MC1580L MC1582L | MC1583L |

These five circuits are extremely useful in numerous applications other than line drivers and receivers. The differential amplifier input of the receiver makes it useful in applications such as voltage comparators, waveform generators and high-input-impedance buffers. The drivers and receivers are useful as logic level translators.

The MC1580L in Figure 16 serves as the line driver and line receiver for a balanced differential transmission line. The driver input and receiver outputs of Figure 16 are compatible with MRTL.

The output stage of the driver switches a current source between the two driver outputs in response to the input logic signals. Hence, a voltage differential that is a function of the line termination impedances is created on the twisted pair and at the input of the receiver. The receiver is designed to reject +3.5/-3.5 Volts of common-mode voltage signals which may be present due to ground loop currents and noise coupled from nearby transmission lines.

While common-mode noise is the major concern in a twisted pair transmission line; a good data transmission system must offer some immunity from differential-mode voltages that may be present due to mismatches in termination impedances. The drivers and receivers of the MC1580 Series are designed with this requirement in mind. The exact amount of noise immunity depends on line impedances but the following example shows how differential-mode noise immunity is calculated for a given system. For a line with a characteristic impedance of Z_0 , calculate the minimum differential input voltage from the equation.

$$\pm V_{in} = \frac{I_o(\min) \times Z_0}{4}$$

For a 170-ohm line, $V_{in} = \frac{(6.9)(170)}{4} = 0.29$ Volts.

Since the MC1580L requires 50 mV maximum input differential to maintain the output state, the worst case differential-mode noise immunity is 0.26 V. (See Figure 17).

FIGURE 17

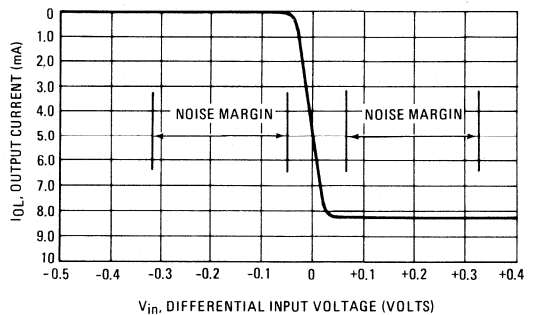
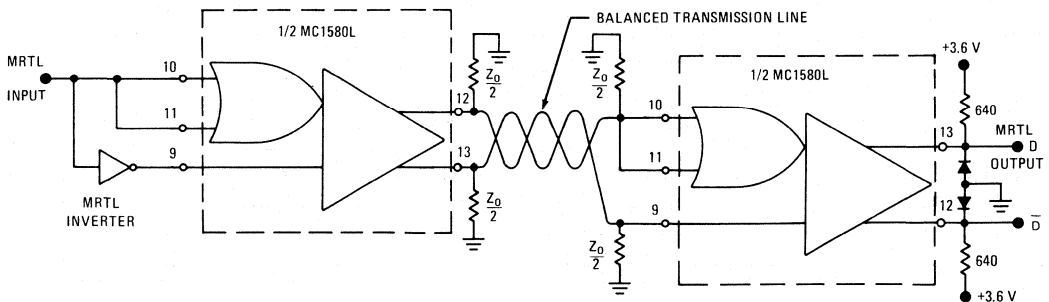


FIGURE 16



APPLICATIONS INFORMATION (continued)

Hence the direct coupling of the driver and receiver to the line provides a built-in differential-mode noise immunity. The direct coupling also matches the line at all frequencies (often a problem with ac coupling lines). The recovery problem in ac coupling devices at high-signal repetition rates is also eliminated.

High input and output impedances of the MC1580L minimize impedance discontinuities on the transmission line and allow many drivers and receivers to be connected to the line.

Use of the MC1580L in a bi-directional MECL compatible transmission system is shown in Figure 18. The MC1580L has an internal MECL line driver. The drivers of Figure 18 are connected so that the current sources from both drivers pull current from the same wire of the twisted pair when both drivers are transmitting logic "0" signals. The external current source, I_S , supplies the current required by one driver. The current for the other driver is drawn from the termination impedances, creating a voltage differential across the line. When either driver transmits a logic "1", a voltage difference of the opposite polarity is created across the line. For a system with two drivers the current source (I_S) can be supplied by a 600-ohm resistor connected to +5.0 Volts.

If additional drivers are connected to the line, a matching current source is connected for each added driver. The current sources are connected to the line so that when all drivers are transmitting logic "0"s, the difference in current drawn from the terminating resistors of the two wires in the twisted pair is equal to one current source (8.6 mA). The current sources should also be connected so that when any driver transmits a logic "1" then a current difference of the opposite polarity exists. The matching current source should be the companion circuit on the MC1580L driver chip. The difference in amplitude of the current sources on a single chip is specified to allow the system designer to calculate the maximum current source mismatch, ΔI_{OL} , and hence the maximum number of drivers that can be connected to a given transmission line.

The MC1580L has many other uses in a digital system. The high input impedance suggests its use as a buffer for delay lines and in waveform generation circuits. Figure 19 shows the MC1580L used as a differential comparator in a double-ended limit detector. When the input signal amplitude is between the two reference voltages, the output signal will be a logic "1"; otherwise a logic "0" output is obtained. The voltage transition region is typically less than 40 mV. External components R1 and CR1 establish an MDTL compatible signal.

FIGURE 18 – BI-DIRECTIONAL TRANSMISSION

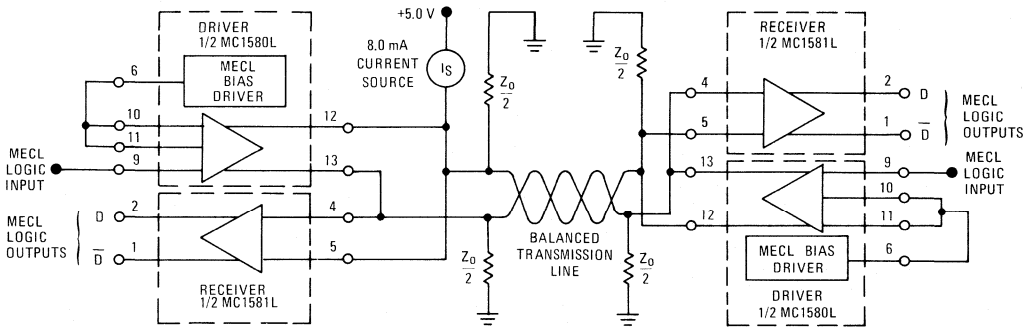
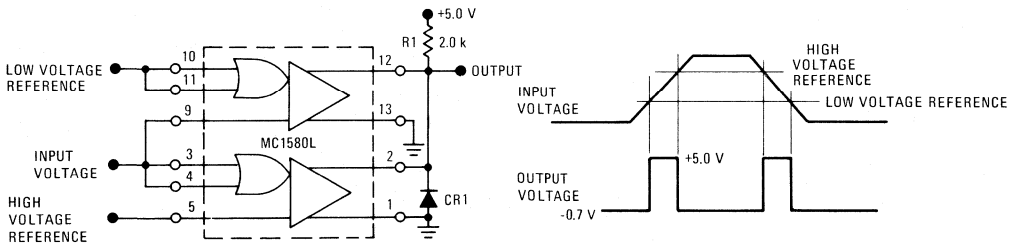


FIGURE 19 – DOUBLE-ENDED LIMIT DETECTOR



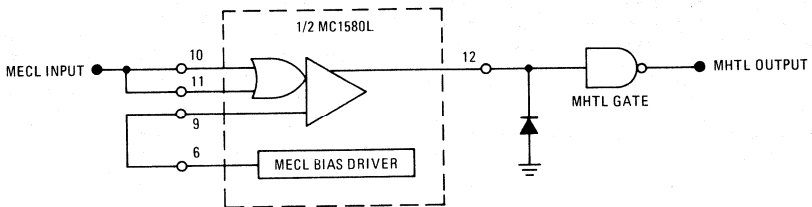
MC1580L (continued)

APPLICATIONS INFORMATION (continued)

Voltage Translator

Translation of voltage levels from MECL (best suited for the high-speed portion of a digital system) to MHTL (tailored for the noisy output portion of the system) is often required. The MC1580 performs this function as indicated in Figure 20.

FIGURE 20 – MECL TO MHTL VOLTAGE LEVEL TRANSLATOR



LINEAR/DIGITAL INTERFACE CIRCUITS

MC1581L

MONOLITHIC DUAL MECL LINE RECEIVER

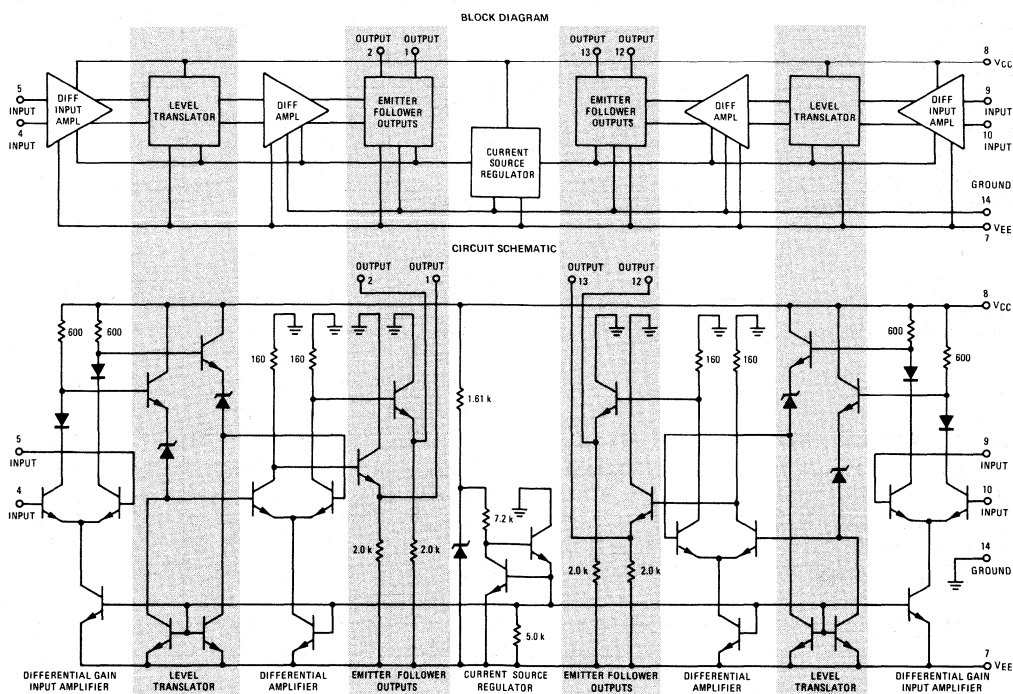
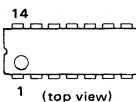
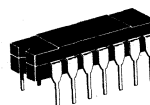
... designed with output emitter follower voltage levels that switch in response to a differential input voltage. The device output voltage levels are compatible with that of the MECL digital logic family. With its excellent common-mode input voltage range, the MC1581L is ideally suited for receiving digital data in noisy environments. Typical applications include line sharing, voltage comparator, and level translation.

- High Input Impedance – 8.0 k ohms @ 10 MHz
- Low Propagation Delay Time – 20 ns max
- Wide Common-Mode Input Voltage Range – ± 3.5 Vdc
- Device Compatibility with Other Members of the Line Driver/Receiver Series

DUAL MECL LINE RECEIVER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

CASE 632
CERAMIC PACKAGE
TO-116



See Packaging Information Section for outline dimensions.

MC1581L (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|-----------------|-------------|----------------------|
| Power Supply Voltage | V_{CC} | +7.0 | Vdc |
| | V_{EE} | -7.0 | |
| Differential-Mode Input Signal Voltage | V_{in} | ± 7.0 | Volts |
| Common-Mode Input Signal Voltage | CMV_{in} | ± 10 | Volts |
| Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above $T_A = +25^\circ\text{C}$ | P_D | 575 | mW |
| | $1/\theta_{JA}$ | 3.85 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +175 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS (Each Receiver, $V_{CC} = +5.0$ Vdc, $V_{EE} = -5.2$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|--------|-------------|--------------|--------------|--------|---------------|
| Operating Supply Currents | 1 | I_{CC} | — | 5.3 | 8.0 | mA |
| | | I_{EE} | — | 22.2 | 28.1 | |
| Input Leakage Current | 1 | I_R | — | — | 0.1 | μA |
| Input Current $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 1 | I_{in} | — | 0.020 | 0.1 | mA |
| | | | — | 0.014 | 0.1 | |
| | | | — | 0.012 | 0.1 | |
| Output Voltage High $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 1 | V_{OH} | -0.825 | -0.900 | -0.990 | Volt |
| | | | -0.690 | -0.780 | -0.850 | |
| | | | -0.535 | -0.62 | -0.700 | |
| Output Voltage Low $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 1 | V_{OL} | -1.580 | -1.83 | — | Volts |
| | | | -1.500 | -1.70 | — | |
| | | | -1.380 | -1.73 | — | |
| Input Voltage Transition Width* $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | | V_{TR} | — | 20 | 50 | mV |
| | | | — | 20 | 50 | |
| | | | — | 30 | 50 | |
| Switching Times Propagation Delay Time Rise Time Fall Time | 2 | t_{pd+} | — | 15 | 20 | ns |
| | | t_{pd-} | — | 25 | 30 | |
| | | t_r | — | 12 | — | |
| | | t_f | — | 23 | — | |
| Parallel Input Impedance ($f = 5.0$ MHz) Capacitance Resistance | | C_p (in) | — | 4.5 | — | pF |
| | | R_p (in) | — | 14 | — | k ohms |
| Common-Mode Input Voltage Range ($T_A = -55$ to $+125^\circ\text{C}$) | 3 | CMV_{Rin} | +3.5 -3.5 | +4.4 -4.2 | — | Volts |
| Power Supply Operating Range | | V_{CC} | +4.75 | +5.0 | +6.00 | Vdc |
| | | V_{EE} | -4.75 | -5.2 | -6.00 | |
| Total Power Dissipation | | P_D | — | 145 | 185 | mW |

*Measurement taken from points of Unity Gain.
Ground unused inputs to assure correct device biasing.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – TERMINAL CURRENTS AND VOLTAGES

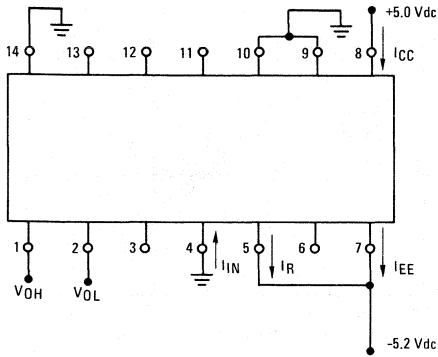


FIGURE 2 – TRANSIENT RESPONSE

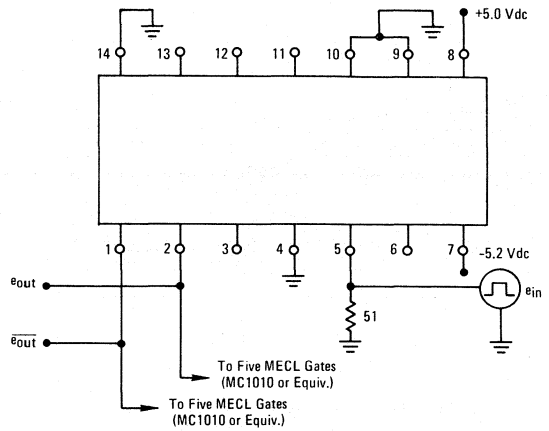
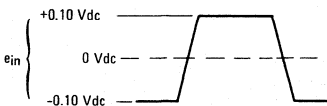
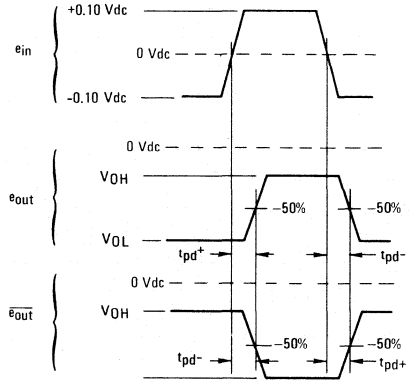
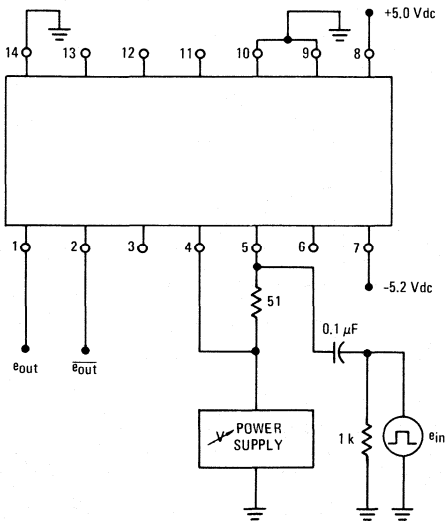


FIGURE 3 – COMMON-MODE INPUT VOLTAGE RANGE



Common-Mode Input Voltage Range is that value of the variable supply (V) which causes a 10% shift in e_{out} or \bar{e}_{out} whichever occurs first.

TYPICAL CHARACTERISTICS

FIGURE 4 – OUTPUT VOLTAGE versus INPUT VOLTAGE AND TEMPERATURE

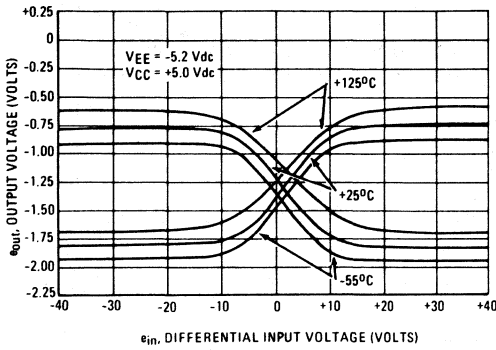


FIGURE 5 – OUTPUT VOLTAGE versus INPUT VOLTAGE AND SUPPLY VARIATION

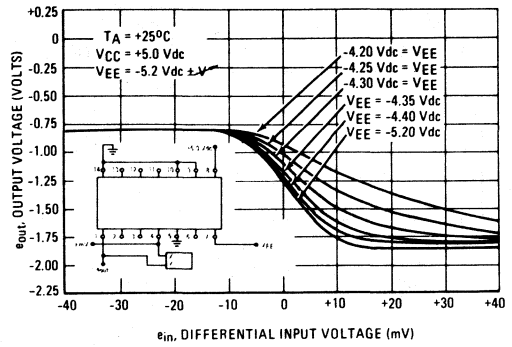


FIGURE 6 – PROPAGATION DELAY versus DIFFERENTIAL INPUT VOLTAGE

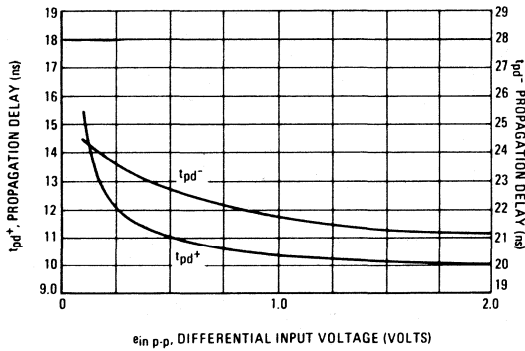


FIGURE 7 – PROPAGATION DELAY versus AMBIENT TEMPERATURE

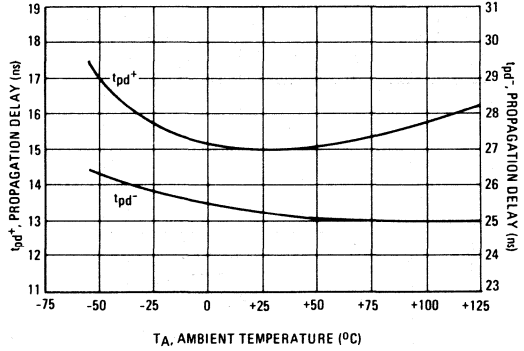
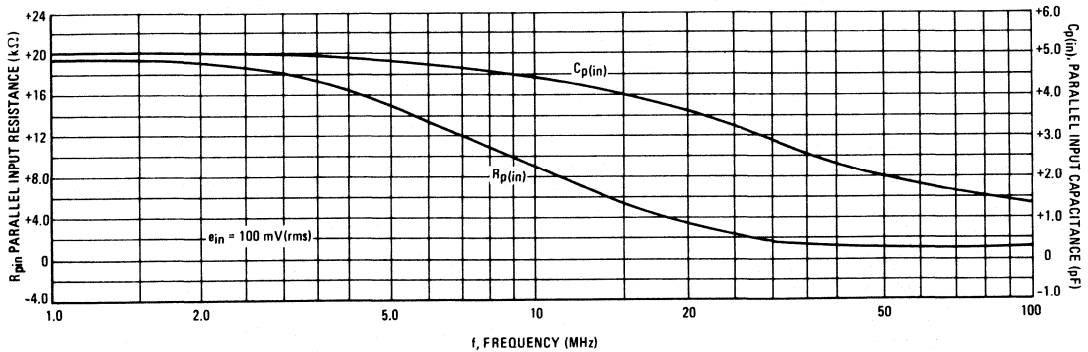


FIGURE 8 – PARALLEL INPUT IMPEDANCE versus FREQUENCY



7

APPLICATIONS INFORMATION

Line Driver/Receiver Family Characteristics

The Motorola line driver/receiver series provides interface circuits for driving digital data transmission lines, e.g., coaxial cable or twisted pair. The digital data transmission is via a balanced differential mode. The line drivers and receivers are designed to provide high common-mode noise rejection, present high impedances to the transmission line and have low propagation times. A feature of the drivers is the capability of operating in a party-line mode whereby a number of drivers can be connected to a single line. The series provides both drivers and receivers compatible with MRTL, MDTL, M TTL and MECL. The five circuits of the family are:

- MC1580L Dual Line Driver/Receiver
- MC1581L Dual MECL Receiver
- MC1582L Dual MDTL/M TTL Driver
- MC1583L Dual Receiver (Open Collector)
- MC1584L Dual Receiver (Active Pullup)

Figure 9 indicates the line drivers and receivers recommended for interfacing with each of the various digital logic families.

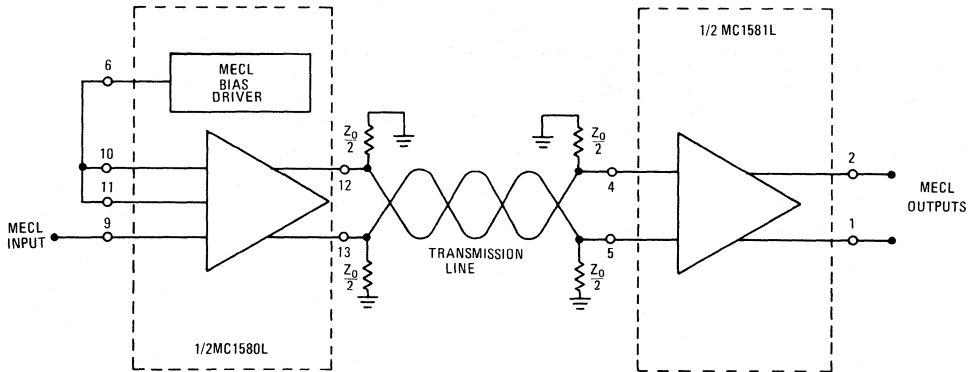
FIGURE 9

| Digital Logic Family | Driver | Receiver |
|----------------------|--------------------|--------------------|
| MECL | MC1580L | MC1581L |
| MDTL | MC1582L | MC1583L MC1584L |
| M TTL | MC1582L | MC1583L MC1584L |
| MRTL | MC1580L MC1582L | MC1583L |

These five circuits are extremely useful in numerous applications other than line drivers and receivers. The differential amplifier input of the receiver makes it useful in such applications as voltage comparators, waveform generators and high-input impedance buffers. The drivers and receivers are useful as logic level translators.

The MC1581L in Figure 10 serves as the line receiver in a balanced differential transmission line. The outputs of the MC1581L receiver and the inputs to the MC1580L driver are compatible with MECL.

FIGURE 10 - MECL COMPATIBLE TRANSMISSION SYSTEM



The output stage of the driver switches a current source between the two driver outputs in response to the input logic signals. Hence, a voltage differential that is a function of the line termination impedances is created on the twisted pair and at the input of the receiver. The receiver is designed to reject +3.5 V/-3.5 V of common-mode voltage signals which may be present due to ground loop currents and noise coupled from nearby transmission lines.

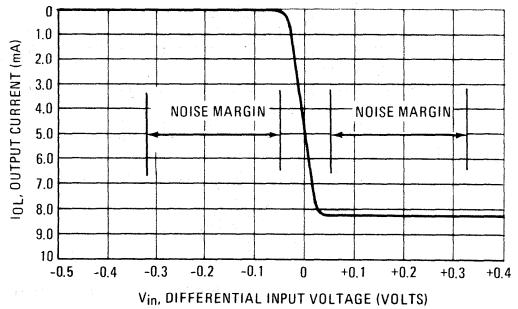
While common-mode noise is the major concern in a twisted pair transmission line, a good data transmission system must offer some immunity from differential-mode voltages that may be present due to mismatches in termination impedances. The drivers and receivers of the MC1580 series are designed with this requirement in mind. The exact amount of noise immunity depends on line impedances but the following example shows how differential-mode noise immunity is calculated for a given system. For a line with a characteristic impedance of Z_0 , calculate the minimum differential input voltage from the equation:

$$\pm V_{in} = \frac{I_0(\min) \times Z_0}{4}$$

For a 170-ohm line, $V_{in} = \frac{(6.9)(170)}{4} = 0.29$ Volts

Since the MC1581L requires a 50 mV maximum input differential to maintain the output state, the worst case differential-mode noise immunity is 0.26 V, (see Figure 11).

FIGURE 11



Hence the direct coupling of the driver and receiver to the line provides a built-in differential-mode noise immunity. The direct coupling also matches the line at all frequencies (often a problem with ac coupled lines). The recovery problem in ac coupling devices at high-signal repetition rates is also eliminated.

High input impedance of the MC1581L and high output impedance of the MC1580L minimize impedance discontinuities on the

APPLICATIONS INFORMATION (continued)

transmission line and allow many drivers and receivers to be connected to the line.

Use of the MC1581L and the MC1580L in a bi-directional MECL compatible transmission system is shown in Figure 12. The MC1580L has an internal MECL bias network that allows the circuit to be used as a MECL line driver. The drivers of Figure 12 are connected so that the current sources from both drivers pull current from the same wire of the twisted pair when both drivers are transmitting logic "0" signals. The external current source, I_S , supplies the current required by one driver. The current for the other driver is drawn from the termination impedances creating a voltage differential across the line. When either driver transmits a logic "1", a voltage difference of the opposite polarity is created across the line. For a system with two drivers the current source (I_S) can be supplied by a 600-ohm resistor connected to +5.0 Volts. If additional drivers are connected to the line, a matching current source must be connected for each added driver. The current sources

are connected to the line so that when all drivers are transmitting logic "0"s, the difference in current drawn from the terminating resistors of the two wires in the twisted pair is equal to one current source (8.6 mA). The current sources should also be connected so that when any driver transmits a logic "1" a current difference of the opposite polarity exists. The matching current source should be the companion circuit on the MC1580L driver chip. The difference in amplitude of the current sources on a single chip is specified to allow the system designer to calculate the maximum current source mismatch, ΔI_{OL} , and hence the maximum number of drivers that can be connected to a given transmission line.

Voltage Translator

Translation of voltage levels from MHTL (tailored for the noisy input/output system portions) to MECL (best suited for the high-speed logic circuits) is often required. The MC1581L performs this function as shown in Figure 13.

FIGURE 12 - BI-DIRECTIONAL TRANSMISSION

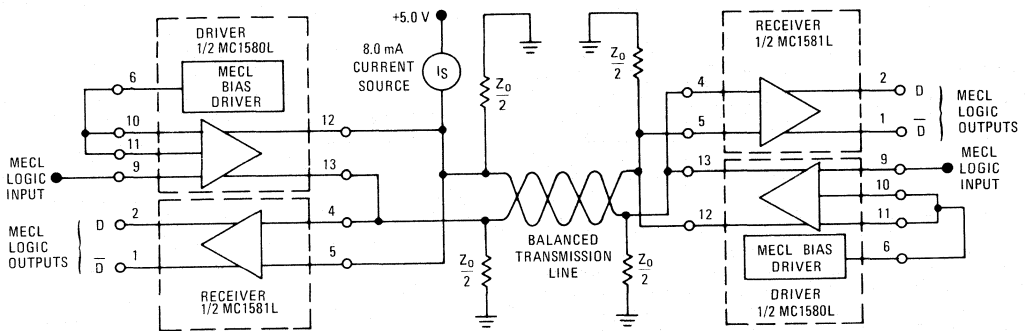
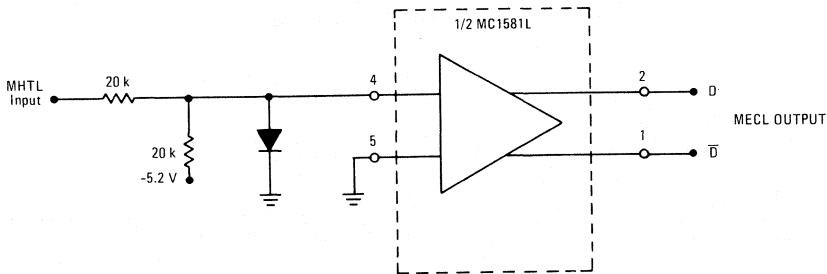


FIGURE 13 - MHTL-TO-MECL VOLTAGE LEVEL TRANSLATOR



MC1582L

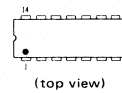
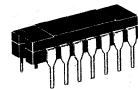
MONOLITHIC DUAL MDTL/MTTL LINE DRIVER

... designed with a three-input AND gate input circuit. The differential output current switches in response to an MDTL or MTTL compatible input voltage level. Typical applications include driving twisted-pair transmission lines, line sharing, and logic level translation.

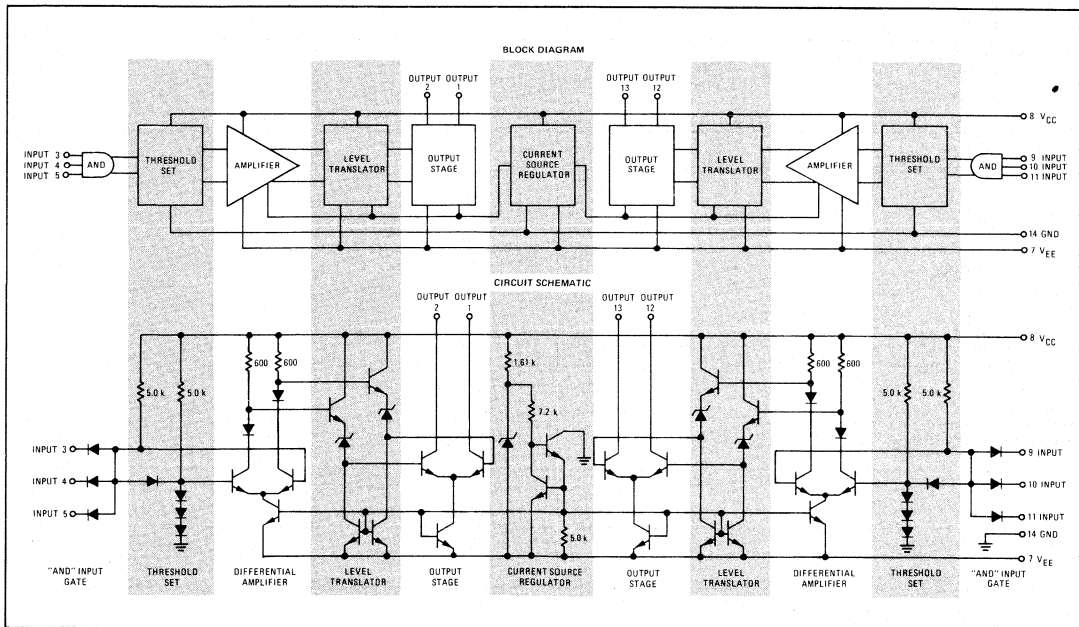
- Low Propagation Delay Time – 20 ns max
- Wide Common-Mode Output Voltage Range – +9.0/-3.0 Volts
- High Output Impedance – 7.0 k Ohms @ 10 MHz
- 3-Input AND Gate
- Device Compatibility with Other Members of the Line Driver/Receiver Series

DUAL MDTL/MTTL LINE DRIVER INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED



CERAMIC PACKAGE
CASE 632
TO-116



MC1582L (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|--------------------------|--------------|----------------------------|
| Power Supply Voltage | V_{CC} V_{EE} | +7.0 -7.0 | Vdc |
| Input Signal Voltage | V_{in} | +30 | Volts |
| Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above $T_A = +25^\circ\text{C}$ | P_D $1/\theta_{JA}$ | 575 3.85 | mW mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +175 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS (Each Line Driver, $V_{CC} = +5.0$ Vdc, $V_{EE} = -5.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|--------|------------------------------|-------------------|----------------------|---------------------|---------------|
| Operating Supply Currents | 1 | I_{CC} I_{EE} | - - | 8.0 25 | 10 30 | mA |
| Input Leakage Current | 1 | I_R | - | 0.04 | 0.1 | μA |
| Input Current $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 1 | I_{in} | - - - | 0.72 0.70 0.63 | 1.0 1.0 1.0 | mA |
| Output Leakage Current | 1 | I_{CEX} | - | 0.8 | 5.0 | μA |
| Output Load Current $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 1 | I_{OL} | 6.5 6.9 6.8 | 8.1 8.6 8.5 | 9.8 10.4 10.2 | mA |
| Output Load Current Match $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 2 | ΔI_{OL} | - - - | 0.7 0.8 0.8 | - - - | mA |
| Input Voltage Transition Width* $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | | V_{TR} | - - - | 50 40 50 | - - - | mV |
| Switching Times Propagation Delay Time | 3 | t_{pd+} t_{pd-} | - - | 15 13 | 20 18 | ns |
| Rise Time Fall Time | | t_r t_f | - - | 8.0 7.0 | - - | |
| Threshold Voltage $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 3 | V_{TH} | 0.9 1.1 0.9 | 1.74 1.45 1.16 | 2.0 1.8 1.5 | Volts |
| Parallel Output Impedance ($f = 5.0$ MHz) Capacitance Resistance | | $C_{p(out)}$ $R_{p(out)}$ | - - | 10 18 | - - | pF k ohms |
| Common-Mode Output Voltage Range $T_A = -55$ to $+125^\circ\text{C}$ | 4 | $CMVR_{out}$ | +9.0 -3.0 | +10 -3.3 | - - | Volts |
| Power Supply Operating Range | | V_{CC} V_{EE} | +4.75 -6.0 | +5.0 -5.0 | +6.0 -4.75 | Vdc |
| Input Breakdown Voltage | | V_{IHh} | 15 | 30 | - | Volts |
| Power Dissipation | | P_D | - | 140 | 170 | mW |

*Measured from points of unity gain with a 50 ohm load.
Ground all unused input pins to assure correct device biasing.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – TERMINAL CURRENTS

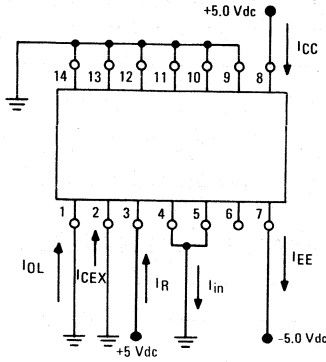


FIGURE 2 – OUTPUT CURRENT MATCH

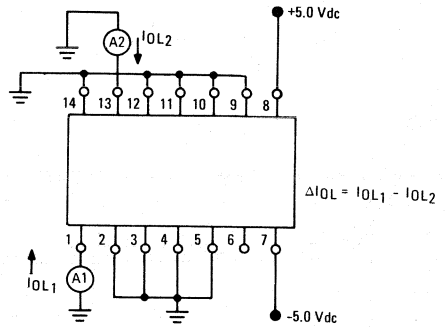


FIGURE 3 – TRANSIENT RESPONSE

All t_r and t_f measured 10% to 90%

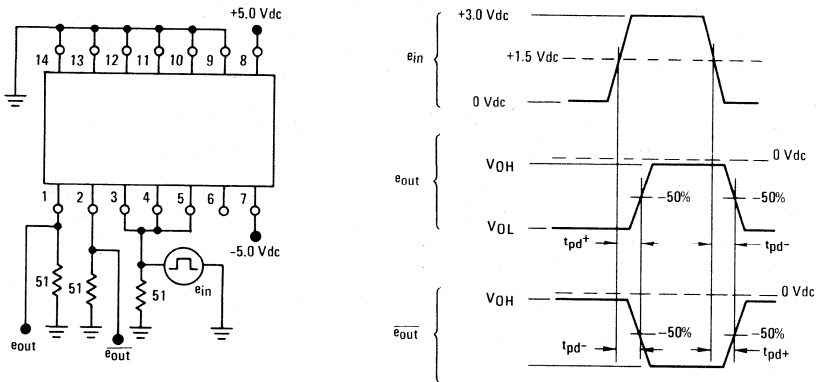
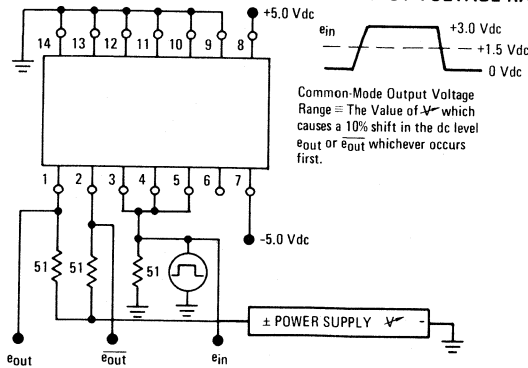


FIGURE 4 – COMMON-MODE OUTPUT VOLTAGE RANGE



TYPICAL CHARACTERISTICS

FIGURE 5 – OUTPUT LOAD CURRENT versus SUPPLY OPERATING VOLTAGE AND TEMPERATURE

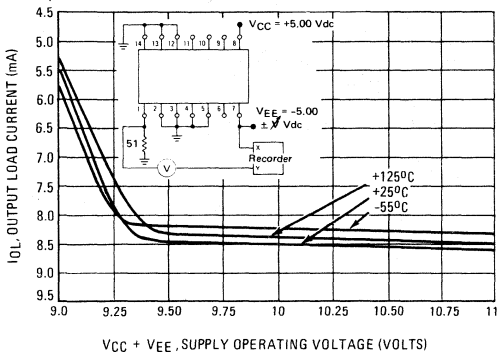


FIGURE 6 – OUTPUT LOAD CURRENT versus INPUT VOLTAGE AND TEMPERATURE

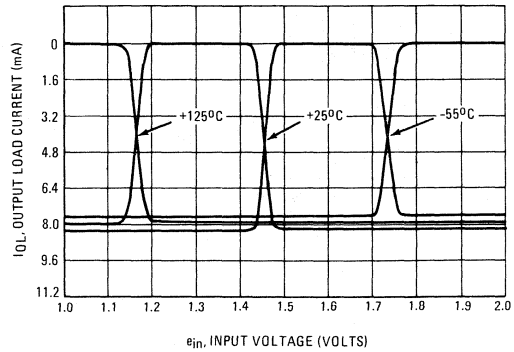


FIGURE 7 – PROPAGATION DELAY TIME versus AMBIENT TEMPERATURE

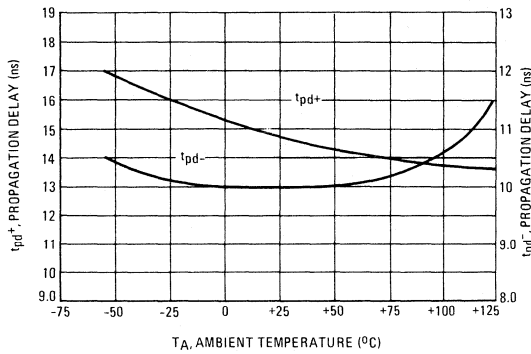
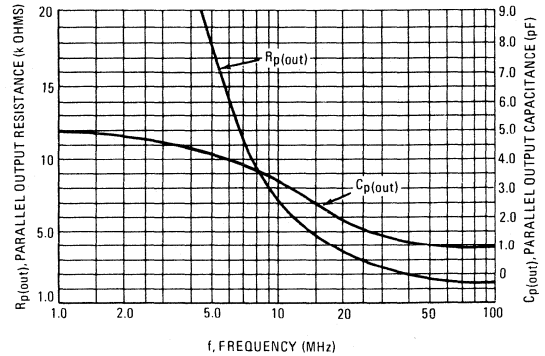


FIGURE 8 – PARALLEL OUTPUT IMPEDANCE versus FREQUENCY



7

APPLICATIONS INFORMATION

Line Driver/Receiver Family Characteristics

The Motorola line driver/receiver series provides interface circuits for driving digital data transmission lines e.g., coaxial cable or twisted pair. The digital data transmission is via a balanced differential mode. The line drivers and receivers are designed to provide high common-mode noise rejection, present high impedances to the transmission line and have low propagation times. A feature of the drivers is the capability to operate in a party-line mode whereby a number of drivers can be connected to a single line. This series provides drivers and receivers compatible with MRTL, MDTL, MTTL and MECL. The five circuits of the family are:

- MC1580L Dual Line Driver/Receiver
- MC1581L Dual MECL Receiver
- MC1582L Dual MDTL/MTTL Driver
- MC1583L Dual Receiver (Open Collector)
- MC1584L Dual Receiver (Active Pullup)

Figure 9 indicates line drivers and receivers recommended for interfacing with each of the various digital logic families.

FIGURE 9

| Digital Logic Family | Driver | Receiver |
|----------------------|--------------------|--------------------|
| MECL | MC1580L | MC1581L |
| MDTL | MC1582L | MC1583L MC1584L |
| MTTL | MC1582L | MC1583L MC1584L |
| MRTL | MC1580L MC1582L | MC1583L |

These five circuits are extremely useful in numerous applications other than line drivers and receivers. The differential amplifier input of the receiver makes it useful in applications such as voltage comparators, waveform generators and high-input-impedance buffers. The drivers and receivers are useful as logic level translators.

The MC1582L in Figure 10 serves as the line driver for a balanced differential transmission line. The driver input and receiver outputs of the MC1584L receiver are compatible with MTTL circuits.

The output stage of the driver switches a current source between the two driver outputs in response to the input logic signals. Hence, a voltage differential that is a function of the line termination impedances is created on the twisted pair and at the input of the receiver. The receiver is designed to reject +3.5/-3.5 Volts of common-mode voltage signals which may be present due to ground loop currents and noise coupled from nearby transmission lines.

While common-mode noise is the major concern in a twisted pair transmission line; a good data transmission system must offer some immunity from differential-mode voltages that may be present due to mismatches in termination impedances. The drivers and receivers of the MC1580 Series are designed with this requirement in mind. The exact amount of noise immunity depends on line impedances but the following example shows how differential-mode noise immunity is calculated for a given system. For a line with a characteristic impedance of Z_0 , calculate the minimum differential input voltage from the equation.

$$\pm V_{in} = \frac{I_o(\min) \times Z_0}{4}$$

For a 170-ohm line, $V_{in} = \frac{(6.9)(170)}{4} = 0.29$ Volts.

Since the receivers recommended for use with the MC1582L driver require 50 mV maximum input differential to maintain the output state, the worst case differential-mode noise immunity is 0.26 V. (See Figure 11).

FIGURE 11

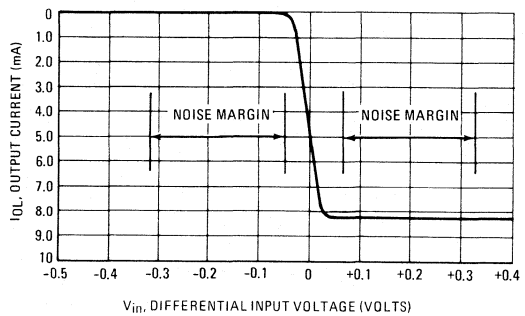
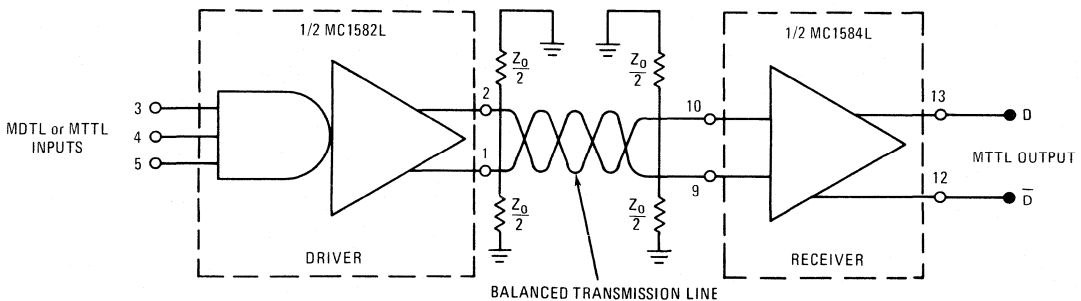


FIGURE 10 – MDTL, MTTL COMPATIBLE TRANSMISSION SYSTEM



APPLICATIONS INFORMATION (continued)

Hence the direct coupling of the driver and receiver to the line provides a built-in differential-mode noise immunity. The direct coupling also matches the line at all frequencies (often a problem with ac coupling lines). The recovery problem in ac coupling devices at high-signal repetition rates is also eliminated.

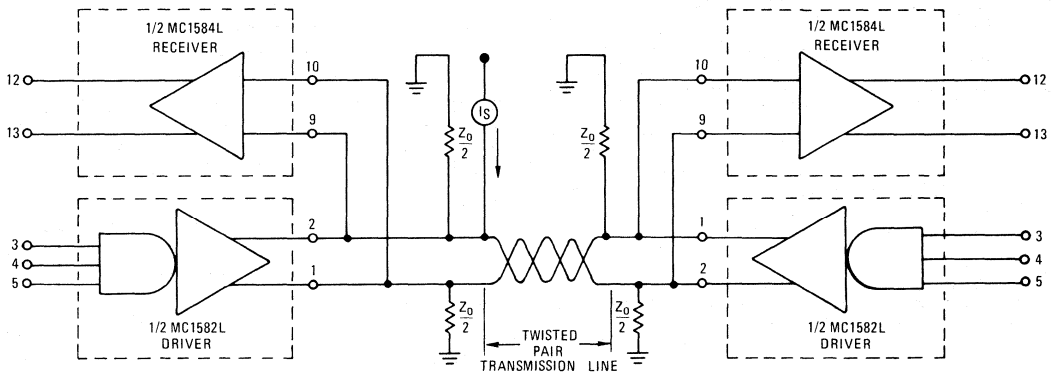
The high output impedance of the MC1582L and the high input impedances of the MC1584L drivers minimize impedance discontinuities on the transmission line and allow many drivers and receivers to be connected to the line.

Use of the MC1584L in a bi-directional MDTL or MTTL compatible transmission system is shown in Figure 12. The MC1582L drivers of Figure 12 are connected so that the current sources from both drivers pull current from the same wire of the twisted pair when both drivers are transmitting logic "0" signals. The external current source, I_S , supplies the current required by one driver. The current for the other driver is drawn from the termination impedances, creating a voltage differential across the line. When either

driver transmits a logic "1", a voltage difference of the opposite polarity is created across the line. For a system with two drivers the current source (I_S) can be supplied by a 600-ohm resistor connected to +5.0 volts.

If additional drivers are connected to the line, a matching current source is connected for each added driver. The current sources are connected to the line so that when all drivers are transmitting logic "0's, the difference in current drawn from the terminating resistors of the two wires in the twisted pair is equal to one current source (8.6 mA). The current sources should also be connected so that when any driver transmits a logic "1" then a current difference of the opposite polarity exists. The matching current source should be the companion circuit on the MC1580L driver chip. The difference in amplitude of the current sources on a single chip is specified to allow the system designer to calculate the maximum current source mismatch, ΔI_{OL} , and hence the maximum number of drivers that can be connected to a given transmission line.

FIGURE 12 - BI-DIRECTIONAL TRANSMISSION



MC1583L

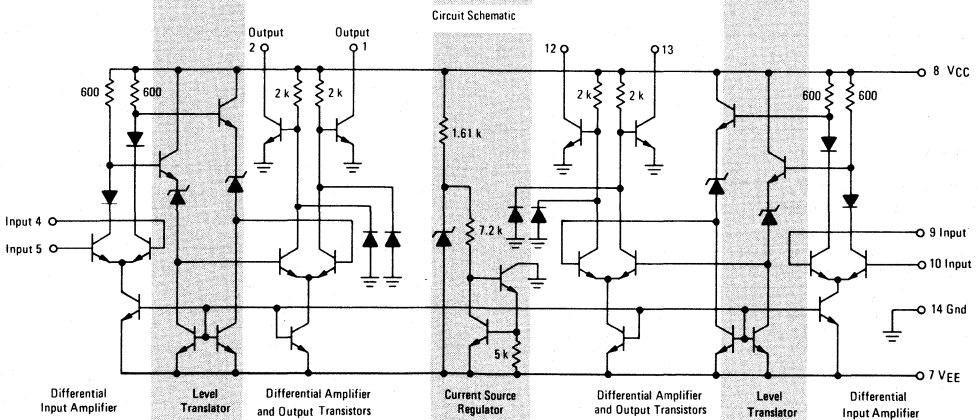
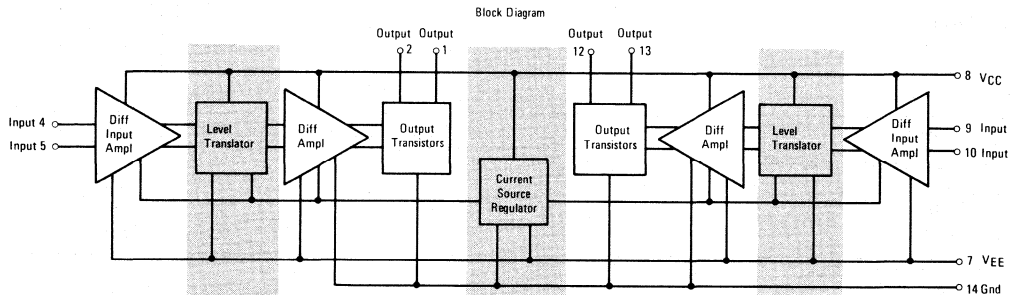
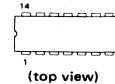
MONOLITHIC DUAL LINE RECEIVER

The MC1583L is a dual open collector output line receiver designed for use in line sharing, differential voltage comparator, and level translator applications. The output transistors switch in response to a differential input voltage. Output logic voltage levels are compatible with MTTL, MDTL, and MRTL logic levels when a suitable external pullup resistor is connected to the device output. Excellent common-mode input voltage range makes this device ideal for receiving digital data in a noisy environment.

- High Input Impedance – 12 Kiloohms @ 5.0 MHz
- Low Propagation Delay Time – 40 ns max
- Excellent Common-Mode Input Voltage Range – ± 3.5 V min
- Compatible with Other Members of the Line Driver/Receiver Series – MC1580 thru MC1584

DUAL SATURATED LOGIC RECEIVER (OPEN-COLLECTOR) MONOLITHIC SILICON EPITAXIAL PASSIVATED

CERAMIC PACKAGE
CASE 632
TO-116



See Packaging Information Section for outline dimensions.

MC1583L (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|------------|-------------|----------------------|
| Power Supply Voltage | V_{CC} | +7.0 | Vdc |
| | V_{EE} | -7.0 | Vdc |
| Differential-Mode Input Signal Voltage | V_{in} | ± 7.0 | Vdc |
| Common-Mode Input Voltage | CMV_{in} | ± 10 | Vdc |
| Static Output Load Current | I_{OL} | 20 | mA |
| Power Dissipation (Package Limitation) Derate above $T_A = +25^\circ\text{C}$ | P_D | 575 | mW |
| | | 3.85 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +175 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS (Each Receiver)

($V_{CC} = +5.0$ Vdc, $V_{EE} = -5.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|--------|--|------|-------|-------|---------------|
| Operating Supply Currents | 1 | I_{CC} | — | 15 | 18 | mA |
| | | I_{EE} | — | 16 | 20 | mA |
| Input Leakage Current | 1 | I_R | — | 0.012 | 0.1 | μA |
| Input Current $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 1 | I_{in} | — | 0.033 | 0.1 | mA |
| | | | — | 0.025 | 0.1 | |
| | | | — | 0.020 | 0.1 | |
| Output Leakage Current | 1 | I_{CEX} | — | 0.8 | 5.0 | μA |
| Output Voltage Low ($I_{OL} = 20$ mA) $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | 1 | V_{OL} | — | 0.23 | 0.40 | Volt |
| | | | — | 0.25 | 0.40 | |
| | | | — | 0.28 | 0.40 | |
| Input Voltage Transition Width \ddagger $T_A = -55^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $T_A = +125^\circ\text{C}$ | | V_{TR} | — | 12 | 50 | mV |
| | | | — | 4.0 | 50 | |
| | | | — | 8.0 | 50 | |
| Switching Times | 2 | t_{pd+} t_{pd-} t_r t_f | — | 24 | 30 | ns |
| | | | — | 34 | 40 | |
| | | | — | 16 | — | |
| | | | — | 5.0 | — | |
| Parallel Input Impedance ($f = 5.0$ MHz) | | C_p R_p | — | 4.0 | — | pF k ohms |
| | | | — | 12 | — | |
| Common-Mode Input Voltage Range $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ | 3 | CMV_{in} | +3.5 | +4.3 | — | Volts |
| | | | -3.5 | -4.2 | — | |
| Power Supply Operating Range | | V_{CC} V_{EE} | 4.75 | 5.0 | 6.0 | Vdc |
| | | | -6.0 | -5.0 | -4.75 | |
| Total Power Dissipation | | P_D | — | 140 | 175 | mW |

Ground unused input pins to assure correct device biasing.

\ddagger Measurement taken from points of Unity Gain with 3.9-kilohm load resistor.

MC1583L (continued)

TEST CIRCUITS AND TYPICAL CHARACTERISTICS

($V_{CC} = +5.0$ Vdc, $V_{EE} = -5.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 1 – TERMINAL CURRENTS

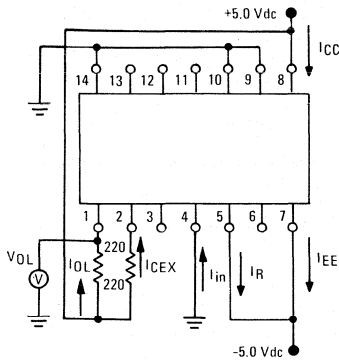


FIGURE 2 – TRANSIENT RESPONSE

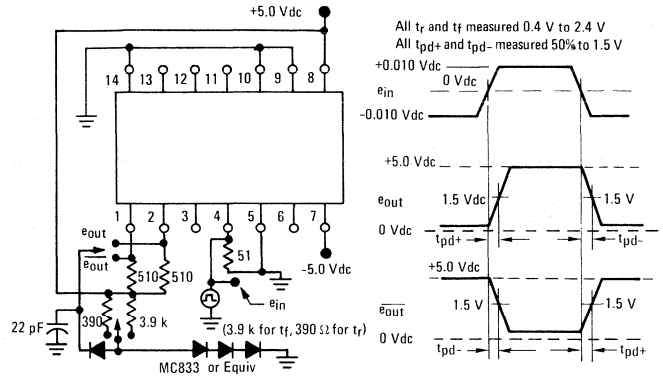


FIGURE 3 – COMMON-MODE INPUT VOLTAGE RANGE

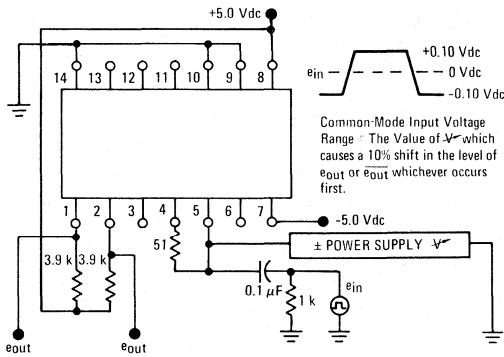


FIGURE 5 – OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE AND TEMPERATURE

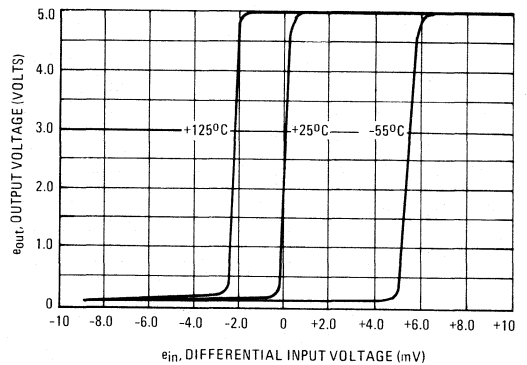
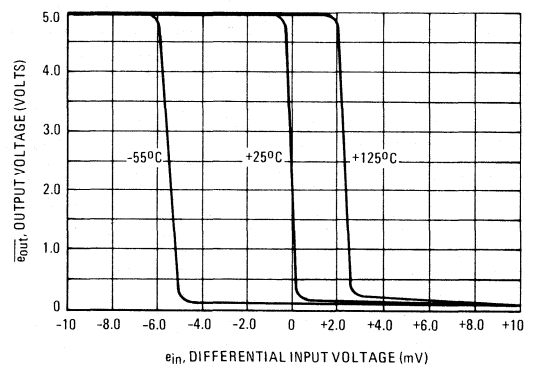
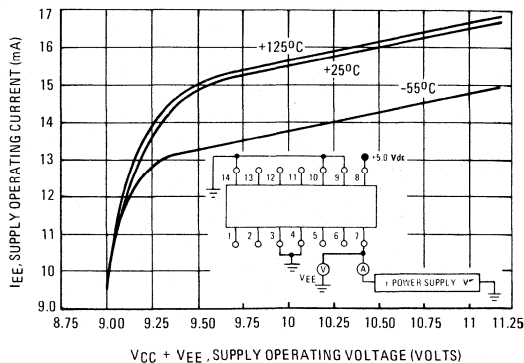


FIGURE 4 – SUPPLY OPERATING CURRENT versus SUPPLY OPERATING VOLTAGE AND TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

($V_{CC} = +5.0$ Vdc, $V_{EE} = -5.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 6 – OUTPUT SATURATION VOLTAGE versus OUTPUT LOAD CURRENT AND TEMPERATURE

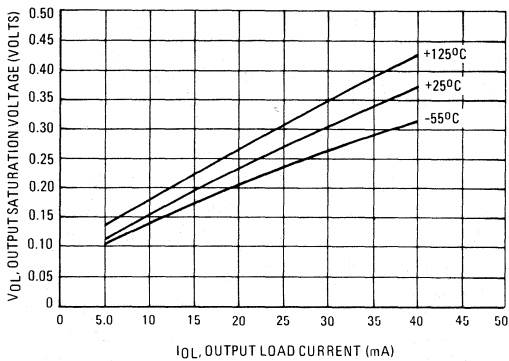


FIGURE 7 – PROPAGATION DELAY versus DIFFERENTIAL INPUT VOLTAGE

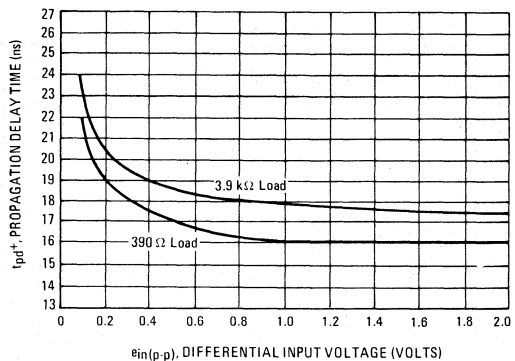


FIGURE 8 – PROPAGATION DELAY versus DIFFERENTIAL INPUT VOLTAGE

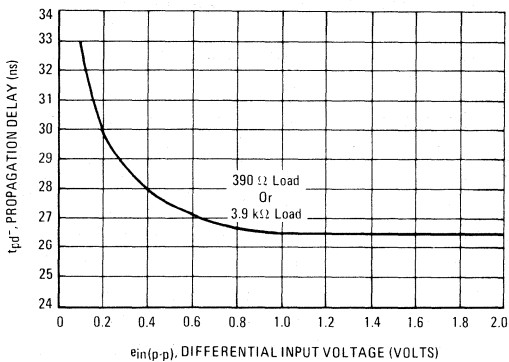


FIGURE 9 – PROPAGATION DELAY versus AMBIENT TEMPERATURE

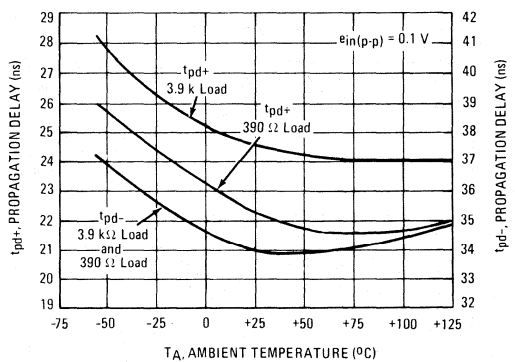
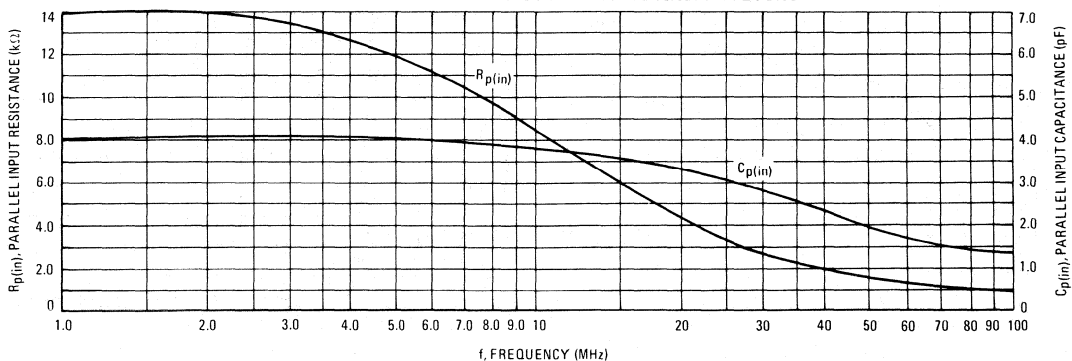


FIGURE 10 – PARALLEL INPUT IMPEDANCE versus FREQUENCY



APPLICATIONS INFORMATION

Line Driver/Receiver Family Characteristics

The Motorola line driver/receiver series provides interface circuits for driving digital data transmission lines e.g., coaxial cable or twisted pair. The digital data transmission is via a balanced differential mode. The line drivers and receivers are designed to provide high common-mode noise rejection, present high impedances to the transmission line and have low propagation times. A feature of the drivers is the capability to operate in a party-line mode whereby a number of drivers can be connected to a single line. This series provides drivers and receivers compatible with MRTL, MDTL, MTTL and MECL. The five circuits of the family are:

- MC1580L Dual Line Driver/Receiver
- MC1581L Dual MECL Receiver
- MC1582L Dual MDTL/MTTL Driver
- MC1583L Dual Receiver (Open Collector)
- MC1584L Dual Receiver (Active Pullup)

Figure 11 indicates line drivers and receivers recommended for interfacing with each of the various digital logic families.

These five circuits are extremely useful in numerous applications other than line drivers and receivers. The differential amplifier input of the receiver makes it useful in applications such as voltage

FIGURE 11

| Digital Logic Family | Driver | Receiver |
|----------------------|--------------------|--------------------|
| MECL | MC1580L | MC1581L |
| MDTL | MC1582L | MC1583L MC1584L |
| MTTL | MC1582L | MC1583L MC1584L |
| MRTL | MC1580L MC1582L | MC1583L |

comparators, waveform generators and high-input-impedance buffers. The drivers and receivers are useful as logic level translators.

The MC1583L in Figure 12 serves as a line receiver for a balanced differential transmission line. The driver inputs and receiver outputs of Figure 12 are compatible with MTTL and MDTL circuits. The MC1583L has an open collector output circuit which is designed to sink 20 mA. The open collector allows the user to interface with MRTL, MDTL, or MTTL by supplying the appropriate external resistor and power supply connection. A 9-volt V_{CE0} rating on the open collector transistor allows the MC1583L to interface with MHTL also.

The MC1584L receiver can also be used to interface with MDTL and MTTL. The MC1584L contains an active pullup on the

output device and hence eliminates the need for an external resistor for MTTL and MDTL compatible systems. The MC1584L has a 6-mA output sink current limitation.

The output stage of the MC1582L driver switches a current source between the two driver outputs in response to the input logic signals. Hence, a voltage differential that is a function of the line termination impedances is created on the twisted pair and at the input of the receiver. The receiver MC1583L is designed to reject +3.5/-3.5 Volts of common-mode voltage signals which may be present due to ground loop currents and noise coupled from nearby transmission lines.

While common-mode noise is the major concern in a twisted pair transmission line; a good data transmission system must offer some immunity from differential-mode voltages that may be present due to mismatches in termination impedances. The drivers and receivers of the MC1580 Series are designed with this requirement in mind. The exact amount of noise immunity depends on line impedances but the following example shows how differential-mode noise immunity is calculated for a given system. For a line with a characteristic impedance of Z_0 , calculate the minimum differential input voltage from the equation.

$$\pm V_{in} = \frac{I_o(\text{min}) \times Z_0}{4}$$

For a 170-ohm line, $V_{in} = \frac{(6.9)(170)}{4} = 0.29$ Volts.

Since the MC1583L requires 50 mV maximum input differential to maintain the output state, the worst case differential-mode noise immunity is 0.26 V. (See Figure 13).

FIGURE 13

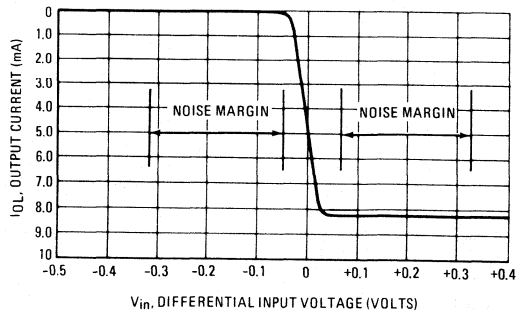
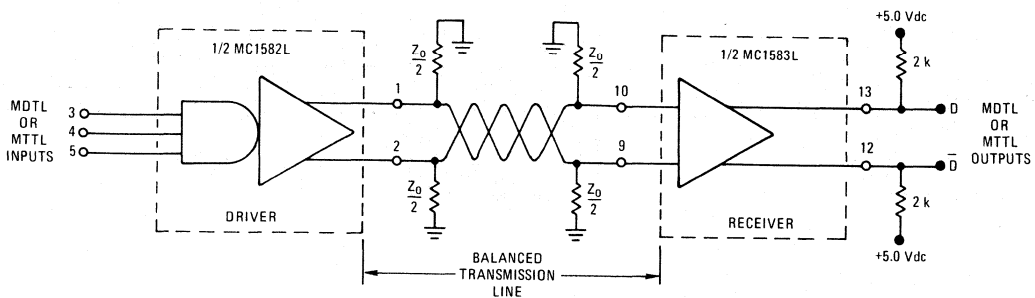


FIGURE 12 - MDTL, MTTL COMPATIBLE TRANSMISSION SYSTEM



APPLICATIONS INFORMATION (continued)

Hence the direct coupling of the driver and receiver to the line provides a built-in differential-mode noise immunity. The direct coupling also matches the line at all frequencies (often a problem with ac coupling lines). The recovery problem in ac coupling devices at high-signal repetition rates is also eliminated.

High input impedance of the MC1583L and high output impedances of the MC1582L minimize impedance discontinuities on the transmission line and allow many drivers and receivers to be connected to the line.

Using MC1580L as a driver and MC1583L as the receiver in a MRTL compatible transmission system is shown in Figure 14.

Use of the MC1583L in a bi-directional MDTL or MTTTL compatible transmission system is shown in Figure 15. The MC1582L drivers of Figure 15 are connected so that the current sources from both drivers pull current from the same wire of the twisted pair when both drivers are transmitting logic "0" signals. The external current source, I_S , supplies the current required by one driver. The current for the other driver is drawn from the termination imped-

ances creating a voltage differential across the line. When either driver transmits a logic "1", a voltage difference of the opposite polarity is created across the line. For a system with two drivers the current source (I_S) can be supplied by a 600-ohm resistor connected to +5.0 Volts. If additional drivers are connected to the line, a matching current source must be connected for each added driver. The current sources are connected to the line so that when all drivers are transmitting logic "0's, the difference in current drawn from the terminating resistors of the two wires in the twisted pair is equal to one current source (8.6 mA). The current sources should also be connected so that when any driver transmits a logic "1" a current difference of the opposite polarity exists. The matching current source should be the companion circuit on the various driver chips. The difference in amplitude of the current sources on a single chip is specified to allow the system designer to calculate the maximum current source mismatch, ΔI_{OL} , and hence the maximum number of drivers that can be connected to a given transmission line.

FIGURE 14 – MRTL COMPATIBLE TRANSMISSION SYSTEM

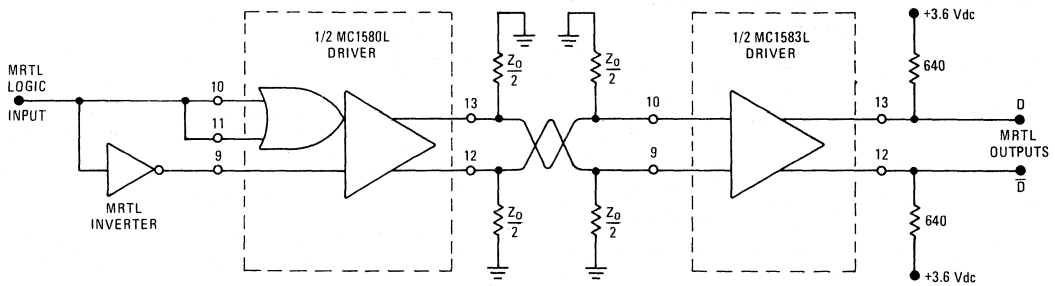
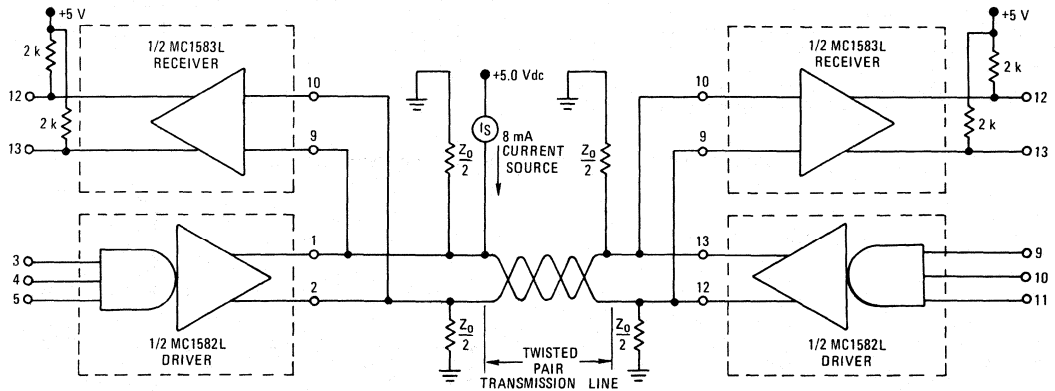


FIGURE 15 – BI-DIRECTIONAL TRANSMISSION



7

MC1583L (continued)

APPLICATIONS INFORMATION (continued)

The MC1583L has many other uses in a digital system. The high input impedance suggests its use as a buffer for delay lines and in waveform generation circuits. Figure 16 shows the MC1583L used as a differential comparator in a double-ended limit detector. When the input signal amplitude is between the two reference voltages, the output signal will be a logic "1"; otherwise a logic "0" output is obtained. The voltage transition region is typically 8 to

12 mV. External component R1 establishes an MDTL compatible output signal.

VOLTAGE TRANSLATOR

Translation of voltage levels from MECL (best suited for the high-speed portion of a digital system) to MHTL (tailored for the noisy output portion of the system) is often required. The MC1583L performs this function as indicated in Figure 17.

FIGURE 16 – DOUBLE-ENDED LIMIT DETECTOR

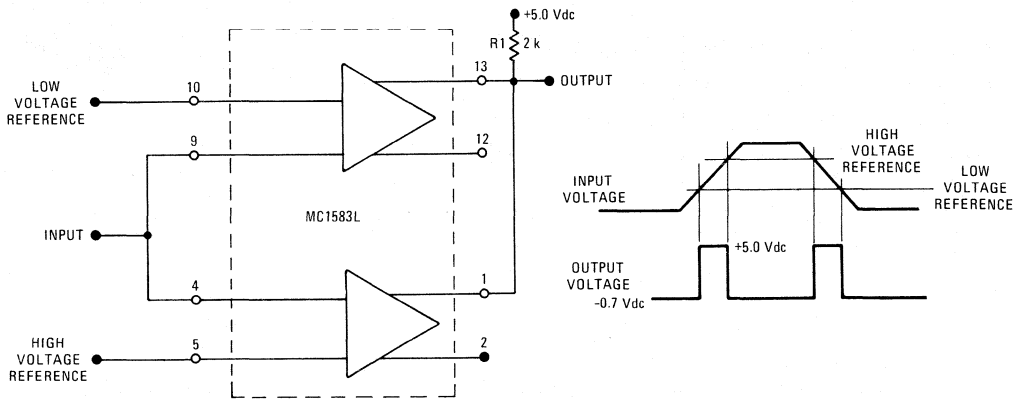
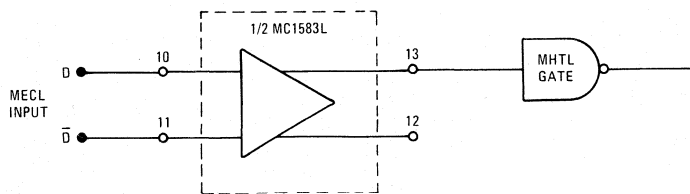


FIGURE 17 – MECL TO MHTL VOLTAGE LEVEL TRANSLATOR



LINEAR/DIGITAL INTERFACE CIRCUITS

MC1584L

MONOLITHIC DUAL MDTL/MTTL RECEIVER

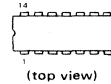
... designed with an active pull-up output that switches in response to a differential input voltage. This silicon device is compatible with the MDTL and MTTL digital logic families. Excellent common-mode input voltage range makes the device ideal for receiving digital information in a noisy environment. The "totem-pole" output (active pullup configuration) affords satisfactory response coupled with power savings for operation with a small number of unit loads. Typical applications include line sharing, voltage comparator, and logic level translation.

- High Input Impedance – 7.0 k ohms @ 10 MHz typ
- Low Propagation Delay Time – 37 ns max
- Wide Common-Mode Input Voltage Range ± 3.5 Volts min
- Device Compatibility with other Members of the Line Driver/Receiver Series

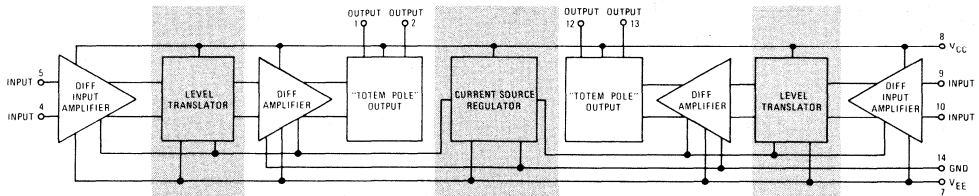
**DUAL MDTL/MTTL RECEIVER
(ACTIVE PULLUP)
INTEGRATED CIRCUIT**

**MONOLITHIC SILICON
EPITAXIAL PASSIVATED**

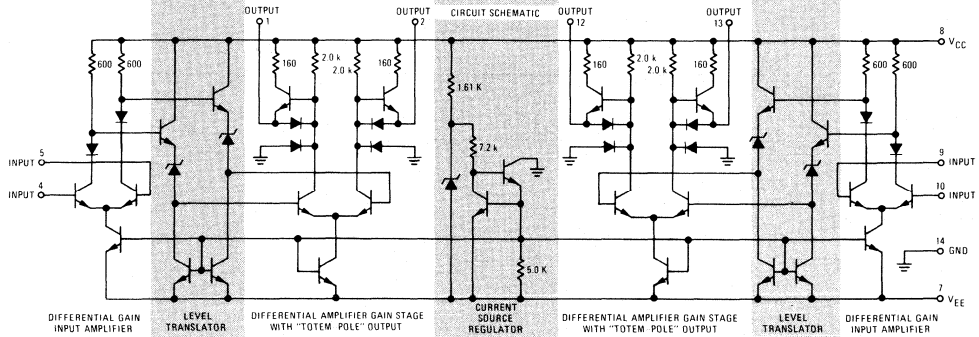
CERAMIC PACKAGE
CASE 632
TO-116



BLOCK DIAGRAM



CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MC1584L (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|-------------------|-------------|-------|
| Power Supply Voltage | V _{CC} | +7.0 | Vdc |
| | V _{EE} | -7.0 | |
| Differential-Mode Input Signal Voltage | V _{in} | ±7.0 | Volts |
| Common-Mode Input Signal Voltage | CMV _{in} | ±10 | Volts |
| Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T _A = +25°C | P _D | 575 | mW |
| | 1/θ _{JA} | 3.85 | mW/°C |
| Operating Temperature Range | T _A | -55 to +125 | °C |
| Storage Temperature Range | T _{stg} | -65 to +175 | °C |

ELECTRICAL CHARACTERISTICS (Each Receiver, V_{EE} = +5.0 V, V_{CC} = -5.0 V, T_A = +25°C unless otherwise noted)

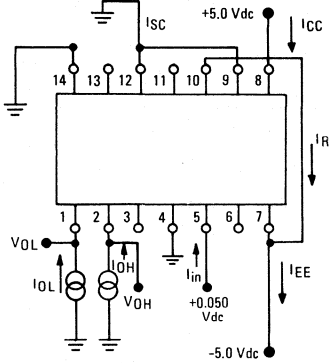
| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|--|--------|--------------------|-------|-------|------|--------|
| Operating Supply Currents | 1 | I _{CC} | - | 11.5 | 15 | mA |
| | | I _{EE} | - | 25 | 31 | |
| Input Leakage Current | 1 | I _R | - | 0.009 | 0.1 | μA |
| Input Current T _A = -55°C T _A = +25°C T _A = +125°C | 1 | I _{in} | - | 0.024 | 0.1 | mA |
| | | | - | 0.016 | 0.1 | |
| | | | - | 0.011 | 0.1 | |
| Output Voltage High (I _{OH} = -0.7 mA) T _A = -55°C T _A = +25°C T _A = +125°C | 1 | V _{OH} | 2.4 | 4.0 | - | Volts |
| | | | 2.4 | 4.0 | - | |
| | | | 2.4 | 4.0 | - | |
| Output Voltage Low (I _{OL} = 4.0 mA) T _A = -55°C to +125°C | 1 | V _{OL} | - | 100 | 400 | mV |
| Output Short-Circuit Current | 1 | I _{SC} | - | 30 | 40 | mA |
| Input Voltage Transition Width* T _A = -55°C T _A = +25°C T _A = +125°C | | V _{TR} | - | 20 | 60 | mV |
| | | | - | 25 | 60 | |
| | | | - | 30 | 60 | |
| Switching Times Propagation Delay Time Rise Time Fall Time | 2 | t _{pd+} | - | 32 | 37 | ns |
| | | t _{pd-} | - | 28 | 33 | |
| | | t _r | - | 14 | - | |
| | | t _f | - | 12 | - | |
| Parallel Input Impedance (f = 5.0 MHz) Capacitance Resistance | | C _{p(in)} | - | 5.0 | - | pF |
| | | R _{p(in)} | - | 11 | - | k ohms |
| Common-Mode Input Voltage Range T _A = -55 to +125°C | 3 | CMV _{Rin} | 3.5 | +4.3 | - | Volts |
| | | | 3.5 | -4.2 | - | |
| Power Supply Operating Range | | V _{CC} | +4.75 | +5.0 | +6.0 | Vdc |
| | | V _{EE} | -4.75 | -5.0 | -6.0 | |
| Power Dissipation | | P _D | - | 170 | 200 | mW |

Ground all unused input pins to assure correct device biasing.

*Measured from points of unity gain.

7

FIGURE 1 – TERMINAL CURRENTS



CHARACTERISTIC DEFINITIONS

FIGURE 2 – TRANSIENT RESPONSE

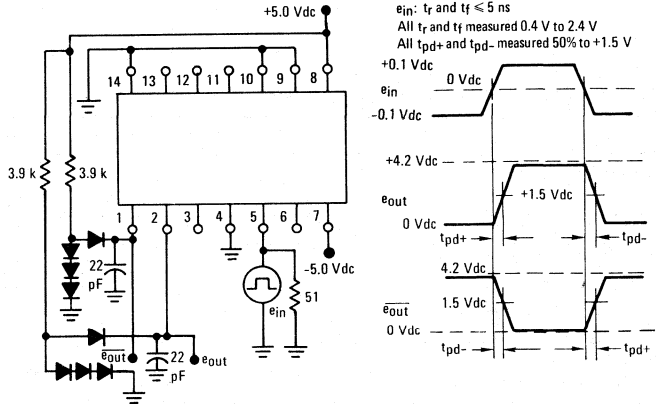
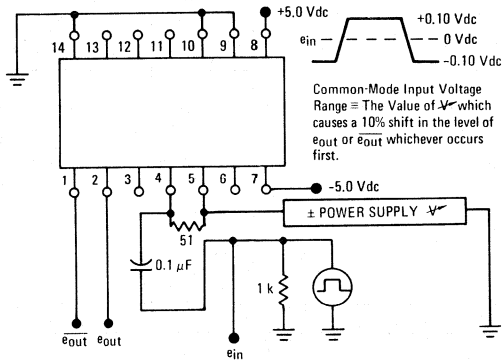


FIGURE 3 – COMMON-MODE INPUT VOLTAGE RANGE



TYPICAL CHARACTERISTICS

($V_{EE} = +5.0$ Vdc, $V_{CC} = -5.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 4 — OUTPUT VOLTAGE HIGH versus SUPPLY OPERATING VOLTAGE AND TEMPERATURE

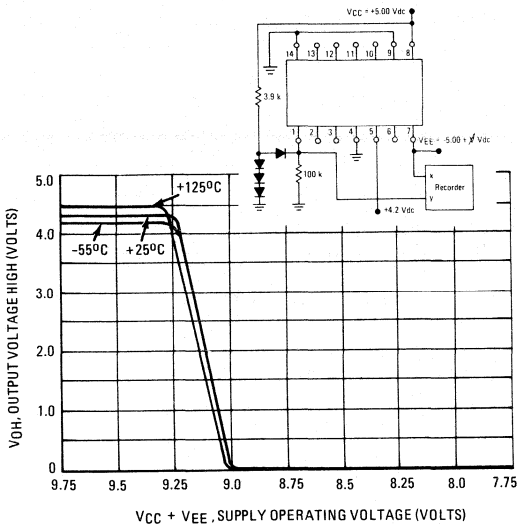


FIGURE 5 — OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE AND TEMPERATURE

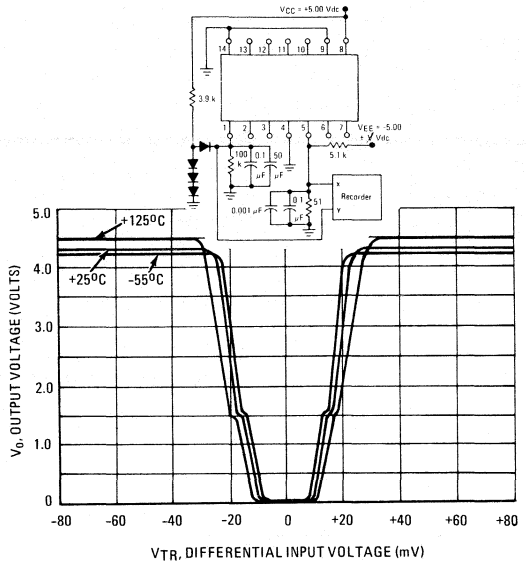


FIGURE 6 — OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE AND VARIOUS LOADS

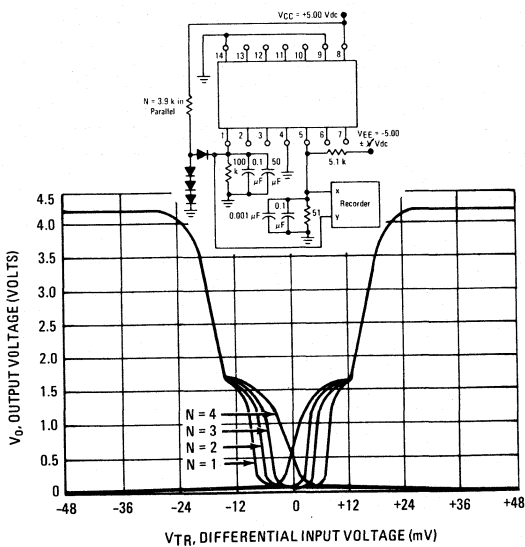
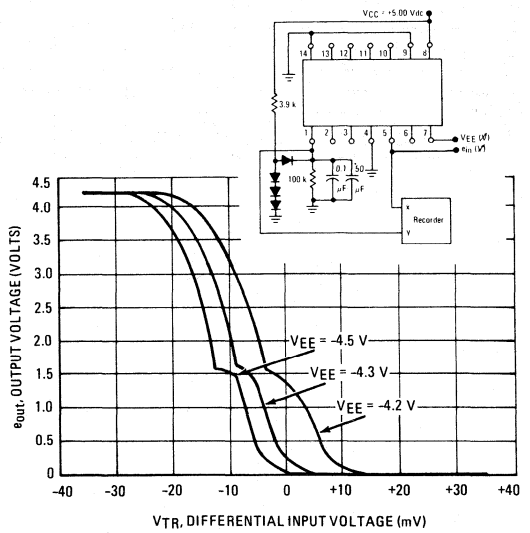


FIGURE 7 — OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE AND VARIATIONS IN NEGATIVE SUPPLY



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – PROPAGATION DELAY versus DIFFERENTIAL INPUT VOLTAGE

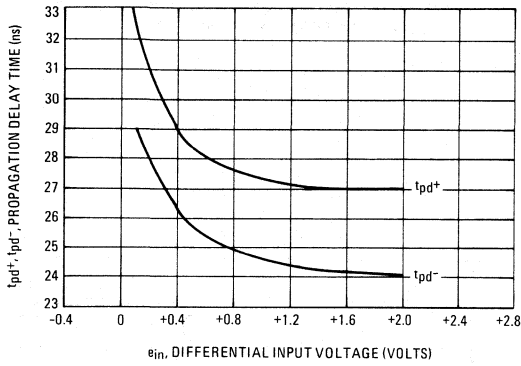


FIGURE 9 – PROPAGATION DELAY versus AMBIENT TEMPERATURE

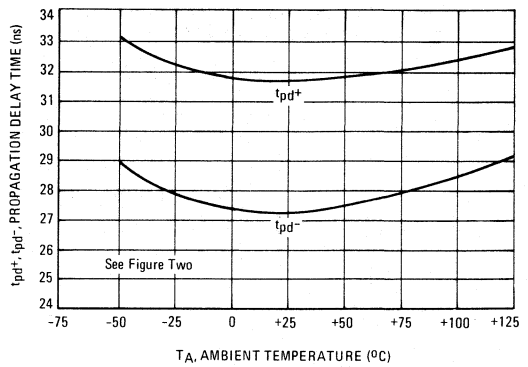
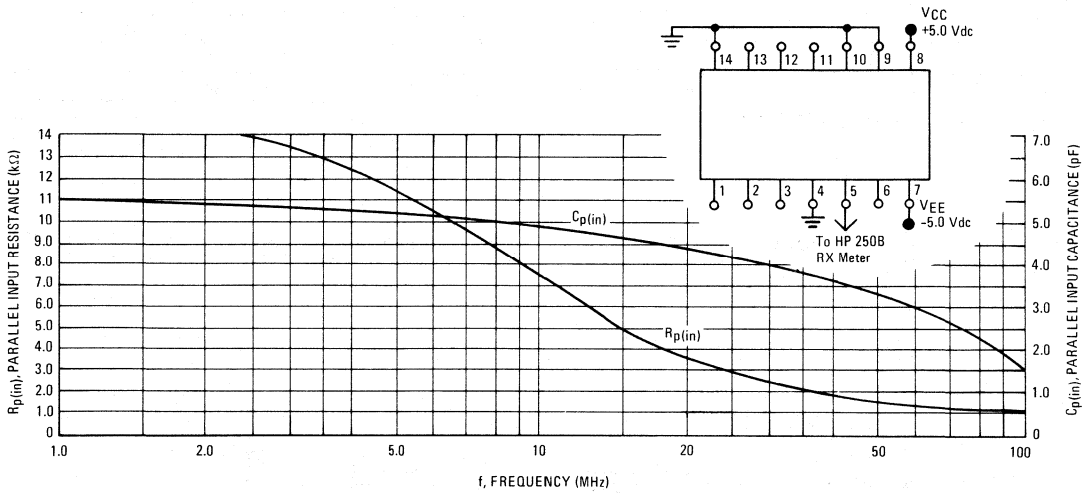


FIGURE 10 – PARALLEL INPUT IMPEDANCE versus FREQUENCY



7

APPLICATIONS INFORMATION

Line Driver/Receiver Family Characteristics

The Motorola line driver/receiver series provides interface circuits for driving digital data transmission lines, e.g., coaxial cable or twisted pair. The digital data transmission is via a balanced differential mode. The line drivers and receivers are designed to provide high common-mode noise rejection, present high impedances to the transmission line and have low propagation times. A feature of the drivers is the capability to operate in a party-line mode whereby a number of drivers can be connected to a single line. This series provides drivers and receivers compatible with MRTL, MDTL, MTTL and MECL. The five circuits of the family are:

- MC1580L Dual Line Driver/Receiver
- MC1581L Dual MECL Receiver
- MC1582L Dual MDTL/MTTL Driver
- MC1583L Dual Receiver (Open Collector)
- MC1584L Dual Receiver (Active Pullup)

Figure 11 indicates the line drivers and receivers recommended for interfacing with each of the various digital logic families.

These five circuits are extremely useful in numerous applications other than line drivers and receivers. The differential amplifier input of the receiver makes it useful in applications such as voltage

FIGURE 11

| Digital Logic Family | Driver | Receiver |
|----------------------|--------------------|--------------------|
| MECL | MC1580L | MC1581L |
| MDTL | MC1582L | MC1583L MC1584L |
| MTTL | MC1582L | MC1583L MC1584L |
| MRTL | MC1580L MC1582L | MC1583L |

comparators, waveform generators and high-input-impedance buffers. The drivers and receivers are useful as logic level translators.

The MC1584L in Figure 12 serves as the line receiver in a balanced differential transmission line. The outputs of the receiver and the inputs to the driver are compatible with MTTL and MDTL circuits. The MC1584L contains an active pullup circuit in the output stage. The MC1583L receiver can also be used for MTTL or MDTL systems. The open collector outputs of the MC1583L require external pullup resistors but is designed to sink up to 20 mA.

While common-mode noise is the major concern in a twisted pair transmission line; a good data transmission system must offer some immunity from differential-mode voltages that may be present due to mismatches in termination impedances. The drivers and receivers of the MC1580 Series are designed with this requirement in mind. The exact amount of noise immunity depends on line impedances but the following example shows how differential-mode noise immunity is calculated for a given system. For a line with a characteristic impedance of Z_0 , calculate the minimum differential input voltage from the equation.

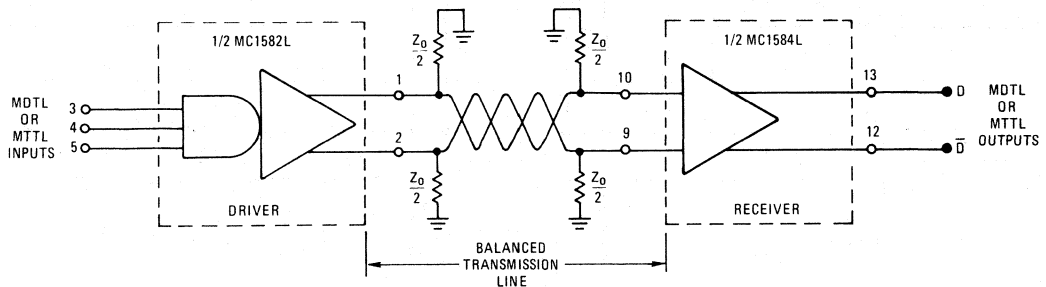
$$\pm V_{in} = \frac{I_o(\min) \times Z_0}{4}$$

For a 170-ohm line, $V_{in} = \frac{(6.9)(170)}{4} = 0.29$ Volts.

Since the MC1584L requires a 50 mV maximum input differential to maintain the output state, the worst case differential-mode noise immunity is 0.26 V. (See Figure 13).

High input impedance of the MC1584L and high output impedance of the MC1582L minimize impedance discontinuities on the transmission line and allow many drivers and receivers to be connected to the line.

FIGURE 12 – MDTL, MTTL COMPATIBLE TRANSMISSION SYSTEM



APPLICATIONS INFORMATION (continued)

Use of the MC1584L in a bi-directional MDTL or MTTL compatible transmission system is shown in Figure 14. The drivers of Figure 14 are connected so that the current sources from both drivers pull current from the same wire of the twisted pair when both drivers are transmitting logic "0" signals. The external current source, I_S , supplies the current required by one driver. The current for the other driver is drawn from the termination impedances creating a voltage differential across the line. When either driver transmits a logic "1", a voltage difference of the opposite polarity is created across the line. For a system with two drivers the current source (I_S) can be supplied by a 600-ohm resistor connected to +5.0 Volts. If additional drivers are connected to the line, a matching current source must be connected for each added driver. The current sources are connected to the line so that when all drivers

are transmitting logic "0's, the difference in current drawn from the terminating resistors of the two wires in the twisted pair is equal to one current source (8.6 mA). The current sources should also be connected so that when any driver transmits a logic "1" a current difference of the opposite polarity exists. The matching current source should be the companion circuit on the various driver chips. The difference in amplitude of the two current sources on a single chip is specified to allow the system designer to calculate the maximum current source mismatch, ΔI_{OL} , and hence the maximum number of drivers that can be connected to a given transmission line. The MC1584L has many other uses in a digital system. The high input impedance suggests its use as a buffer for delay lines and in waveform generation circuits.

FIGURE 13

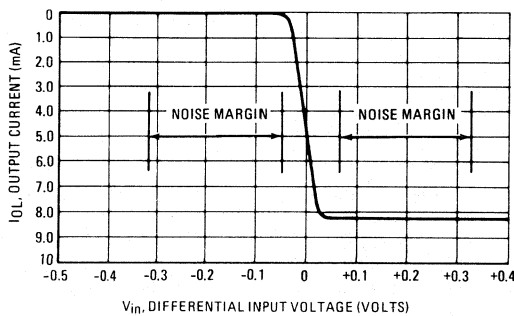


FIGURE 14 – BI-DIRECTIONAL TRANSMISSION SYSTEM

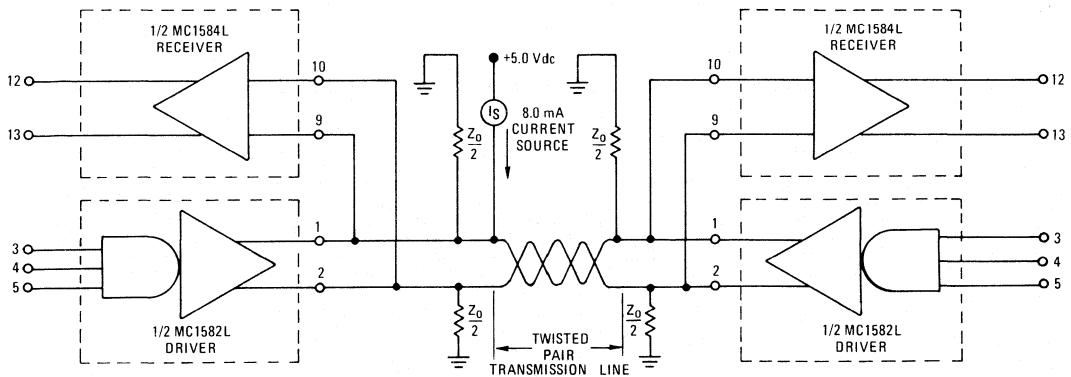
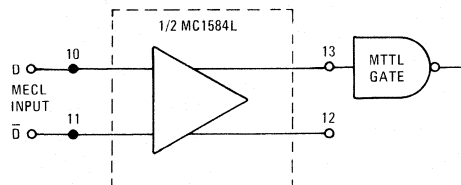


FIGURE 15 – MECL-TO-MTTL LEVEL TRANSLATOR



Voltage Translator

Translation of voltage levels from MECL (often used for the high-speed portion of a digital system) to MTTL (used in other slower portions of the system) is often required. The MC1584L can perform this function as indicated in Figure 15. The complements of the MECL input must be present unless a MECL bias source is available.

7

MC1585L

DUAL CLOCK DRIVER

Advance Information

DUAL MOS CLOCK DRIVER

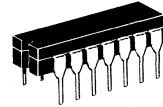
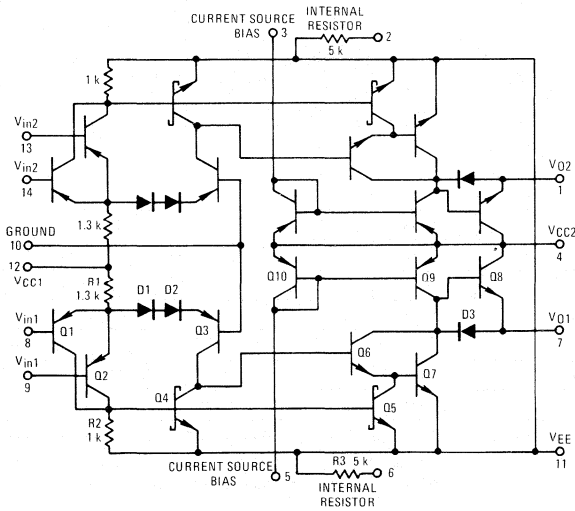
... designed for high-speed driving of highly capacitive loads in a MOS system.

- High Output Current (± 400 mA peak)
- MDTL, MTTL Compatible Input
- Output Compatible with High and Low Threshold P-Channel MOS Devices
- High-Speed (2.0 MHz Pulse Repetition Rate at $C_L = 1000$ pF)

DUAL MOS CLOCK DRIVER

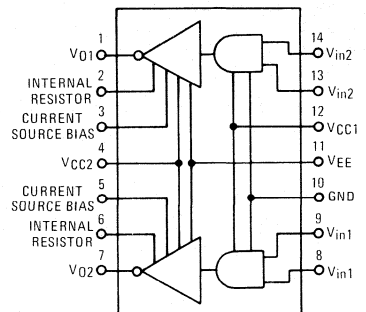
MONOLITHIC SILICON
INTEGRATED CIRCUIT

FIGURE 1 - CIRCUIT SCHEMATIC

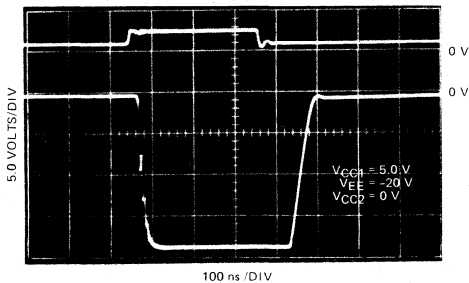


CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 2



TYPICAL OPERATION



See Packaging Information Section for outline dimensions.

MC1585L (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|-----------------|-------------|----------------------------|
| Voltage Supply Range 1 (See Figure 3) | V_{R1} | 10 | Vdc |
| Voltage Supply Range 2 (See Figure 3) | V_{R2} | 30 | Vdc |
| Voltage Supply Range 3 (See Figure 3) | V_{R3} | 22 | Vdc |
| Input Voltage | $V_{in(max)}$ | 10 | Vdc |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| Power Dissipation | P_D | 1000 | mW |
| Ceramic Package | $1/\theta_{JA}$ | 6.7 | $\text{mW}/^\circ\text{C}$ |
| Derate above $T_A = +25^\circ\text{C}$ | | | |

FIGURE 3 – SUPPLY VOLTAGE RANGE DEFINITION

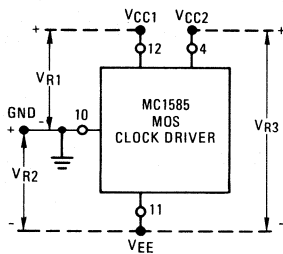
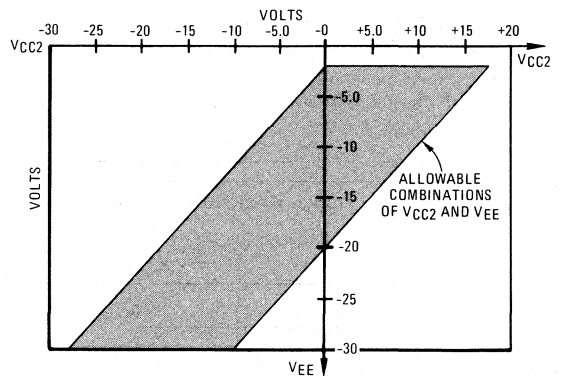


FIGURE 4 – ALLOWABLE VALUES FOR V_{CC2} AND V_{EE}



SWITCHING CHARACTERISTICS ($C_L = 1000 \text{ pF}$)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---------------|-----|-----|-----|------|
| Propagation Delay Time before Rise Time | t_{TLH} | — | 55 | 75 | ns |
| Rise Time | t_r | — | 50 | 75 | ns |
| Propagation Delay Time before Fall Time | t_{THL} | — | 25 | 50 | ns |
| Fall Time | t_f | — | 22 | 50 | ns |
| Pulse Repetition Rate | PRR | 0 | — | 2.0 | MHz |
| Peak Output Current | $I_{O(peak)}$ | — | 400 | 500 | mA |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

The above characteristics were measured with $V_{CC1} = 5.0$ volts, $V_{EE} = -20$ volts, $V_{CC2} = 0$ volts, $C_L = 1000 \text{ pF}$ (with a 10-ohm series resistor). The minimum values and maximum values apply from -55°C to $+125^\circ\text{C}$. Typical values are for $T_A = 25^\circ\text{C}$. The transition times are measured as shown in Figure 5 and 6.

FIGURE 5 – SWITCHING TIME WAVEFORM

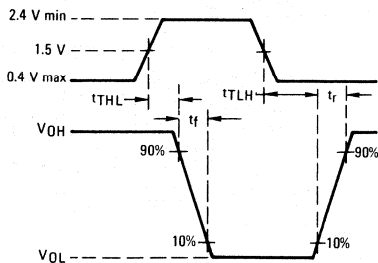
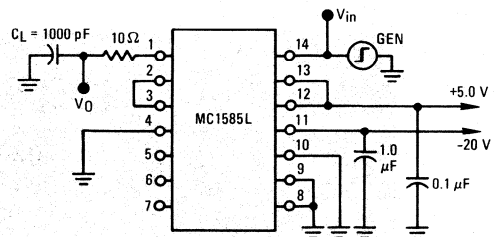


FIGURE 6 – AC TEST CIRCUIT



MC1585L (continued)

ELECTRICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$ unless otherwise noted)
 (Pin 2 is shorted to pin 3 and pin 5 is shorted to pin 6.)

| Characteristic | Symbol | Pin Under Test | TEST CURRENT AND VOLTAGE VALUES | | | | | | | | | | | GND | |
|--------------------------------------|------------|----------------|---------------------------------|--|----------------|---------------|-----------------|------------|------------|-----------|-----------|----|----|-----|----|
| | | | Load Currents | | Input Voltages | | Supply Voltages | | | | | | | | |
| | | | Symbol | I_{OH} | I_{OL} | V_{IL} | V_{IH} | V_{CC1L} | V_{CC1H} | V_{EE} | V_{CC2} | | | | |
| | | | Unit | mA | | Volts | | | | | | | | | |
| | | | Value | -1.0 | +1.0 | 1.1 | 1.78 | 4.5 | 5.5 | -15 | +5.0 | | | | |
| | | | Test Limits | TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: | | | | | | | | | | | |
| | | | Min | Typ | Max | Unit | | | | | | | | | |
| Input Currents: Forward | I_{IL} | 8 | - | - | -1.6 | mA | - | - | 8 | 9 | - | 12 | 11 | 4 | 10 |
| Reverse Leakage | I_{IH} | 8 | - | - | +50 | μA | - | - | - | 8.9 | - | 12 | 11 | 4 | 10 |
| Output Voltage: High Output | V_{OH} | 7 | +3.7 | - | - | Volts | 7 | - | 8 | 9 | 12 | - | 11 | 4 | 10 |
| Low Output | V_{OL} | 7 | - | - | -13.4 | Volts | - | 7 | - | 8.9 | - | 12 | 11 | 4 | 10 |
| Supply Current V_{CC1} High Output | I_{CC1H} | 12 | - | - | 10 | mA | - | - | 8.13 | 9.14 | - | 12 | 11 | 4 | 10 |
| V_{CC1} Low Output | I_{CC1L} | 12 | - | - | 7.0 | mA | - | - | - | 8.9,13,14 | - | 12 | 11 | 4 | 10 |
| V_{EE} High Output | I_{EEH} | 11 | - | - | 25 | mA | - | - | 8.13 | 9.14 | - | 12 | 11 | 4 | 10 |
| V_{EE} Low Output | I_{EEL} | 11 | - | - | 64 | mA | - | - | - | 8.9,13,14 | - | 12 | 11 | 4 | 10 |
| V_{CC2} High Output | I_{CC2H} | 4 | - | - | 15 | mA | - | - | 8.13 | 9.14 | - | 12 | 11 | 4 | 10 |
| V_{CC2} Low Output | I_{CC2L} | 4 | - | - | 57 | mA | - | - | - | 8.9,13,14 | - | 12 | 11 | 4 | 10 |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

TYPICAL CHARACTERISTICS

FIGURE 7 – PACKAGE LIMITATION ON POWER DISSIPATION

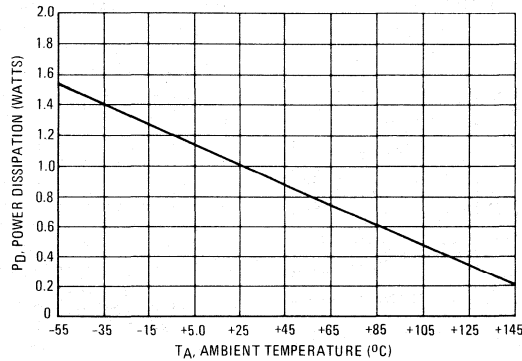


FIGURE 8 – MAXIMUM DIFFERENTIAL LEVEL SHIFT POWER DISSIPATION (WITH BOTH INPUTS HIGH)

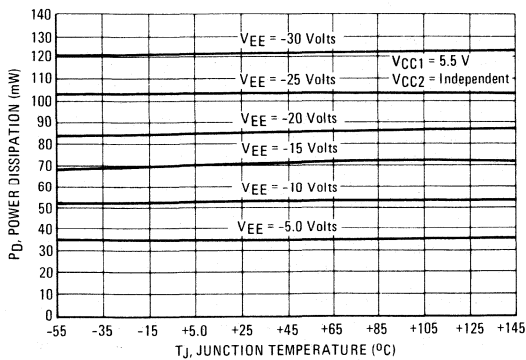
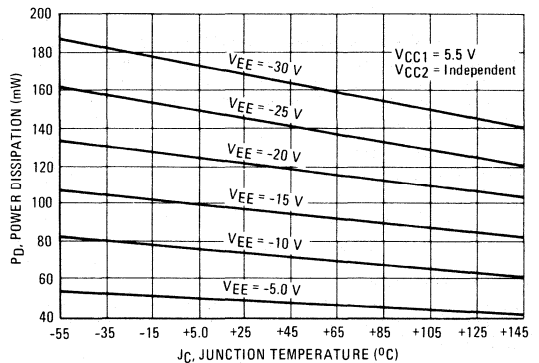


FIGURE 9 – MAXIMUM DIFFERENTIAL LEVEL SHIFT POWER DISSIPATION (At least one input low)



TYPICAL CHARACTERISTICS (cont.)

FIGURE 10 – MAXIMUM BIAS CURRENT versus VOLTAGE AND TEMPERATURE WHEN USING INTERNAL BIAS RESISTOR

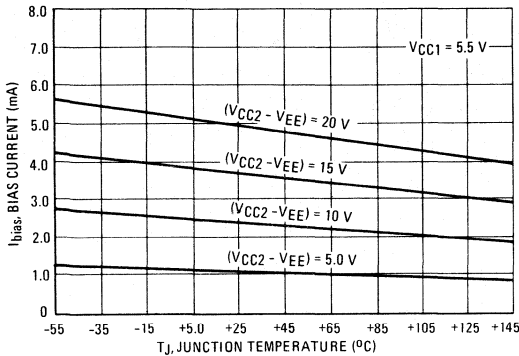


FIGURE 11 – MAXIMUM POWER DISSIPATION OF INTERNAL RESISTOR (R3)

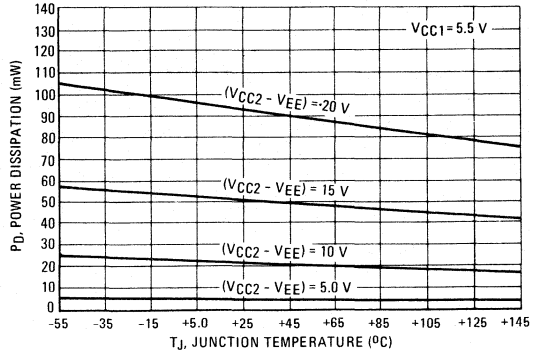


FIGURE 12 – MAXIMUM BIAS POWER DISSIPATION IN Q9, Q10 (INDEPENDENT OF OUTPUT STATE)

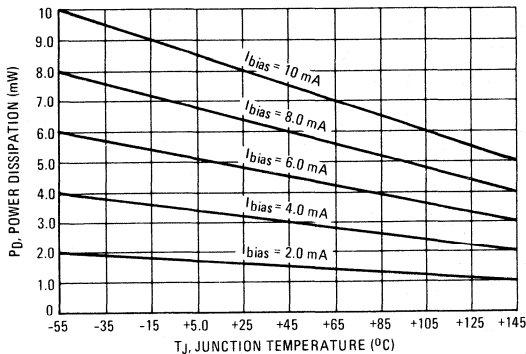
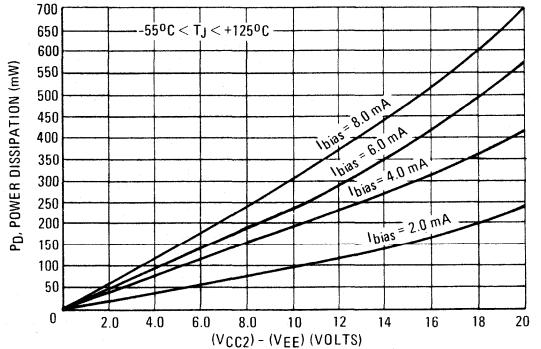


FIGURE 13 – POWER DISSIPATION OF OUTPUT CURRENT OF ACTIVE PULLUP versus BIAS CURRENT versus VOLTAGE



APPLICATIONS INFORMATION

The total power dissipation in the MOS clock driver is the sum of a dc and an ac component. The total of these components must not exceed the package power dissipation limit at the maximum temperature of operation. The package limitation on power dissipation is shown in Figure 7.

AC Power Dissipation

The ac component of power dissipation is given in equation 1.

$$P_{ac} = C_L \cdot [(V_{CC2}) - (V_{EE})]^2 \cdot (PRR) \quad (1)$$

where C_L is the load capacitance and PRR is the pulse repetition rate.

DC Power Dissipation

For ease of calculation, the dc power dissipation is divided into two parts: 1) differential level shift power 2) output pullup current source power.

Differential Level Shift Power

In Figure 1 it may be seen that the differential level shift consists of the input PNP transistors, Q1, Q2, Q3, and bias resistor, R1. The values of maximum level shift power versus junction temperature are given in Figures 8 and 9 for several values of V_{EE} and both input conditions. If the duty cycle is defined as in equation 2, the total level shift power is given in equation 3.

$$\text{Duty Cycle} = \frac{\text{Time Both Inputs are High}}{\text{Total Time}} \quad (2)$$

$$\text{Level Shift Power} = (\text{Value from Figure 8}) \cdot (1 - \text{Duty Cycle}) + (\text{Value from Figure 9}) \cdot (1 - \text{Duty Cycle}) \quad (3)$$

Output Pullup Current Source

The output pullup current source consists of transistors Q9, Q10 and resistor R3. The power dissipated in the output pullup current

APPLICATIONS INFORMATION (continued)

source depends upon temperature, supply voltages, bias current drawn from the collector-base short of transistor Q10 and output logic level. Neglecting the emitter-base drop of transistor Q10 the value of bias current is determined from equation 4.

$$I_{IB} = \frac{V_{CC2} - V_{EE}}{R_3} \quad (4)$$

If the internal bias resistor is used the maximum value of bias current versus temperature is as shown in Figure 10. The maximum power dissipated in the internal bias resistor and the maximum power dissipated in Q9 and Q10 (due to bias current) are independent of output logic level and are shown in Figures 11 and 12. The maximum power dissipation due to collector current in Q9 is approximately zero when the output is high but when the output is low the power dissipation is as shown in Figure 13. The total output pullup current-source power dissipation is thus defined by equation 5.

$$P(\text{max}) \text{ current source} = (\text{Value from Figure 11}) + (\text{Value from Figure 12}) + (\text{Value from Figure 13}) \times (\text{Duty Cycle}) \quad (5)$$

Example Calculation

Suppose it is desired to use the MOS clock driver in an application which requires the following:

$V_{CC1} = +5.0 \text{ volts}$
 $V_{EE} = -15 \text{ volts}$
 $V_{CC2} = +5.0 \text{ volts}$
 $PRR = 1.0 \text{ MHz}$
 Duty Cycle = 0.1%

Load capacitance, 500 pF @ $T_A(\text{max}) +70^\circ\text{C}$

A calculation of dc and ac power is necessary to find whether or not package limitations will be exceeded. Since each power dissipation figure either decreases or remains constant with temperature, it is assumed that $T_J \geq +25^\circ\text{C}$ and points at $+25^\circ\text{C}$ will be used in this calculation. The total differential level-shift power may be found from Figures 8 and 9 and equation 3 to be:

$$\text{Level-Shift Power} = 92.5 \text{ mW}$$

If the internal bias resistor is used, Figure 10 shows the value of the bias current to be 4.9 mA, and the power dissipation of the internal bias resistor is found from Figure 11 to be 90 mW.

The power dissipation in Q9 and Q10 due to bias current is found from Figure 12 to be 4.0 mW.

The power dissipation in Q9 when the output is low is found from Figure 13 to be 490 mW.

The total power dissipated in the output pullup current source can now be found from equation 5 to be:

$$\text{Power (current source)} = 143 \text{ mW}$$

The total dc dissipation, the sum of differential level-shift dissipation and output pullup current-source dissipation, is 235.5 mW.

The ac dissipation may be found from equation 1 to be 200 mW.

The total power dissipation for one clock driver is thus 435.5 mW. If both clock drivers are used in an identical fashion the total package dissipation is 871 mW. Referring to Figure 7 it is seen that safe operation to approximately $+45^\circ\text{C}$ is possible. If external resistors are used for R3 to produce the same bias current as above, a net total savings in power dissipation of 180 mW can be made reducing the total package dissipation to 691 mW and permitting safe operation at $+70^\circ\text{C}$.

MC1590G

MONOLITHIC RF/IF/AUDIO AMPLIFIER

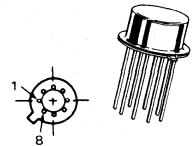
... an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, -55 to +125°C. See Motorola Application Note AN-513 for design details.

- High Power Gain – 50 dB typ at 10 MHz
45 dB typ at 60 MHz
35 dB typ at 100 MHz
- Wide-Range AGC – 60 dB min, dc to 60 MHz
- Low Reverse Transfer Admittance – $< 10 \mu\text{mhos}$ typ at 60 MHz
- 6.0 to 15-Volt Operation, Single-Polarity Power Supply

WIDEBAND AMPLIFIER WITH AGC

SILICON
EPITAXIAL PASSIVATED

METAL PACKAGE
CASE 601
TO-99



(bottom view)

FIGURE 1 – UNNEUTRALIZED POWER GAIN versus FREQUENCY
(Tuned Amplifier, see Figure 16)

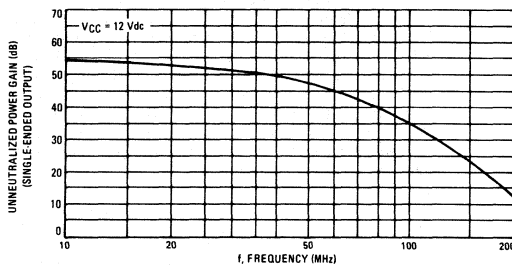
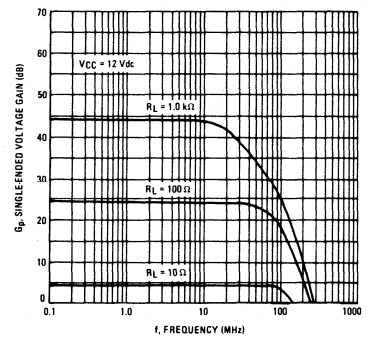
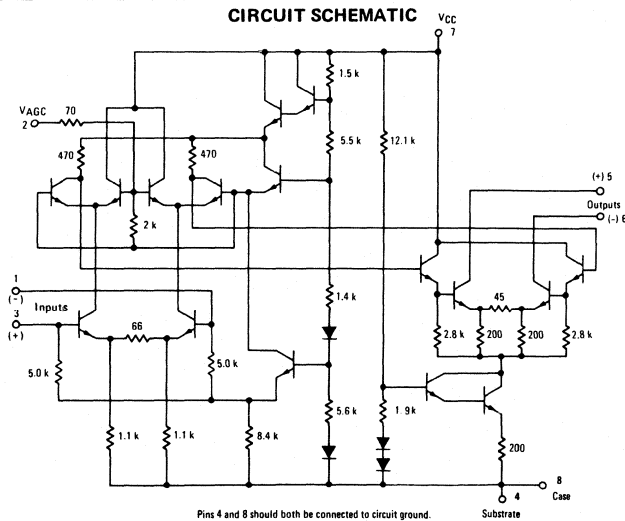


FIGURE 2 – VOLTAGE GAIN versus FREQUENCY
(Video Amplifier, see Figure 17)

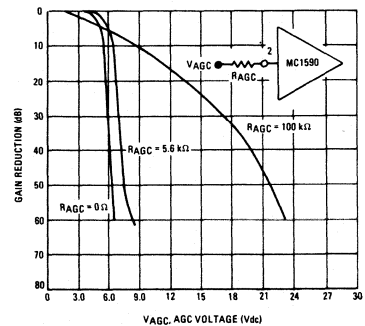


CIRCUIT SCHEMATIC



Pins 4 and 8 should both be connected to circuit ground.

FIGURE 3 – TYPICAL GAIN REDUCTION
versus AGC VOLTAGE



See Packaging Information Section for outline dimensions.

See MCBC1590/MCB1590F for beam-lead device information.

MC1590G (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol* | Value | Unit |
|--|------------|-------------|----------------------------|
| Power Supply Voltage | V_{CC} | +18 | Vdc |
| Output Supply | V_5, V_6 | +18 | Vdc |
| AGC Supply | V_{AGC} | V_{CC} | Vdc |
| Differential Input Voltage | V_{in} | 5.0 | Vdc |
| Power Dissipation (Package Limitation) Derate above $T_A = +25^\circ\text{C}$ | P_D | 680 4.6 | mW mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS ($V_{CC} = +12\text{ Vdc}$, $f = 60\text{ MHz}$, $BW = 1.0\text{ MHz}$, $T_A = +25^\circ\text{C}$ unless otherwise noted, see Figure 16 for test circuit.)

| Characteristic | Symbol* | Min | Typ | Max | Unit |
|---|-------------|-----|-----|-----|-----------|
| AGC Range, $V_2 = 5.0\text{ Vdc}$ to 7.0 Vdc | | 60 | 68 | — | dB |
| Single-Ended Power Gain | G_p | 40 | 45 | — | dB |
| Noise Figure ($R_s = 50\text{ ohms}$) | NF | — | 6.0 | — | dB |
| Output Voltage Swing (Pin 5) | V_5 | | | | V_{p-p} |
| Differential Output — 0 dB AGC | | — | 14 | — | |
| —30 dB AGC | | — | 6.0 | — | |
| Single-Ended Output — 0 dB AGC | | — | 7.0 | — | |
| —30 dB AGC | | — | 3.0 | — | |
| Output Stage Current (Pins 5 and 6) | $I_5 + I_6$ | — | 5.6 | — | mA |
| Total Supply Power Current ($V_O = 0$) | I_D | — | 14 | 17 | mAdc |
| Power Dissipation ($V_{in} = 0$) | P_D | — | 168 | 200 | mW |

*Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

ADMITTANCE PARAMETERS ($V_{CC} = +12\text{ Vdc}$, $T_A = +25^\circ\text{C}$)

| Parameter | Symbol | Typ | | Unit |
|--|-----------------------------|---------------------|---------------------|------------------|
| | | $f = 30\text{ MHz}$ | $f = 60\text{ MHz}$ | |
| Single-Ended Input Admittance | a_{11} b_{11} | 0.4 1.2 | 0.75 3.4 | mmhos |
| Single-Ended Output Admittance | a_{22} b_{22} | 0.05 0.50 | 0.1 1.0 | mmho |
| Forward Transfer Admittance (Pin 1 to Pin 5) | $ Y_{21} $ θ_{21} | 150 -45 | 150 -105 | mmhos degrees |
| Reverse Transfer Admittance* | a_{12} b_{12} | -0 -5.0 | -0 -10 | μmhos |

*The value of Reverse Transfer Admittance includes the feedback admittance of the test circuit used in the measurement. The total feedback capacitance (including test circuit) is 0.025 pF and is a more practical value for design calculations than the internal feedback of the device alone. (See Figure 6)

SCATTERING PARAMETERS ($V_{CC} = +12\text{ Vdc}$, $T_A = +25^\circ\text{C}$, $Z_0 = 50\ \Omega$)

| Parameter | Symbol | Typ | | Unit |
|----------------------------------|-----------------------------|---------------------|---------------------|--------------|
| | | $f = 30\text{ MHz}$ | $f = 60\text{ MHz}$ | |
| Input Reflection Coefficient | $ S_{11} $ θ_{11} | 0.95 -7.3 | 0.93 -16 | — degrees |
| Output Reflection Coefficient | $ S_{22} $ θ_{22} | 0.99 -3.0 | 0.98 -5.5 | — degrees |
| Forward Transmission Coefficient | $ S_{21} $ θ_{21} | 16.8 128 | 14.7 64.3 | — degrees |
| Reverse Transmission Coefficient | S_{12} θ_{12} | 0.00048 84.9 | 0.00092 79.2 | — degrees |

TYPICAL CHARACTERISTICS
 ($V_{CC} = 12 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 4 – FIXED TUNED POWER GAIN versus TEMPERATURE (See test circuit, Figure 16)

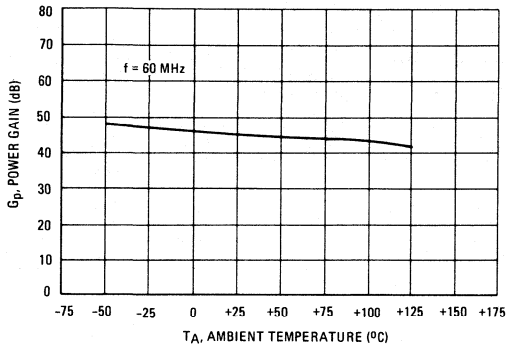


FIGURE 5 – POWER GAIN versus SUPPLY VOLTAGE (See test circuit, Figure 16)

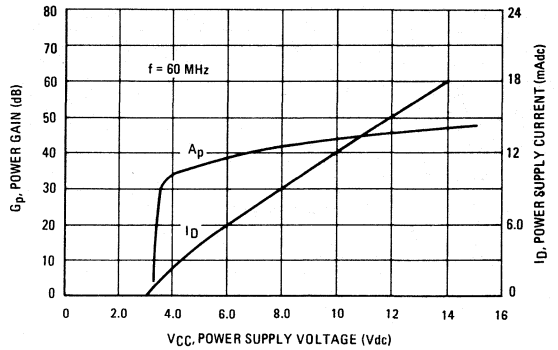


FIGURE 6 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY (See Parameter Table, page 2 of MC1590 specification)

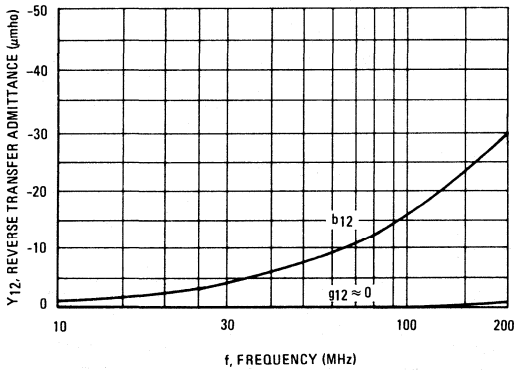


FIGURE 7 – NOISE FIGURE versus FREQUENCY

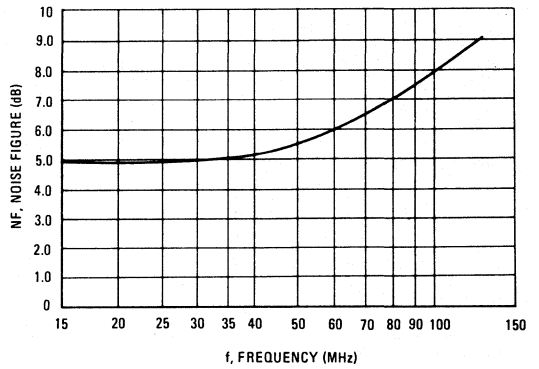


FIGURE 8 – SINGLE-ENDED OUTPUT ADMITTANCE

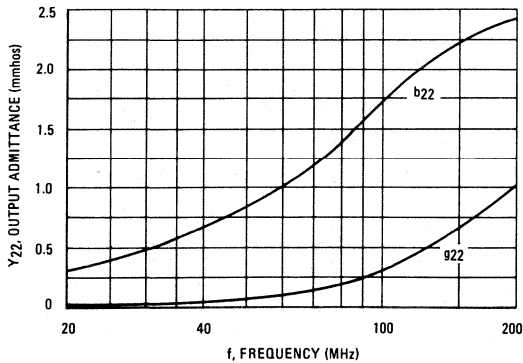
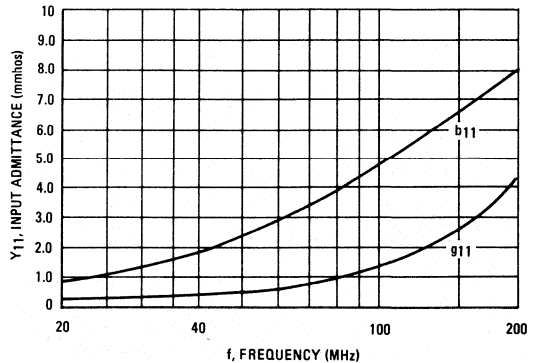


FIGURE 9 – SINGLE-ENDED INPUT ADMITTANCE



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – Y_{21} , FORWARD TRANSFER ADMITTANCE, RECTANGULAR FORM

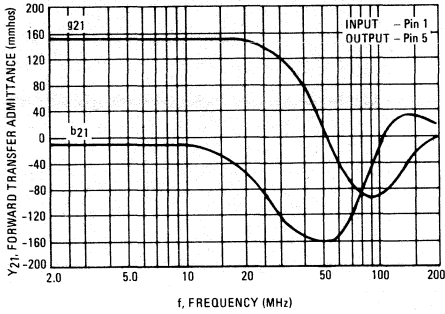


FIGURE 11 – Y_{21} , FORWARD TRANSFER ADMITTANCE, POLAR FORM

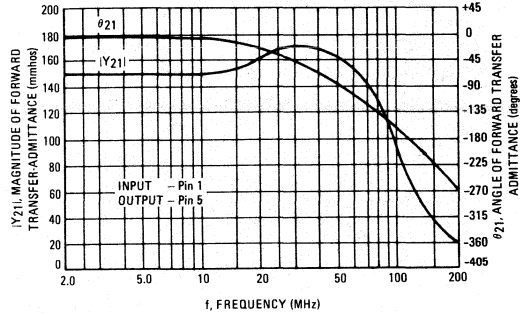


FIGURE 12 – S_{11} and S_{22} , INPUT AND OUTPUT REFLECTION COEFFICIENT

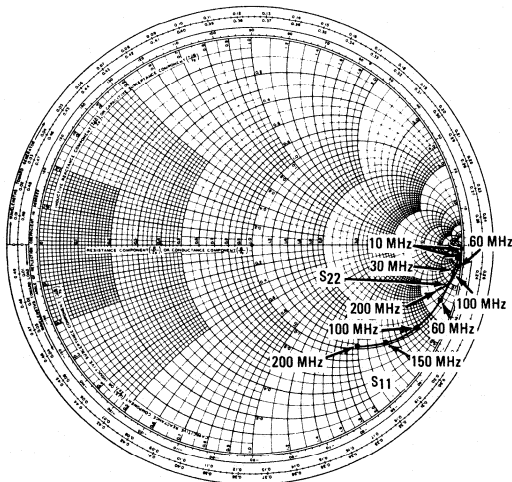
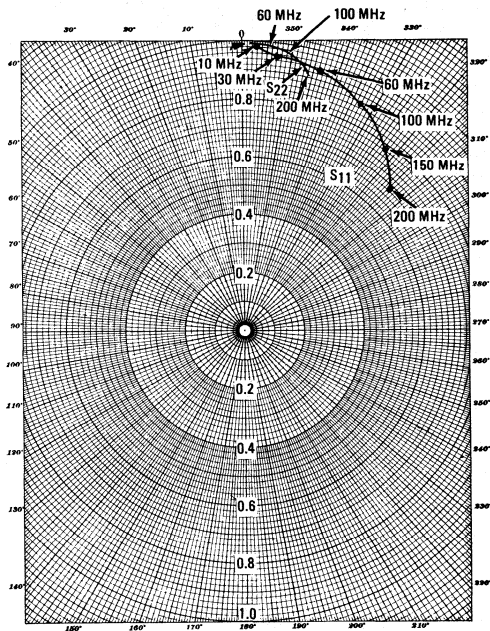


FIGURE 13 – S_{11} , and S_{22} , INPUT AND OUTPUT REFLECTION COEFFICIENT



TYPICAL CHARACTERISTICS (continued)

FIGURE 14 – S_{21} , FORWARD TRANSMISSION COEFFICIENT (GAIN)

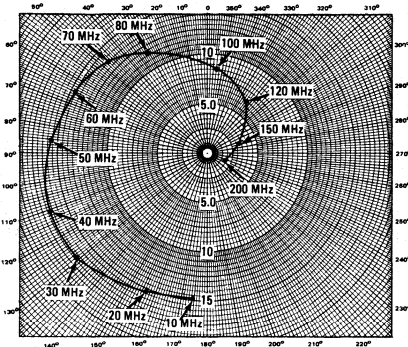
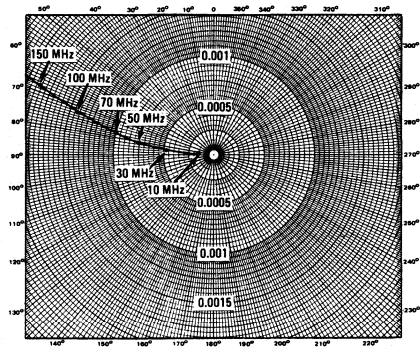
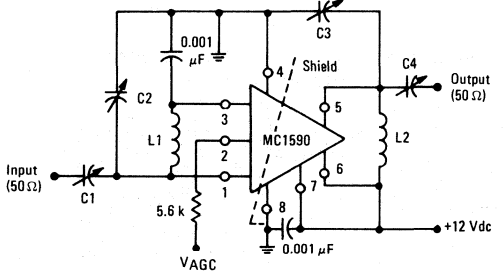


FIGURE 15 – S_{12} , REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



TYPICAL APPLICATIONS

FIGURE 16 – 60-MHz POWER GAIN TEST CIRCUIT



L1 = 7 Turns, #20 AWG Wire, 5/16" Dia., 5/8" Long
 L2 = 6 Turns, #14 AWG Wire, 9/16" Dia., 3/4" Long
 C1, C2, C3 = (1-30) pF
 C4 = (1-10) pF

FIGURE 17 – VIDEO AMPLIFIER

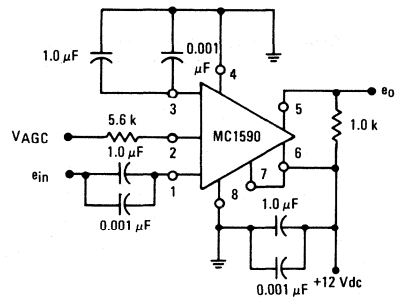
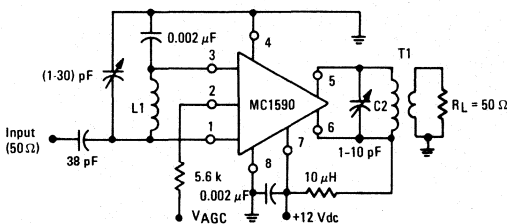
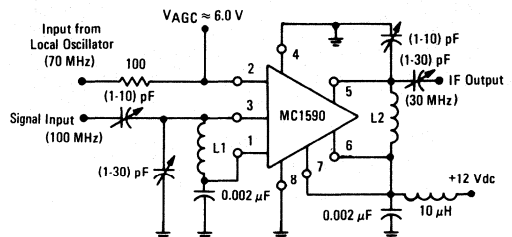


FIGURE 18 – 30-MHz AMPLIFIER
 (Power Gain = 50 dB, BW ≈ 1.0 MHz)



L1 = 12 Turns #22 AWG Wire on a Toroid Core, (T37-6 Micro Metal or Equiv)
 T1: Primary = 17 Turns #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)
 Secondary = 2 Turns #20 AWG Wire

FIGURE 19 – 100-MHz MIXER



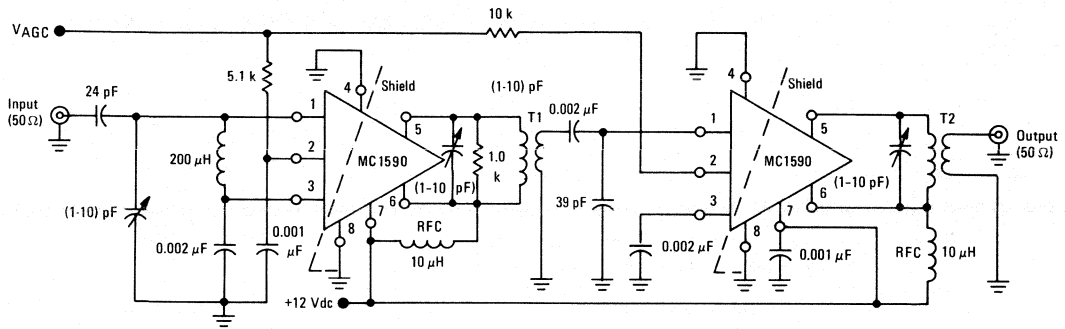
L1 = 5 Turns, #16 AWG Wire, 1/4" ID, 5/8" Long
 L2 = 16 Turns, #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)

7

MC1590G (continued)

TYPICAL APPLICATIONS (continued)

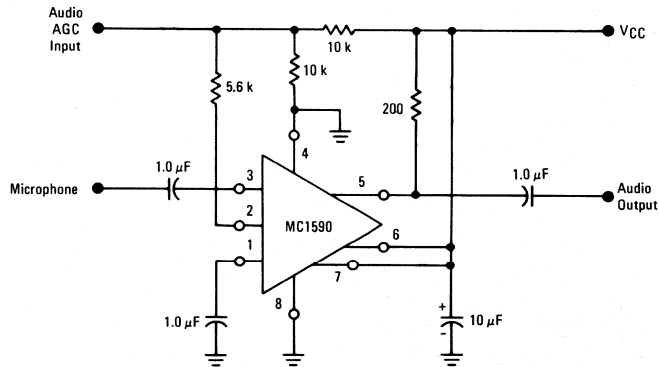
FIGURE 20 – TWO-STAGE 60 MHz IF AMPLIFIER (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)



T1: Primary Winding = 15 Turns, #22 AWG Wire, 1/4" ID Air Core
 Secondary Winding = 4 Turns, #22 AWG Wire,
 Coefficient of Coupling ≈ 1.0

T2: Primary Winding = 10 Turns, #22 AWG Wire, 1/4" ID Air Core
 Secondary Winding = 2 Turns, #22 AWG Wire,
 Coefficient of Coupling ≈ 1.0

FIGURE 21 – SPEECH COMPRESSOR



MC1594L MC1494L

Specifications and Applications Information

MONOLITHIC FOUR-QUADRANT MULTIPLIER

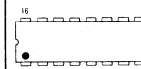
... designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

- Operates With ± 15 V Supplies
- Excellent Linearity – Maximum Error (X or Y): $\pm 0.5\%$ (MC1594)
 $\pm 1.0\%$ (MC1494)
- Wide Input Voltage Range – ± 10 volts
- Adjustable Scale Factor, K (0.1 nominal)
- Single-Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small-Signal) – 1.0 MHz
- Power Supply Sensitivity – 30 mV/V typical

LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED

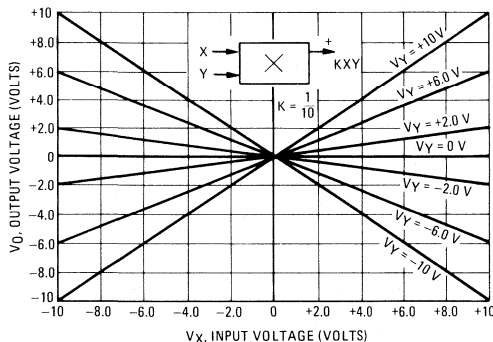


(top view)

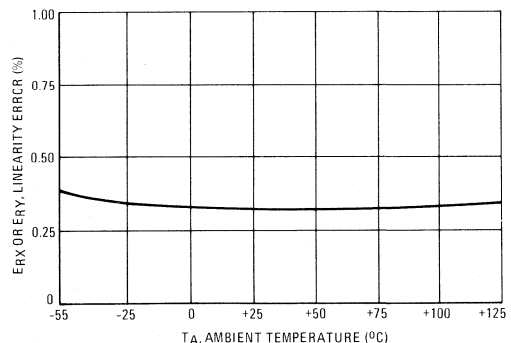


CERAMIC PACKAGE
CASE 620

FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC



TYPICAL LINEARITY ERROR versus TEMPERATURE



CONTENTS

| Subject Sequence | Specification Page No. | Subject Sequence | Specification Page No. |
|----------------------------|------------------------|----------------------------|------------------------|
| Maximum Ratings | 2 | AC Operation | 8 |
| Electrical Characteristics | 2 | DC Applications | 9 |
| Test Circuits | 3 | AC Applications | 11 |
| Characteristic Curves | 4 | Definitions | 13 |
| Circuit Description | 5 | General Information Index | 14 |
| Circuit Schematic | 5 | Package Outline Dimensions | 14 |
| DC Operation | 6 | | |

MC1594L, MC1494L (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|--|--|-------------|
| Power Supply Voltage | V ⁺ V ⁻ | +18 -18 | Vdc |
| Differential Input Signal | V _G -V _G V ₁₀ -V ₁₃ | ± 6 + I ₁ R _Y < 30 ± 6 + I ₁ R _X < 30 | Vdc |
| Common-Mode Input Voltage V _{CMY} = V _G = V _G V _{CMX} = V ₁₀ = V ₁₃ | V _{CMY} V _{CMX} | ±11.5 ±11.5 | Vdc |
| Power Dissipation (Package Limitation) T _A = +25°C Derate above T _A = +25°C | P _D 1/θ _{JA} | 750 5.0 | mW mW/°C |
| Operating Temperature Range MC1594 MC1494 | T _A | -55 to +125 0 to +75 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V⁺ = +15 V, V⁻ = -15 V, T_A = +25°C, R₁ = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, unless otherwise noted)

| Characteristic | Fig. | Symbol | MC1594 | | | MC1494 | | | Unit |
|---|-------|---|------------------------------|---|------------------------------------|------------------------------|---|--|--|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Linearity Output error in Percent of full scale -10 V < V _X < +10 V (V _Y = ±10 V) -10 V < V _Y < +10 V (V _X = ±10 V) T _A = +25°C T _A = T _{high} ① T _A = T _{low} ② | 1 | E _{RX} or E _{RY} | - | ± 0.3 | ± 0.5 | - | ± 0.5 | ± 1.0 | % |
| Input Voltage Range (V _X = V _Y = V _{in}) Resistance (X or Y Input) Offset Voltage (X Input) (Note 1) (Y Input) (Note 1) Bias Current (X or Y Input) Offset Current (X or Y Input) | 2,3,4 | V _{in} R _{in} V _{ioX} V _{ioY} I _b I _{io} | ±10 - - - - - | - 300 0.1 0.4 0.5 28 | - - 1.6 1.6 1.5 150 | ±10 - - - - - | - 300 0.2 0.8 1.0 50 | ± 1.3 - 2.5 2.5 2.5 400 | V _{pk} MΩ V μA nA |
| Output Voltage Swing Capability Impedance Offset Voltage (Note 1) Offset Current (Note 1) | 3,4 | V _o R _o V _{ool} I _{ool} | ±10 - - - | - 850 0.8 17 | - - 1.6 34 | ±10 - - - | - 850 1.2 25 | - - 2.5 52 | V _{pk} kΩ V μA |
| Temperature Stability (Drift) T _A = T _{high} to T _{low} Output Offset (X = 0, Y = 0) Voltage Current X Input Offset (Y = 0) Y Input Offset (X = 0) Scale Factor Total dc Accuracy Drift (X = 10, Y = 10) | | TCV _{oo} TCI _{oo} TCV _{ioX} TCV _{ioY} TCK TCE | - - - - - - | 1.3 27 0.3 1.5 0.07 0.09 | - - - - - - | - - - - - - | 1.3 27 0.3 1.5 0.07 0.09 | - - - - - - | mV/°C nA/°C mV/°C %/°C |
| Dynamic Response Small Signal (3 dB) X Y Power Bandwidth (47 k) 3 ^o Relative Phase Shift 1% Absolute Error | 5 | BW _{3 dB} (X) BW _{3 dB} (Y) P _{BW} φ _p φ _e | - - - - - | 0.8 1.0 440 240 30 | - - - - - | - - - - - | 0.8 1.0 440 240 30 | - - - - - | MHz kHz |
| Common Mode Input Swing (X or Y) Gain (X or Y) | 6 | CMV ACM | ±10.5 - | - -65 | - - | ±10.5 - | - -65 | - - | V _{pk} dB |
| Power Supply Current Quiescent Power Dissipation Sensitivity | 7 | I _d ⁺ I _d ⁻ P _d S ⁺ S ⁻ | - - - - - | 6.0 6.5 185 13 30 | 9.0 9.0 260 50 100 | - - - - - | 6.0 6.5 185 13 30 | 12 12 350 100 200 | mAdc mW mV/V |
| Regulated Offset Adjust Voltages Positive Negative Temperature Coefficient (V _R ⁺ or V _R ⁻) Power Supply Sensitivity (V _R ⁺ or V _R ⁻) | 7 | V _R ⁺ V _R ⁻ TCV _R S _R ⁺ , S _R ⁻ | +3.5 -3.5 - - | +4.3 -4.3 0.03 0.6 | +5.0 -5.0 - - | +3.5 -3.5 - - | +4.3 -4.3 0.03 0.6 | +5.0 -5.0 - - | Vdc mV/°C mV/V |

Note 1: Offsets can be adjusted to zero with external potentiometers.

① T_{high} = +125°C for MC1594
+75°C for MC1494

② T_{low} = -55°C for MC1594
0°C for MC1494

TEST CIRCUITS

FIGURE 1 - LINEARITY

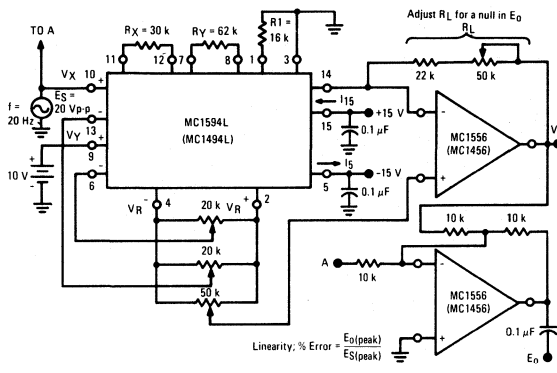


FIGURE 2 - INPUT RESISTANCE

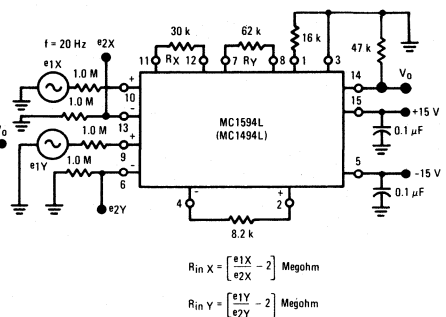


FIGURE 3 - OFFSET VOLTAGES, GAIN

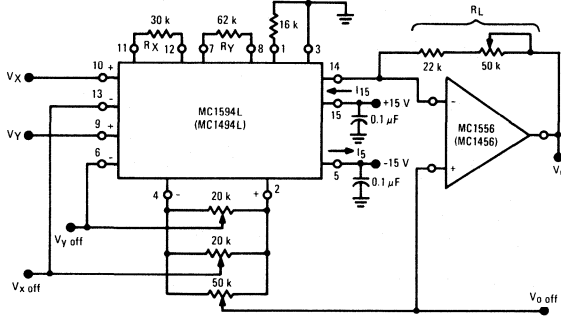


FIGURE 4 - INPUT BIAS CURRENT/INPUT OFFSET CURRENT, OUTPUT RESISTANCE

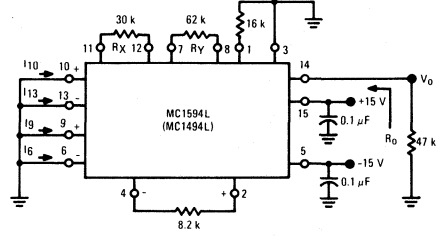


FIGURE 5 - FREQUENCY RESPONSE

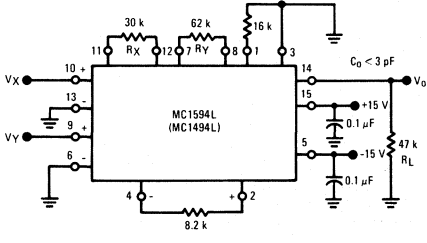


FIGURE 6 - COMMON-MODE

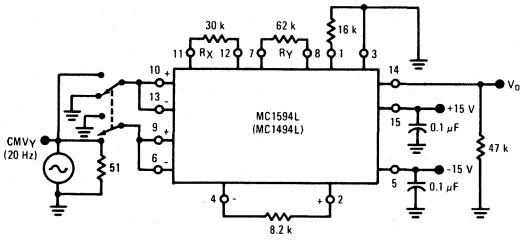


FIGURE 7 - POWER-SUPPLY SENSITIVITY

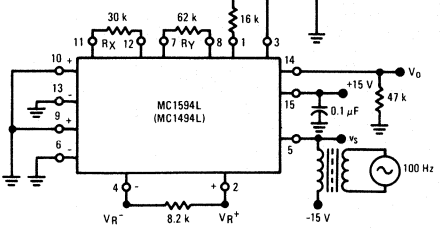
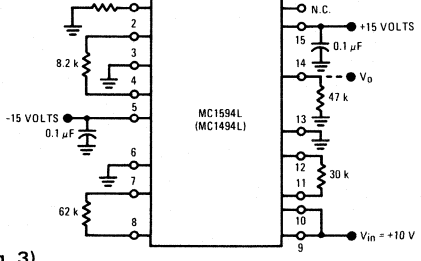


FIGURE 8 - BURN-IN



7

TYPICAL CHARACTERISTICS

(Unless otherwise noted, $V^+ = +15\text{ V}$, $V^- = -15\text{ V}$, $R_1 = 16\text{ k}\Omega$, $R_X = 30\text{ k}\Omega$, $R_Y = 62\text{ k}\Omega$, $R_L = 47\text{ k}\Omega$, $T_A = +25^\circ\text{C}$)

FIGURE 9 – FREQUENCY RESPONSE OF Y INPUT versus LOAD RESISTANCE

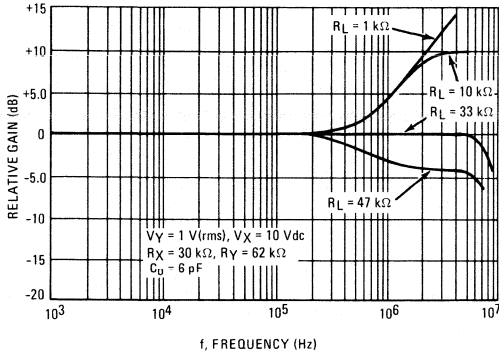


FIGURE 10 – FREQUENCY RESPONSE OF X INPUT versus LOAD RESISTANCE

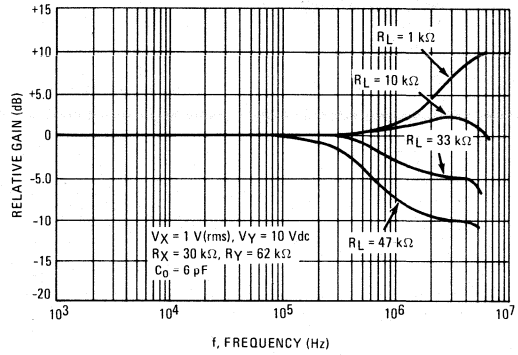


FIGURE 11 – LARGE SIGNAL VOLTAGE versus FREQUENCY

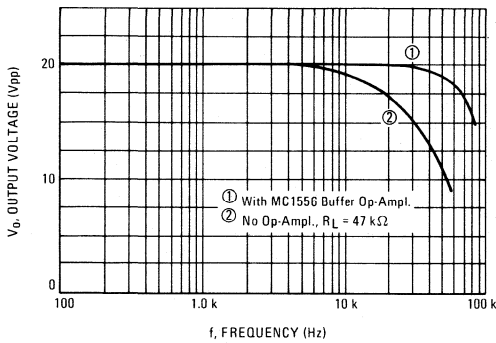


FIGURE 12 – LINEARITY versus R_X OR R_Y WITH $K = 1/10$

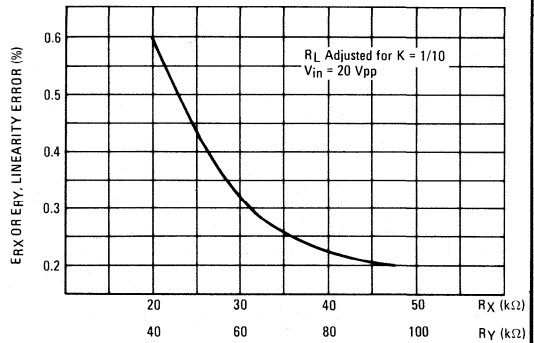


FIGURE 13 – LINEARITY versus R_X OR R_Y WITH $K = 1$

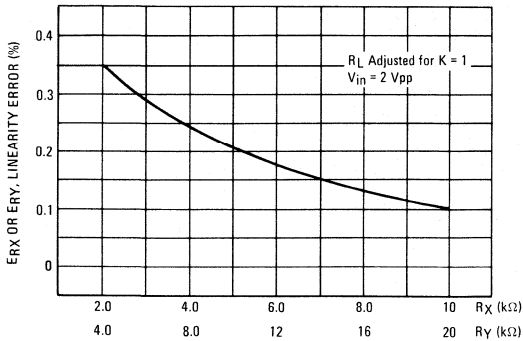
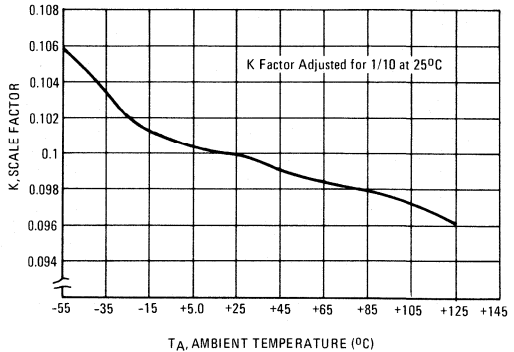


FIGURE 14 – SCALE FACTOR (K) versus TEMPERATURE



GENERAL INFORMATION

1. CIRCUIT DESCRIPTION

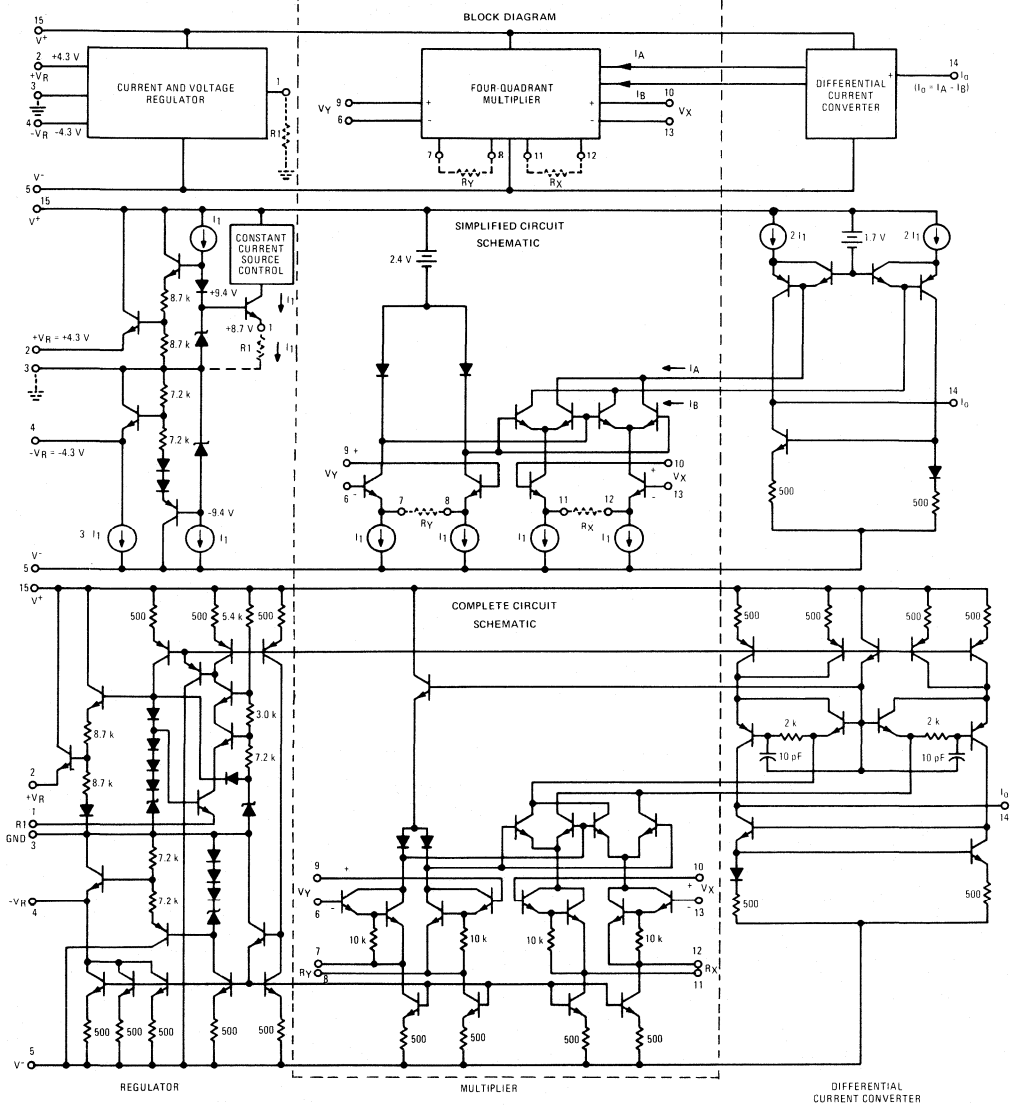
1.1 Introduction

The MC1594 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a single-ended current output referenced to ground and provides two complementary regulated voltages for use

with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltage.

As shown in Figure 15, the MC1594 consists of a multiplier proper and associated peripheral circuitry to provide these features.

FIGURE 15
(Recommended External Circuitry is Depicted With Dotted Lines)



7

1.2 Regulator (Figure 15)

The regulator biases the entire MC1594 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at pin 2 is approximately +4.3 V while the regulated voltage at pin 4 is approximately -4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0$ mA (equivalent load of 8.6 kΩ). As will be shown later, there will normally be two 20 k-ohm potentiometers and one 50 k-ohm potentiometer connected between pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1594. Note that all current sources are related to current I_1 which is determined by R_1 . For best temperature performance, R_1 should be 16 kΩ so that $I_1 \approx 0.5$ mA for all applications.

1.3 Multiplier (Figure 15)

The multiplier section of the MC1594 (center section of Figure 15) is nearly identical to the MC1595 and is discussed in detail in Application Note AN-489, "Analysis and Basic Operation of the MC1595". The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I \approx \frac{2V_X V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages.

1.4 Differential Current Converter (Figure 15)

This portion of the circuitry converts the differential output current ($I_A - I_B$) of the multiplier to a single-ended output current (I_O):

$$I_O = I_A - I_B$$

or

$$I_O = \frac{2V_X V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor R_L from the output (pin 14) to ground (Figure 17) or by using an op-ampl. as a current-to-voltage converter (Figure 16). The result in both circuits is that the output voltage is given by:

$$V_O = \frac{2R_L V_X V_Y}{R_X R_Y I_1} = K V_X V_Y$$

where K (scale factor) = $\frac{2R_L}{R_X R_Y I_1}$

2. DC OPERATION

2.1 Selection of External Components

For low frequency operation the circuit of Figure 16 is recommended. For this circuit, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, $R_1 = 16$ kΩ and hence $I_1 \approx 0.5$ mA. Therefore, to set the scale factor, K, equal to 1/10, the value of R_L can be calculated to be:

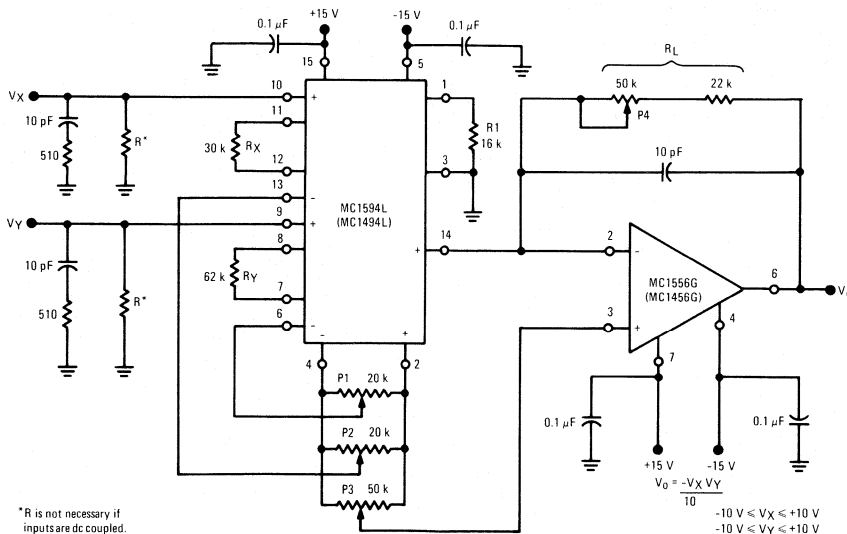
$$K = \frac{1}{10} = \frac{2R_L}{R_X R_Y I_1}$$

or $R_L = \frac{R_X R_Y I_1}{(2)(10)} = \frac{(30 \text{ k})(62 \text{ k})(0.5 \text{ mA})}{20}$

$$R_L = 46.5 \text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making R_L a fixed 47 kΩ resistor. However, if it is desired

FIGURE 16 – TYPICAL MULTIPLIER CONNECTION



*R is not necessary if inputs are dc coupled.

that the scale factor be exact, R_L can be comprised of a fixed resistor and a potentiometer as shown in Figure 16. It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the V_X and V_Y input voltages are expected to be large, say ± 10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set $K = 1/2$ or $K = 1$ or even $K = 100$. This can be accomplished by adjusting R_X , R_Y and R_L appropriately.

The selection of R_L is arbitrary and can be chosen after resistors R_X and R_Y are found. Note in Figure 16 that R_Y is 62 k Ω while R_X is 30 k Ω . The reason for this is that the "Y" side of the multiplier exhibits a second order non-linearity whereas the "X" side exhibits a simple non-linearity. By making the R_Y resistor approximately twice the value of the R_X resistor, the linearity on both the "X" and "Y" sides are made equal. The selection of the R_X and R_Y resistor values is dependent upon the expected amplitude of V_X and V_Y inputs. To maintain a specified linearity, resistors R_X and R_Y should be selected according to the following equations:

$$R_X \geq 3 V_X (\text{max}) \text{ in k}\Omega \text{ when } V_X \text{ is in volts}$$

$$R_Y \geq 6 V_Y (\text{max}) \text{ in k}\Omega \text{ when } V_Y \text{ is in volts}$$

For example, if the maximum input on the "X" side is ± 1 volt, resistor R_X can be selected to be 3 k Ω . If the maximum input on the "Y" side is also ± 1 volt, then resistor R_Y can be selected to be 6 k Ω (6.2 k Ω nominal value). If a scale factor of $K = 10$ is desired, the load resistor is found to be 47 k Ω . In this example, the multiplier provides a gain of 20 dB.

2.2 Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate current-to-voltage converter. The output current of the multiplier flows through the feedback resistor R_L to provide a low impedance output voltage from the op-ampl. Since the offset current and bias currents of the op-ampl. will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1556/MC1456 or MC1741/MC1741C are excellent choices for this application.

Since the MC1594 is capable of operation at much higher frequencies than the op-ampl., the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the op-ampl.

2.3 Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op-ampl.) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with R_L should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op-ampl. might be employed using slightly heavier compensation than that recommended for unity-gain operation.

2.4 Offset Adjustment

The non-inverting input of the op-ampl. provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output

offset voltage can be adjusted to zero (see offset and scale factor adjustment procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).

2.5 Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 16 is:

A. X Input Offset

- connect oscillator (1 kHz, 5 Vpp sine wave) to the "Y" input (pin 9)
- connect "X" input (pin 10) to ground
- adjust X-offset potentiometer, P2 for an ac null at the output

B. Y Input Offset

- connect oscillator (1 kHz, 5 Vpp sine wave) to the "X" input (pin 10)
- connect "Y" input (pin 9) to ground
- adjust Y-offset potentiometer, P1 for an ac null at the output

C. Output Offset

- connect both "X" and "Y" inputs to ground
- adjust output offset potentiometer, P3, until the output voltage V_O , is zero volts dc

D. Scale Factor

- apply +10 Vdc to both the "X" and "Y" inputs
- adjust P4 to achieve -10.00 V at the output
- apply -10 Vdc to both "X" and "Y" inputs and check for $V_O = -10.00$ V

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1594 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinite" resolution type rather than wirewound. Fine adjustments in balanced-modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

2.6 Temperature Stability

While the MC1594 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Previous discussion shows the direct dependence on R_X , R_Y , and R_L and indirect dependence on R1 (through I_1). Any circuit subjected to temperature variations should be evaluated with these effects in mind.

2.7 Bias Currents

The MC1594 multiplier, like most linear IC's, requires a dc bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs V_X and V_Y are able to supply the small bias current ($\approx 0.5 \mu\text{A}$) resistors, R (Figure 16) can be omitted. If the MC1594 is used in an ac mode of operation and capacitive coupling is used the value of resistor R can be any reasonable value up to 100 k Ω . For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

2.8 Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network

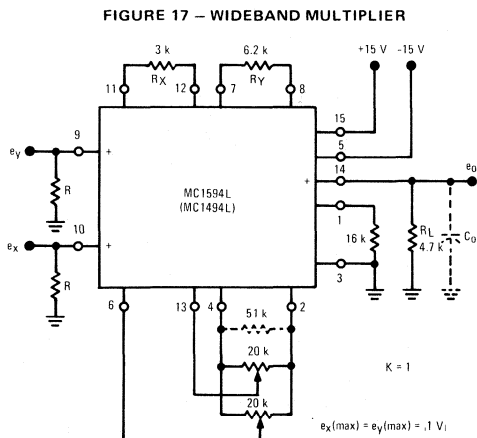
is to reduce the "Q" of the source-tuned circuits which cause the oscillation.

Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

3. AC OPERATION

3.1 General

For ac operation, such as balanced modulation, frequency doubler, AGC, etc., the op-amp. will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be ac-coupled and the dc voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 17



shows a typical ac multiplier circuit with a scale factor $K \approx 1$. Again, resistor R_X and R_Y are chosen as outlined in the previous section, with R_L chosen to provide the required scale factor.

The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1594 is typically $17 \mu A$ and $35 \mu A$ maximum. Thus, the maximum output offset would be about 160 mV.

3.2 Bandwidth

The bandwidth of the MC1594 is primarily determined by two factors. First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance (C_O) of 10 pF, the 3 dB bandwidth would be approximately 3.4 MHz. If the load resistor were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors R_X and R_Y and the transistors associated with them. The effect of these transmission

"zeros" is seen in Figures 9 and 10. The reason for this increase in gain is due to the bypassing of R_X and R_Y at high frequencies. Since the R_Y resistor is approximately twice the value of the R_X resistor, the zero associated with the "Y" input will occur at approximately one octave below the zero associated with the "X" input. For $R_X = 30 k\Omega$ and $R_Y = 62 k\Omega$, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7 MHz respectively.

It should be noted that the MC1594 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a dc voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an ac voltage on both the "X" and "Y" side, such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for ac applications; (1) the value of resistors R_X , R_Y and R_L should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor R_L such that the dominant pole (R_L, C_O) cancels the input zero ($R_X, 3.5 pF$ or $R_Y, 3.5 pF$) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10. Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the ac signal.

For ac applications requiring bandwidths greater than those specified for the MC1594, two other devices are recommended. For modulator-demodulator applications, the MC1596 may be used up to 100 MHz. For wideband multiplier applications, the MC1595 (using small collector loads and ac coupling) can be used.

3.3 Slew-Rate

The MC1594 multiplier is not slew-rate limited in the ordinary sense that an op-amp. is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitations. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew-Rate} = \frac{\Delta V_O}{\Delta T} = \frac{I_O}{C}$$

Thus, if C_O is 10 pF, the maximum slew-rate would be:

$$\frac{\Delta V_O}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50 \text{ V}/\mu\text{s}$$

This can be improved if necessary by addition of an emitter-follower or other type of buffer.

3.4 Phase-Vector Error

All multipliers are subject to an error which is known as the phase-vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase-vector

B. DC Procedure:

1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_O = 0.0$ Vdc
2. Set $V_X = V_Y = 1.0$ V and adjust P1 (Y input offset potentiometer) such that the output voltage is -0.100 volts
3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is -10.00 volts
4. Set $V_X = V_Y = -10$ Vdc and check that $V_O = -10$ V. Repeat steps 1 through 4 as necessary.

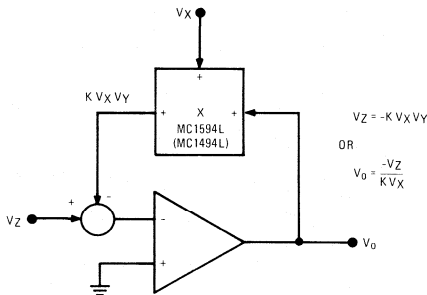
4.2 Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21.

The characteristic "failure" mode of the divide circuit is latch-up. One way it can occur is if V_X is allowed to go negative or, in some cases, if V_X approaches zero.

Figure 20 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is non-inverting. Its output is fed to the inverting input of the op-amp. Thus, operation is in the negative feedback mode and the circuit is dc stable. Should V_X change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from

FIGURE 20 - BASIC DIVIDE CIRCUIT USING MULTIPLIER



V_X being near zero is a result of the transfer through the multiplier being near zero. The op-amp. is then operating with a very high closed loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op-amp. exceeding the rated common-mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op-amp. to approximately ± 10.7 volts. Five-percent tolerance, 10-volt zeners are used to assure adequate output swing but still limit the output voltage of the op-amp. from exceeding the common-mode input range of the MC1594.

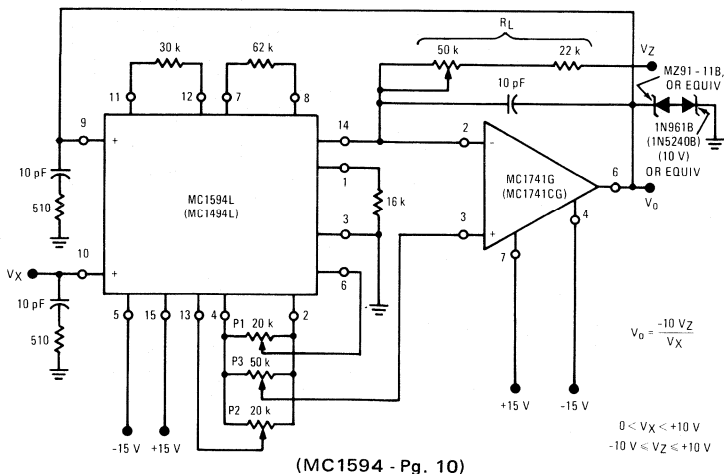
Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P3) until the output voltage (V_O) remains at some (not necessarily zero) constant value as V_X is varied between $+1.0$ volt and $+10$ volts.
2. Maintain V_Z at 0 volts, set V_X at $+10$ volts and adjust the Y input offset potentiometer (P1) until $V_O = 0$ volts.
3. With $V_X = V_Z$, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily -10 volts) constant value as $V_Z = V_X$ is varied between $+1.0$ volt and $+10$ volts.
4. Maintain $V_X = V_Z$ and adjust the scale factor potentiometer (R_L) until the average value of V_O is -10 volts as $V_Z = V_X$ is varied between $+1.0$ volt and $+10$ volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

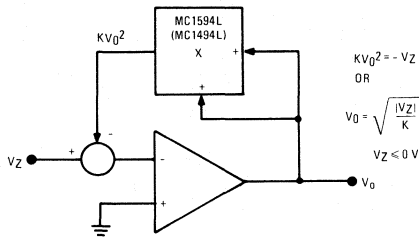
Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denomi-

FIGURE 21 - PRACTICAL DIVIDE CIRCUIT



(MC1594 - Pg. 10)

FIGURE 22 – BASIC SQUARE ROOT CIRCUIT



nator voltage. As a result, if V_X is set to 10 volts and 0.5% accuracy is available, then 5% accuracy can be expected when V_X is only 1 volt.

In accordance with an earlier statement, V_X may have only one polarity, positive, while V_Z may be either polarity.

4.3 Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up.

This circuit too, may be adjusted in the closed-loop mode:

1. Set $V_Z = -0.01$ Vdc and adjust P3 (output offset) for $V_0 = 0.316$ Vdc.
2. Set V_Z to -0.9 Vdc and adjust P2 ("X" adjust) for $V_0 = +3$ Vdc.
3. Set V_Z to -10 Vdc and adjust P4 (gain adjust) for $V_0 = +10$ Vdc.

Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

Note: Operation near zero volts input may prove very inaccurate, hence, it may not be possible to adjust V_0 to 0 but rather only to within 100 to 400 mV of zero.

5. AC APPLICATIONS

5.1 Wideband Amplifier With Linear AGC

If one input to the MC1594 is a dc voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the dc voltage. Hence, the multiplier can function as a dc coupled, wideband amplifier with linear AGC control.

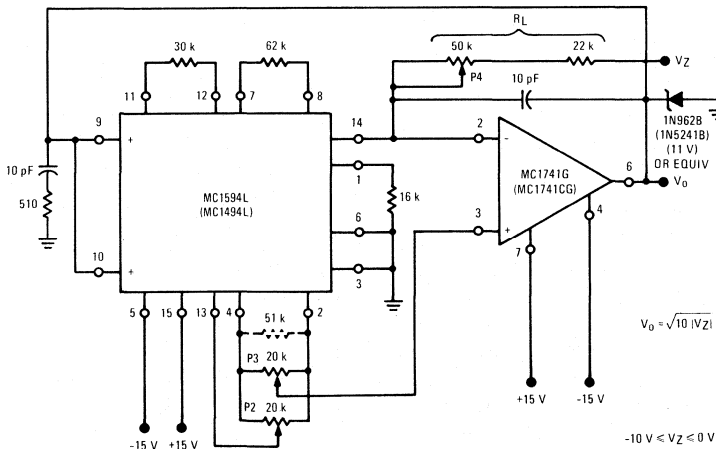
In addition to the advantage of Linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with zero volts dc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using carmet multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output-voltage-swing capability and output impedance are unchanged with variations in AGC voltage.

The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier can handle 1 V(rms) and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter-follower buffer has been added to extend the bandwidth in excess of 1 MHz.

5.2 Balanced Modulator

When two-time variant signals are used as inputs, the result-

FIGURE 23 – SQUARE ROOT CIRCUIT



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ing output is suppressed-carrier double-sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

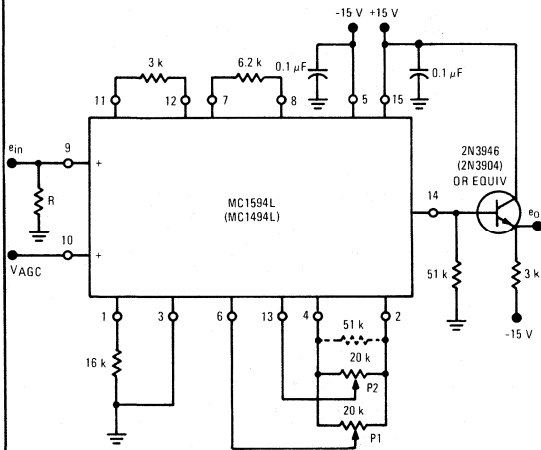
$$V_o = K(e_1 \cos \omega_m t)(e_2 \cos \omega_c t)$$

where ω_m is the modulation frequency and ω_c is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_o = \frac{Ke_1e_2}{2} [\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

Unlike many modulation schemes, which are non-linear in nature, the modulation which takes place when using the MC1594 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 25 shows the MC1594 configuration to perform this function.

FIGURE 24 – WIDEBAND AMPLIFIER WITH LINEAR AGC

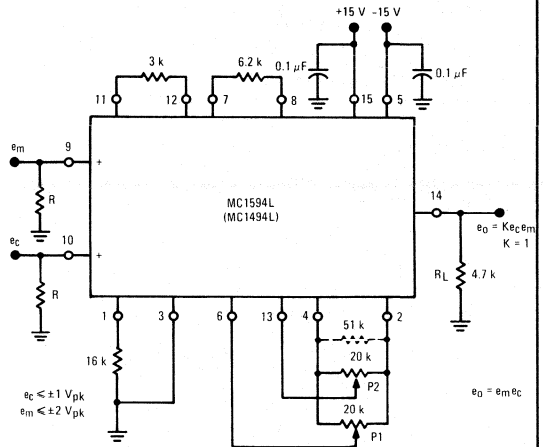


Notice that the resistor values for R_X , R_Y , and R_L have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1594 and then lowering R_X and R_Y to achieve a gain of 1. The e_c can be as large as 1 volt peak and e_m as high as 2 volts peak. No output offset adjust is employed since we are interested only in the ac output components.

The input R 's are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 k ohm output impedance and capacitive loading. Assuming a 6 pF load, the small-signal bandwidth is 5.5 MHz.

The circuit of Figure 25 will provide a typical carrier rejection of ≥ 70 dB from 10 kHz to 1.5 MHz.

FIGURE 25 – BALANCED MODULATOR



The adjustment procedure for this circuit is quite simple.

- (1) Place the carrier signal at pin 10. With no signal applied to pin 9, adjust potentiometer P1 such that an ac null is obtained at the output.
- (2) Place a modulation signal at pin 9. With no signal applied to pin 10, adjust potentiometer P2 such that an ac null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

5.3 Frequency Doubler

If for Figure 25 both inputs are identical;

$$e_m = e_c = E \cos \omega t$$

Then the output is given by

$$e_o = e_m e_c = E^2 \cos^2 \omega t$$

which reduces to

$$e_o = \frac{E^2}{2} (1 + \cos 2\omega t)$$

This equation states that the output will consist of a dc term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires no filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2 MHz.

5.4 Amplitude Modulator

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the modu-

lation input. This procedure places a dc offset on the modulation input of the multiplier such that the carrier still passes thru the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with $K = 1$,

$$e_o = (E + E_m \cos \omega_m t) (E_c \cos \omega_c t)$$

where E is the dc input offset adjust voltage. This expression can be written as:

$$e_o = E_o [1 + M \cos \omega_m t] \cos \omega_c t$$

where $E_o = EE_c$

and $M = \frac{E_m}{E} = \text{modulation index}$

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation, E_m . This is done by observing the output waveform and adjusting the input offset potentiometer, P1, until the output exhibits the familiar amplitude modulation waveform.

5.5 Phase Detector

If the circuit of Figure 25 has as its inputs two signals of identical frequency but having a relative phase shift the output will be a dc signal which is directly proportional to the cosine of phase difference as well as the double frequency term.

$$e_c = E_c \cos \omega_c t$$

$$e_m = E_m \cos(\omega_c t + \phi)$$

$$e_o = e_c e_m = E_c E_m \cos \omega_c t \cos(\omega_c t + \phi)$$

or
$$e_o = \frac{E_c E_m}{2} [\cos \phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of R_L to an offset adjustment potentiometer will result in a dc output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

6. DEFINITIONS OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of this mystery, the following definitions and examples are presented.

6.1 Multiplier Transfer Function

The output of the multiplier may be expressed by this equation:

$$V_o = K (V_x \pm V_{ioX} - V_{x\ off}) (V_y \pm V_{ioY} - V_{y\ off}) \pm V_{oo} \quad (1)$$

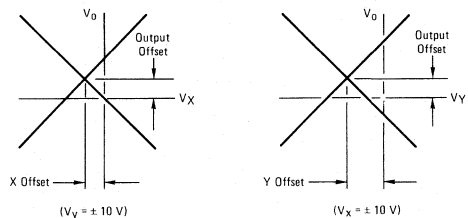
where K = scale factor (see 6.5)

- V_x = "x" input voltage
- V_y = "y" input voltage
- V_{ioX} = "x" input offset voltage
- V_{ioY} = "y" input offset voltage
- $V_{x\ off}$ = "x" input offset adjust voltage

- $V_{y\ off}$ = "y" input offset adjust voltage
- V_{oo} = output offset voltage

The voltage transfer characteristic below indicates "X", "Y" and output offset voltages.

FIGURE 26



6.2 Linearity

Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full-scale output and is measured for V_x and V_y separately either using an "X-Y" plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_o = \frac{V_x V_y}{10} \pm (0.0035) (10 \text{ volts})$$

6.3 Input Offset Voltage

The input offset voltage is defined from Equation (1). It is measured for V_x and V_y separately and is defined to be that dc input offset adjust voltage ("x" or "y") that will result in minimum ac output when ac (5 Vpp, 1 kHz) is applied to the other input ("y" or "x" respectively). From Equation (1) we have:

$$V_o(ac) = K (0 \pm V_{ioX} - V_{x\ off}) (\sin \omega t)$$

adjust $V_{x\ off}$ so that $(\pm V_{ioX} - V_{x\ off}) = 0$.

6.4 Output Offset Current and Voltage

Output offset current (I_{oo}) is the dc current flowing in the output lead when $V_x = V_y = 0$ and "X" and "Y" offset voltages are adjusted to zero.

Output offset voltage (V_{oo}) is:

$$V_{oo} = I_{oo} R_L$$

where R_L is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting "X" and "Y" offset voltages to zero. Thus it includes input offset terms, an output offset term and a scale factor term.

6.5 Scale Factor

Scale factor is the K term in Equation (1). It determines the "gain" of the multiplier and is expressed approximately by the following equation.

$$K = \frac{2R_L}{R_x R_y I_1} \text{ where } R_x \text{ and } R_y \gg \frac{kT}{qI_1}$$

and I_1 is the current out of pin 1.

6.6 Total DC Accuracy

The total dc accuracy of a multiplier is defined as error in multiplier output with dc (± 10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1594 because error terms can be nulled by the user.

6.7 Temperature Stability (Drift)

Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by re-adjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by:

$$\Delta V_o = \pm [K \pm K (TCK) (\Delta T)] [(TCV_{ioX}) (\Delta T)] [(TCV_{ioY}) (\Delta T)] \pm (TCV_{oo}) (\Delta T)$$

6.8 Total DC Accuracy Drift

This is the temperature drift in output voltage with 10 volts applied to each input. The output is adjusted to 10 volts at $T_A = +25^\circ C$. Assuming initial offset voltages have been adjusted to zero at $T_A = +25^\circ C$, then:

$$V_o = [K \pm K (TCK) (\Delta T)] [10 \pm (TCV_{ioX}) (\Delta T)] [10 \pm (TCV_{ioY}) (\Delta T)] \pm (TCV_{oo}) (\Delta T)$$

6.9 Power Supply Rejection

Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1-volt, 100-Hz signal on each supply (± 15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

6.10 Output Voltage Swing

Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load (note: output offset is adjusted to zero).

If an op-ampl. is used, the multiplier output becomes a virtual ground — the swing is then determined by the scale factor and the op-ampl. selected.

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- 1.3 Multiplier
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- 2.3 Stability
- 2.4 Offset Adjustment
- 2.5 Offset and Scale Factor Adjustment Procedure
- 2.6 Temperature Stability
- 2.7 Bias Currents
- 2.8 Parasitic Oscillation

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- 3.3 Slew-Rate
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- 3.5 Circuit Layout

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- 6.9 Power Supply Rejection
- 6.10 Output Voltage Swing

MC1595L MC1495L

Specifications and Applications Information

WIDEBAND MONOLITHIC FOUR-QUADRANT MULTIPLIER

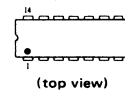
... designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier.

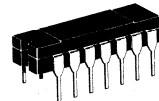
- Wide Bandwidth
- Excellent Linearity – 1% max Error on X-Input, 2% max Error on Y-Input – MC1595L
- Excellent Linearity – 2% max Error on X-Input, 4% max Error on Y-Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts
- ± 15 Volt Operation

LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED



(top view)



CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 – FOUR-QUADRANT
MULTIPLIER TRANSFER CHARACTERISTIC

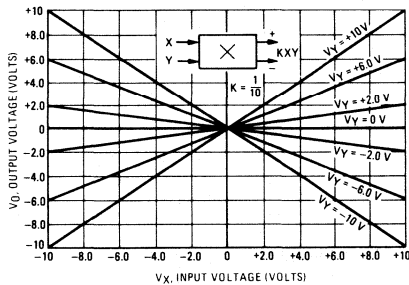


FIGURE 2 – TRANSCONDUCTANCE BANDWIDTH

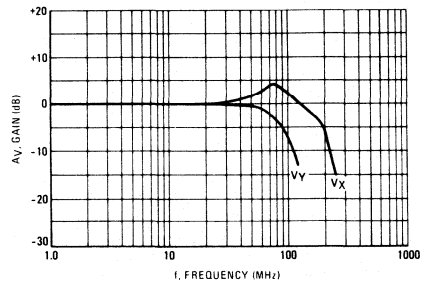
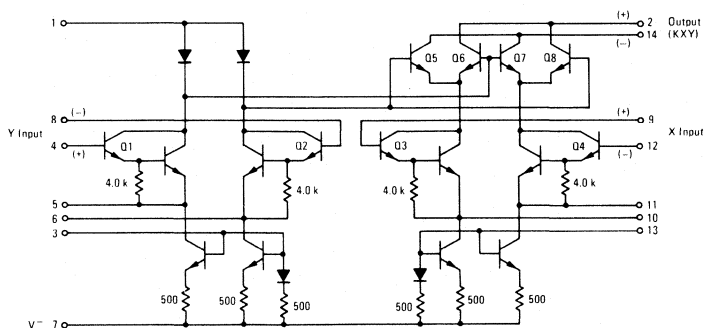


FIGURE 3 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

See current MCC1595/1495 data sheet for standard linear chip information.

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MC1595L, MC1495L (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +32V$, $V^- = -15V$, $T_A = +25^\circ C$, $I_3 = I_{13} = 1\text{ mA}$, $R_X = R_Y = 15\text{ k}\Omega$, $R_L = 11\text{ k}\Omega$ unless otherwise noted)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|--|--------|--|----------------------------|--|--|--------------------------|
| Linearity: Output Error in Percent of Full Scale: $T_A = +25^\circ C$ $-10 < V_X < +10$ ($V_Y = \pm 10\text{ V}$) MC1495 MC1595 $-10 < V_Y < +10$ ($V_X = \pm 10\text{ V}$) MC1495 MC1595 $T_A = 0$ to $+70^\circ C$ MC1495 $-10 < V_X < +10$ ($V_Y = \pm 10\text{ V}$) $-10 < V_Y < +10$ ($V_X = \pm 10\text{ V}$) $T_A = -55^\circ C$ to $+125^\circ C$ MC1595 $-10 < V_X < +10$ ($V_Y = \pm 10\text{ V}$) $-10 < V_Y < +10$ ($V_X = \pm 10\text{ V}$) | 5 | E_{RX} E_{RY} E_{RX} E_{RY} E_{RX} E_{RY} | — — — — — — | ± 1.0 ± 0.5 ± 2.0 ± 1.0 ± 1.5 ± 3.0 ± 0.75 ± 1.50 | ± 2.0 ± 1.0 ± 4.0 ± 2.0 — — — — | % |
| Squaring Mode Error: Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment $T_A = +25^\circ C$ MC1495 MC1595 $T_A = 0$ to $+70^\circ C$ MC1495 $T_A = -55^\circ C$ to $+125^\circ C$ MC1595 | 5 | E_{SQ} | — — — — | ± 0.75 ± 0.5 ± 1.0 ± 0.75 | — — — — | % |
| Scale Factor (Adjustable) $(K = \frac{2R_L}{I_3 R_X R_Y})$ | — | K | — | 0.1 | — | — |
| Input Resistance ($f = 20\text{ Hz}$) MC1495 MC1595 MC1495 MC1595 | 7 | R_{INX} R_{INY} | — — — — | 20 35 20 35 | — — — — | MegOhms |
| Differential Output Resistance ($f = 20\text{ Hz}$) | 8 | R_o | — | 300 | — | k Ohms |
| Input Bias Current $I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$ MC1495 MC1595 MC1495 MC1595 | 6 | I_{bx} I_{by} | — — — — | 2.0 2.0 2.0 2.0 | 12 8.0 12 8.0 | μA |
| Input Offset Current $ I_9 - I_{12} $ MC1495 MC1595 $ I_4 - I_8 $ MC1495 MC1595 | 6 | $ I_{iox} $ $ I_{ioy} $ | — — — — | 0.4 0.2 0.4 0.2 | 2.0 1.0 2.0 1.0 | μA |
| Average Temperature Coefficient of Input Offset Current ($T_A = 0$ to $+70^\circ C$) MC1495 ($T_A = -55^\circ C$ to $+125^\circ C$) MC1595 | 6 | $ TC_{Iio} $ | — — | 2.0 2.0 | — — | $nA/^\circ C$ |
| Output Offset Current $ I_{14} - I_{12} $ MC1495 MC1595 | 6 | $ I_{oo} $ | — — | 20 10 | 100 50 | μA |
| Average Temperature Coefficient of Output Offset Current ($T_A = 0$ to $+70^\circ C$) MC1495 ($T_A = -55^\circ C$ to $+125^\circ C$) MC1595 | 6 | $ TC_{Ioo} $ | — — | 20 20 | — — | $nA/^\circ C$ |
| Frequency Response 3.0 dB Bandwidth, $R_L = 11\text{ k}\Omega$ 3.0 dB Bandwidth, $R_L = 50\ \Omega$ (Transconductance Bandwidth) 3° Relative Phase Shift Between V_X and V_Y 1% Absolute Error Due to Input-Output Phase Shift | 9,10 | BW_{3dB} $T_{BW3\text{ dB}}$ f_ϕ f_θ | — — — — | 3.0 80 750 30 | — — — — | MHz MHz kHz kHz |
| Common Mode Input Swing (Either Input) MC1495 MC1595 | 11 | CMV | ± 10.5 ± 11.5 | ± 12 ± 13 | — — | Vdc |
| Common Mode Gain (Either Input) MC1495 MC1595 | 11 | A_{CM} | -40 -50 | -50 -60 | — — | dB |
| Common Mode Quiescent Output Voltage | 12 | V_{o1} V_{o2} | — — | 21 21 | — — | Vdc |
| Differential Output Voltage Swing Capability | 9 | V_o | — | ± 14 | — | V_{peak} |
| Power Supply Sensitivity | 12 | S^+ S^- | — — | 5.0 10 | — — | mV/V |
| Power Supply Current | 12 | I_7 | — | 6.0 | 7.0 | mA |
| DC Power Dissipation | 12 | P_D | — | 135 | 170 | mW |

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---------------------------|---|--------------------------------------|
| Applied Voltage ($V_2-V_1, V_{14}-V_1, V_1-V_9, V_1-V_{12}, V_1-V_4,$ $V_1-V_8, V_{12}-V_7, V_9-V_7, V_8-V_7, V_4-V_7$) | ΔV | 30 | Vdc |
| Differential Input Signal | $V_{12}-V_9$ V_4-V_8 | $\pm(6+I_{13} R_X)$ $\pm(6+I_3 R_Y)$ | Vdc Vdc |
| Maximum Bias Current | I_3 I_{13} | 10 10 | mA |
| Power Dissipation (Package Limitation) Ceramic Package Derate above $T_A = +25^\circ\text{C}$ | P_D | 750 5.0 | mW mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | 0 to +70 -55 to +125 | $^\circ\text{C}$ $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

TEST CIRCUITS

FIGURE 4 – LINEARITY (USING NULL TECHNIQUE)

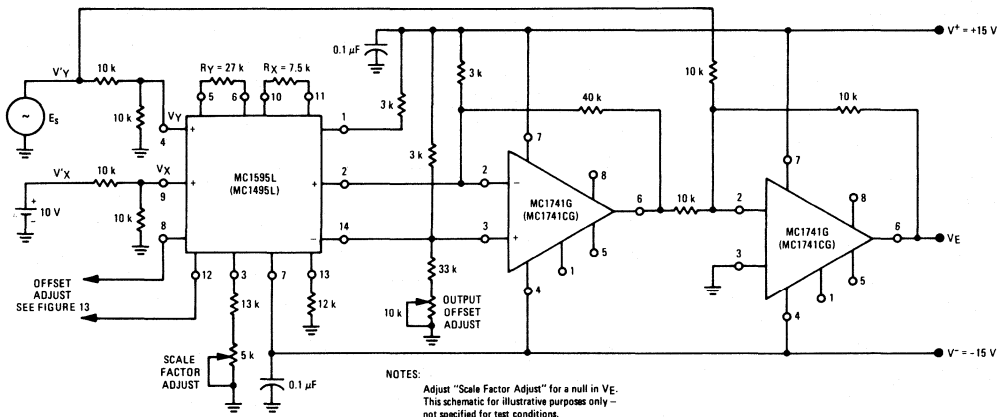
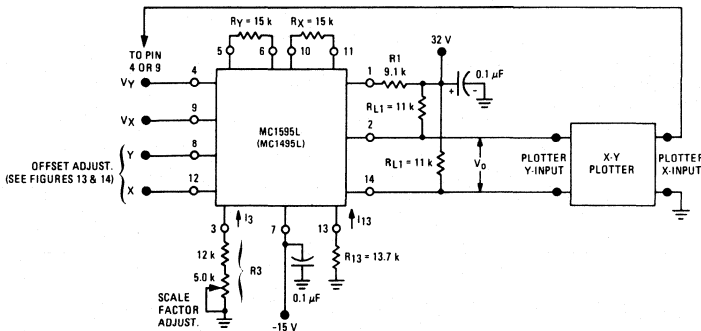


FIGURE 5 – LINEARITY (USING X-Y PLOTTER TECHNIQUE)



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TEST CIRCUITS (continued)

FIGURE 6 – INPUT AND OUTPUT CURRENT

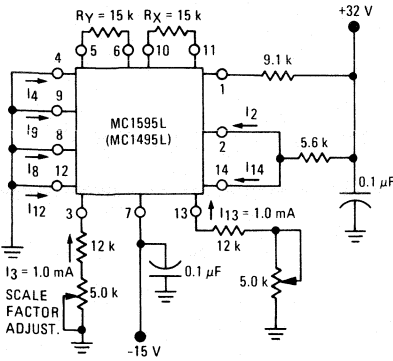
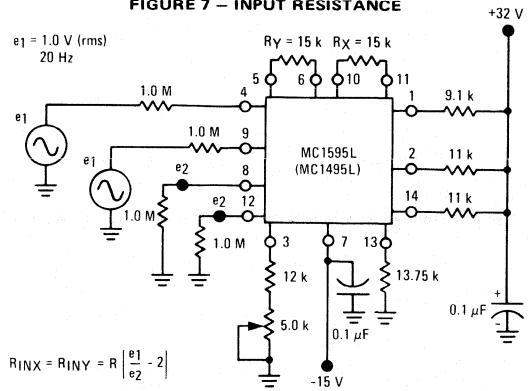
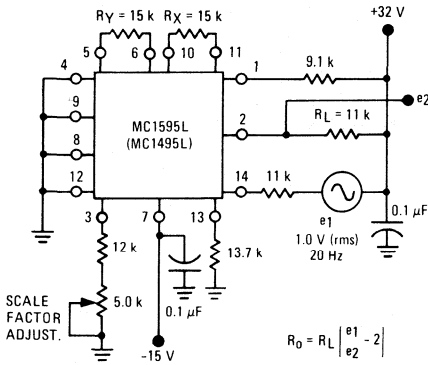


FIGURE 7 – INPUT RESISTANCE



$$R_{INX} = R_{INY} = R \left| \frac{e_1}{e_2} - 2 \right|$$

FIGURE 8 – OUTPUT RESISTANCE



$$R_o = R_L \left| \frac{e_1}{e_2} - 2 \right|$$

FIGURE 9 – BANDWIDTH ($R_L = 11 \text{ k}\Omega$)

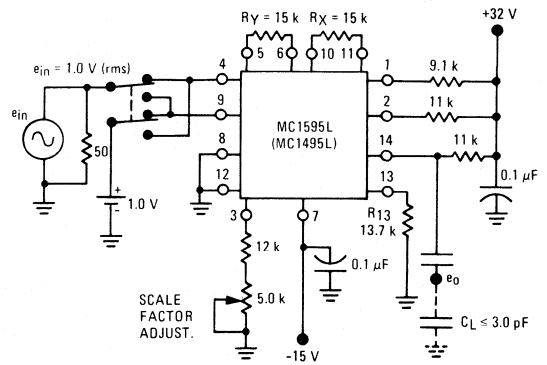


FIGURE 10 – BANDWIDTH ($R_L = 50 \Omega$)

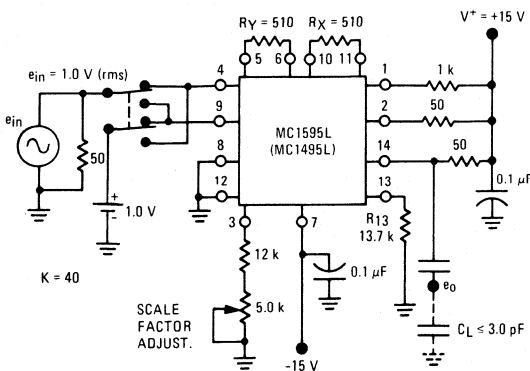
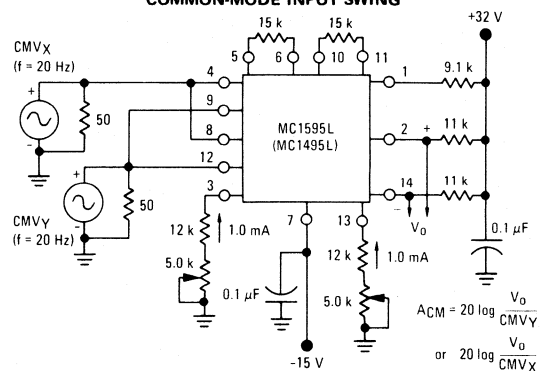


FIGURE 11 – COMMON-MODE GAIN and COMMON-MODE INPUT SWING



$$ACM = 20 \log \frac{V_o}{CMV_X}$$

$$\text{or } 20 \log \frac{V_o}{CMV_X}$$

TEST CIRCUITS (continued)

FIGURE 12 – POWER SUPPLY SENSITIVITY

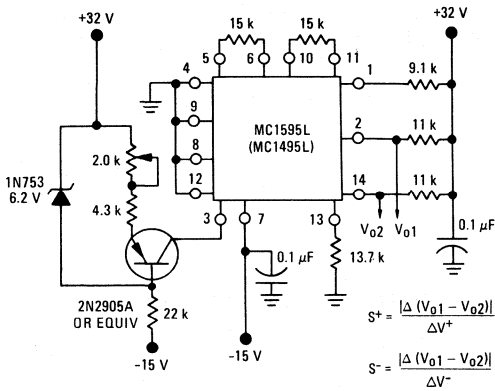


FIGURE 13 – OFFSET ADJUST CIRCUIT

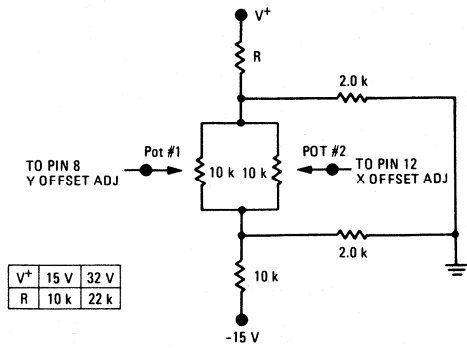
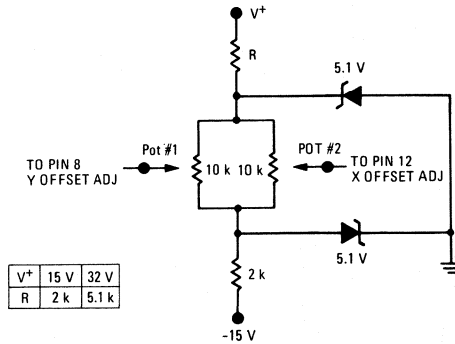


FIGURE 14 – OFFSET ADJUST CIRCUIT (ALTERNATE)



TYPICAL CHARACTERISTICS

FIGURE 15 – LINEARITY versus TEMPERATURE

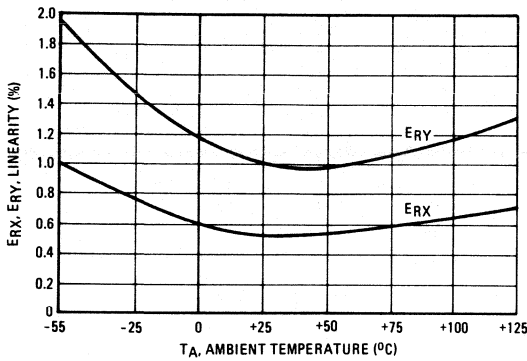


FIGURE 16 – SCALE FACTOR versus TEMPERATURE

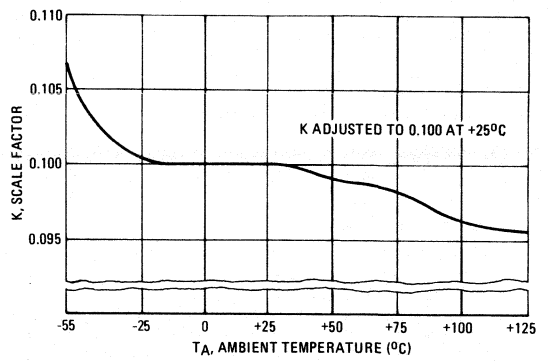


FIGURE 17 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

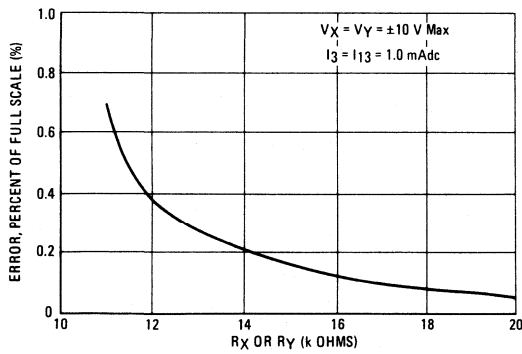


FIGURE 18 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

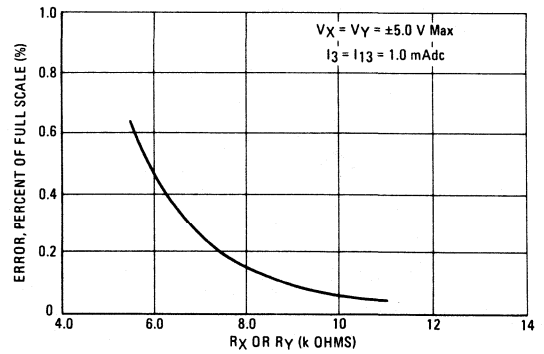
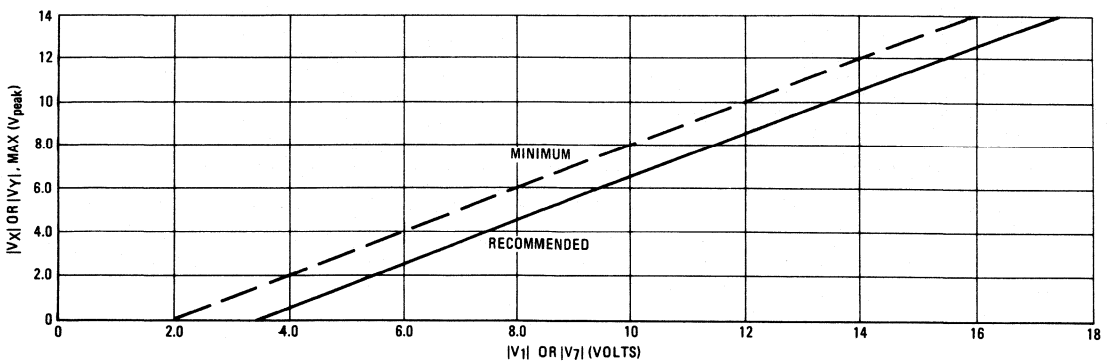


FIGURE 19 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7



OPERATION AND APPLICATIONS INFORMATION

1. Theory of Operation

The MC1595 (MC1495) is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. The detailed theory of operation is covered in Application Note AN-489, Analysis and Basic Operation of the MC1595. The result of this analysis is that the differential output current of the multiplier is given by

$$I_A - I_B = \Delta I = \frac{2V_X V_Y}{R_X R_Y I_3}$$

where I_A and I_B are the currents into pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

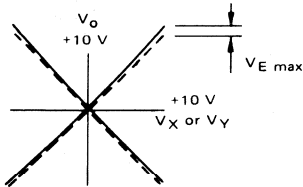
2. Design Considerations

2.1 General

The MC1595 (MC1495) permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

2.1.1 Linearity, Output Error, E_{RX} or E_{RY}

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_{E(max)}$, is ± 100 mV and the full scale output is 10 volts, then the percentage error is

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%$$

Linearity error may be measured by either of the following methods:

1. Using an X - Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input. The peak output of the null operational amplifier will be equal to the error voltage, $V_{E(max)}$.

One source of linearity error can arise from large signal non-linearity in the X and Y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that non-linear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

2.1.2 3 dB-Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transmittance in the X and Y channels). If the input to output phase shift is only 0.6° , the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

2.1.3 Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ maximum input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$

$$V_{Y(max)} < I_3 R_Y$$

Exceeding this value will drive one side of the input amplifier to "cutoff" and cause non-linear operation.

Currents I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

$$\text{For } V_{X(max)} = V_{Y(max)} = 10 \text{ volts;}$$

$$R_X = R_Y > \frac{10 \text{ V}}{1.0 \text{ mA}} = 10 \text{ k}\Omega$$

The equation $I_A - I_B = \frac{2V_X V_Y}{R_X R_Y I_3}$

$$\text{is derived from } I_A - I_B = \frac{2V_X V_Y}{(R_X + \frac{2kT}{qI_{13}})(R_Y + \frac{2kT}{qI_3}) I_3}$$

$$\text{with the assumption } R_X \gg \frac{2kT}{qI_{13}} \text{ and } R_Y \gg \frac{2kT}{qI_3}$$

$$\text{At } T_A = +25^\circ\text{C and } I_{13} = I_3 = 1 \text{ mA,}$$

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52 \Omega$$

Therefore, with $R_X = R_Y = 10 \text{ k}\Omega$ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7 . Exceeding these limits will cause saturation or "cutoff" of the input transistors. See Step 4 of Section 3 (General Design Procedure) for further details.

2.1.4 Maximum Output Voltage Swing

The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at pin 1 for negative swing. The potential at pin 1 determines the quiescent level for transistors Q_5 , Q_6 , Q_7 , and Q_8 . This potential

OPERATION AND APPLICATIONS INFORMATION (continued)

it can be seen that the resistor values necessary are given by:

$$R_{13} + 500 \Omega = \frac{|V^-| - 0.7 \text{ V}}{I_{13}}$$

$$R_3 + 500 \Omega = \frac{|V^-| - 0.7 \text{ V}}{I_3}$$

Let $V^- = -15 \text{ V}$

$$\text{Then } R_{13} + 500 = \frac{14.3 \text{ V}}{1 \text{ mA}} \text{ or } R_{13} = 13.8 \text{ k}\Omega$$

Let $R_{13} = 12 \text{ k}\Omega$

Similarly, $R_3 = 13.8 \text{ k}\Omega$

Let $R_3 = 15 \text{ k}\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3 , offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.), pins 3 and 13 can be connected together and a single resistor from pin 3 to ground can be used. In this case, the single resistor would have a value of one-half the above calculated value for R_{13} .

Step 2. The next step is to select R_X and R_Y . To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13} \quad \frac{V_Y}{R_Y} < I_3$$

A good rule of thumb is to make $I_3 R_Y \geq 1.5 V_{Y(\max)}$ and $I_{13} R_X \geq 1.5 V_{X(\max)}$.

The larger the $I_3 R_Y$ and $I_{13} R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

$$\text{Let } R_X = R_Y = 10 \text{ k}\Omega$$

$$\text{Then } I_3 R_Y = 10 \text{ V}$$

$$I_{13} R_X = 10 \text{ V}$$

since $V_{X(\max)} = V_{Y(\max)} = 5.0 \text{ volts}$ the value of $R_X = R_Y = 10 \text{ k}\Omega$ is sufficient.

Step 3. Now that R_X , R_Y and I_3 have been chosen, R_L can be determined:

$$K = \frac{2R_L}{R_X R_Y I_3} = \frac{4}{10}$$

$$\text{or } \frac{(2)(R_L)}{(10 \text{ k})(10 \text{ k})(1 \text{ mA})} = \frac{4}{10}$$

$$\text{Thus } R_L = 20 \text{ k}\Omega.$$

Step 4. To determine what power-supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1 , Q_2 , Q_3 and Q_4 in an active

region when the maximum input voltages are applied ($V_X' = V_Y' = 10 \text{ V}$ or $V_X = 5.0 \text{ V}$, $V_Y = 5.0 \text{ V}$), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 are at a potential which is two diode-drops below the voltage at pin 1. Thus, the voltage at pin 1 should be about two volts higher than the maximum input voltage. Therefore, to handle +5.0 volts at the inputs, the voltage at pin 1 must be at least +7.0 volts. Let $V_1 = 9.0 \text{ Vdc}$.

Since the current following into pin 1 is always equal to $2I_3$, the voltage at pin 1 can be set by placing a resistor, R_1 from pin 1 to the positive supply:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

Let $V^+ = +15 \text{ V}$

$$\text{Then } R_1 = \frac{15 \text{ V} - 9 \text{ V}}{(2)(1 \text{ mA})}$$

$$R_1 = 3 \text{ k}\Omega.$$

Note that the voltage at the base of transistors Q_5 , Q_6 , Q_7 and Q_8 is one diode-drop below the voltage at pin 1. Thus, in order that these transistors stay active, the voltage at pins 2 and 14 should be approximately halfway between the voltage at pin 1 and the positive-supply voltage. For this example, the voltage at pins 2 and 14 should be approximately 11 volts.

Step 5. Level Shifting

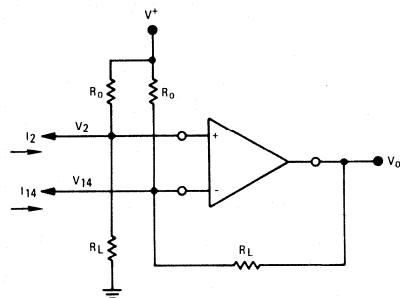
For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_o = (I_2 - I_{14}) R_L$$

$$\text{And since } I_A - I_B = I_2 - I_{14} = \frac{2I_X I_Y}{I_3} = \frac{2V_X V_Y}{I_3 R_X R_Y}$$

$$\text{Then } V_o = \frac{2R_L V_X V_Y}{4R_X R_Y I_3} \text{ where } V_X V_Y \text{ is the voltage at the input to the voltage dividers.}$$

FIGURE 22 - LEVEL SHIFT CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common-mode input voltage range as well as a high common-mode rejection ratio. The MC1556, and MC1741 operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13} . In Step 3, R_L was found to be 20 kΩ and in Step 4, V_2 and V_{14} were found to be approximately 11 volts. From this information, R_O can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V_2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_O}$$

And for this example, $\frac{11 \text{ V}}{20 \text{ k}\Omega} + 1 \text{ mA} = \frac{15 \text{ V} - 11 \text{ V}}{R_O}$

Solving for R_O , $R_O = 2.6 \text{ k}\Omega$

Thus, select $R_O = 3.0 \text{ k}\Omega$

For $R_O = 3.0 \text{ k}\Omega$, the voltage at pins 2 and 14 is calculated to be

$$V_2 = V_{14} = 10.4 \text{ volts.}$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are

possible as shown in Figure 23 where R_Y has been increased substantially to improve the Y linearity, and R_X decreased somewhat so as not to materially affect the X linearity, this avoids increasing R_L significantly in order to maintain a K of 0.1.

The versatility of the MC1595 (MC1495) allows the user to optimize its performance for various input and output signal levels.

4. Offset and Scale Factor Adjustment

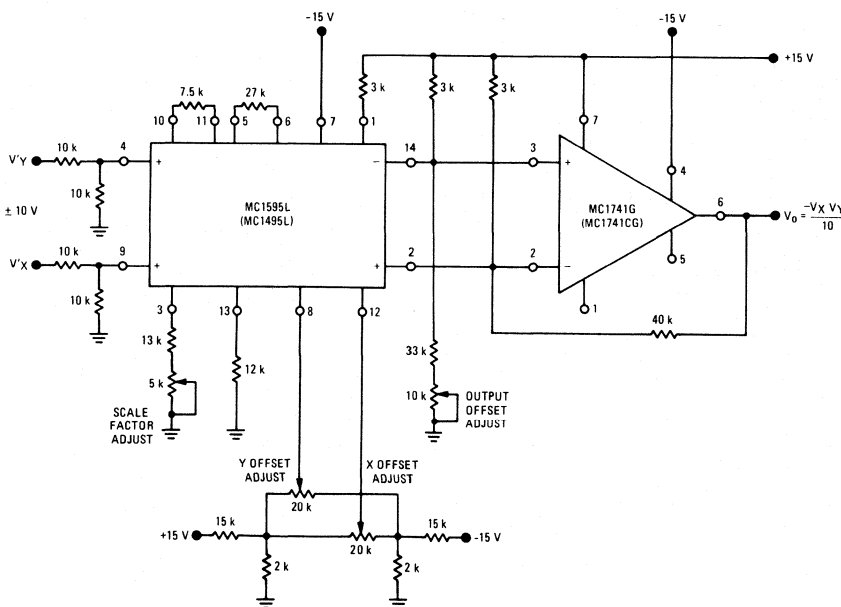
4.1 Offset Voltages

Within the monolithic multiplier (Figure 3) transistor base-emitter junctions are typically matched within 1 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X-input offset voltage, Y-input offset voltage, and output offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function:

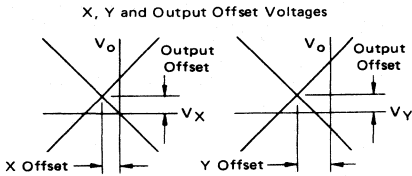
$$V_O = K(V_X \pm V_{IOX} \pm V_{X \text{ off}})(V_Y \pm V_{IOY} \pm V_{Y \text{ off}}) \pm V_{OO} \quad (1)$$

- Where K = scale factor
- V_X = X input voltage
- V_Y = Y input voltage
- V_{IOX} = X input offset voltage
- V_{IOY} = Y input offset voltage
- $V_{X \text{ off}}$ = X input offset adjust voltage
- $V_{Y \text{ off}}$ = Y input offset adjust voltage
- V_{OO} = output offset voltage.

FIGURE 23 – MULTIPLIER WITH IMPROVED LINEARITY



OPERATION AND APPLICATIONS INFORMATION (continued)



For most dc applications, all three offset adjust potentiometers (P₁, P₂, P₄) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (See Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

4.2 Scale Factor

The scale factor, K, is set by P₃ (Figure 21). P₃ varies I₃ which inversely controls the scale factor K. It should be noted that current I₃ is one-half the current through R₁. R₁ sets the bias level for Q₅, Q₆, Q₇, and Q₈ (See Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P₃ over wide voltage ranges (see Section 3, General Design Procedure).

4.3 Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation. (See Figure 21)

1. X Input Offset
 - (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 4)
 - (b) Connect "X" input (pin 9) to ground
 - (c) Adjust X offset potentiometer, P₂, for an ac null at the output
2. Y Input Offset
 - (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 9)
 - (b) Connect "Y" input (pin 4) to ground
 - (c) Adjust "Y" offset potentiometer, P₁, for an ac null at the output
3. Output Offset
 - (a) Connect both "X" and "Y" inputs to ground
 - (b) Adjust output offset potentiometer, P₄, until the output voltage V_O is zero volts dc
4. Scale Factor
 - (a) Apply +10 Vdc to both the "X" and "Y" inputs
 - (b) Adjust P₃ to achieve +10.00 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1595 (MC1495) depends upon the characteristics of potentiometers P₁ through P₄. Multi-turn, infinite resolution potentiometers with low-temperature coefficients are recommended.

5. DC Applications

5.1 Multiply

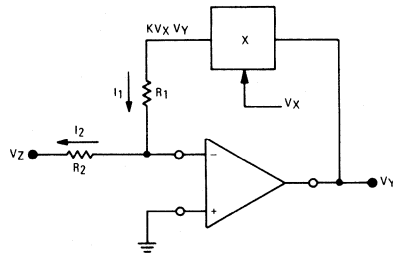
The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large — however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

5.2 Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is V_O = KV² where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

1. AC Procedure:
 - (a) Connect oscillator (1 kHz, 15 Vpp) to input
 - (b) Monitor output at 2 kHz with tuned voltmeter and adjust P₃ for desired gain (be sure to peak response of the voltmeter)
 - (c) Tune voltmeter to 1 kHz and adjust P₁ for a minimum output voltage
 - (d) Ground input and adjust P₄ (output offset) for zero volts dc output
 - (e) Repeat steps a through d as necessary.
2. DC Procedure:
 - (a) Set V_X = V_Y = 0 V and adjust P₄ (output offset potentiometer) such that V_O = 0.0 Vdc
 - (b) Set V_X = V_Y = 1.0 V and adjust P₁ (Y input offset potentiometer) such that the output voltage is +0.100 volts
 - (c) Set V_X = V_Y = 10 Vdc and adjust P₃ such that the output voltage is +10.00 volts
 - (d) Set V_X = V_Y = -10 Vdc. Repeat steps a through d as necessary.

FIGURE 24 — BASIC DIVIDE CIRCUIT



5.3 Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a "virtual ground" at the inverting (-) input. Assuming that the bias current of the operational amplifier is negligible, then I₁ = I₂ and

$$\frac{KV_X V_Y}{R_1} = \frac{-V_Z}{R_2} \tag{1}$$

Solving for V_Y,

$$V_Y = \frac{-R_1 V_Z}{R_2 K V_X} \tag{2}$$

If R₁ = R₂

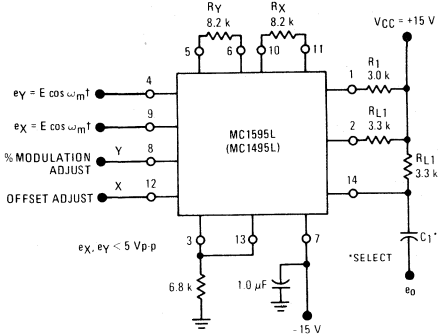
$$V_Y = \frac{-V_Z}{KV_X} \tag{3}$$

If R₁ = KR₂

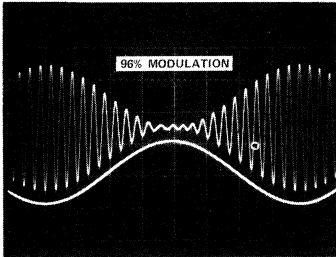
$$V_Y = \frac{-V_Z}{V_X} \tag{4}$$

OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 30 — AMPLITUDE MODULATION



(B)



The signal is applied to the unit's Y input. Since the total input range is limited to 1.0 volt p-p, a 2.0-volt swing, a current source of 2.0 mA and an R_Y value of 1.0 kilohm is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X input varies between 0 and +1.0 volt, the current source selected was 1.0 mA and the R_X value chosen was 2.0 kilohms. This also insures linear operation over the X input dynamic range.

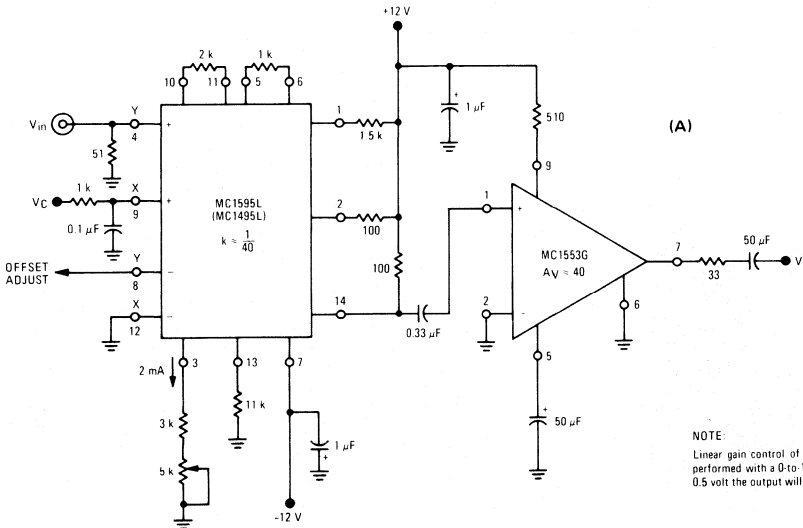
Choosing $R_L = 100$ assures wide-bandwidth operation. Hence, the scale factor for this configuration is

$$K = \frac{R_L}{R_X R_Y I_3} = \frac{100}{(2\text{ k})(1\text{ k})(2 \times 10^{-3})} \text{ V}^{-1} = \frac{1}{40} \text{ V}^{-1}$$

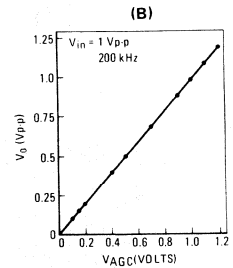
The 2 in the numerator of the equation is missing in this scale-factor expression because the output is single-ended and ac coupled.

To recover the gain, an MC152 video amplifier with a gain of 40 is used. An operational amplifier also could have been used with frequency compensation to allow a gain of 40 at 200 kHz. The MC1539 operational amplifier can be tailored for this use; and the MC1520 operational amplifier does it directly.

FIGURE 31 — LINEAR GAIN CONTROL



(A)



NOTE: Linear gain control of a 1-volt peak-to-peak signal is performed with a 0-to-1-volt control voltage. If V_C is 0.5 volt the output will be 0.5 volt p-p.

**OPERATIONS AND APPLICATIONS
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 - 2.1.2 3-dB Bandwidth and Phase Shift
 - 2.1.3 Maximum Input Voltage
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MC1596 MC1496

BALANCED MODULATOR-DEMODULATOR

Specifications and Applications Information

MONOLITHIC BALANCED MODULATOR – DEMODULATOR

... designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications.

- Excellent Carrier Suppression – 65 dB typ @ 0.5 MHz
– 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common-Mode Rejection – 85 dB typ

BALANCED MODULATOR – DEMODULATOR INTEGRATED CIRCUIT SILICON EPITAXIAL PASSIVATED



Pin 10 electrically connected to case through substrate.



Pin 14 electrically connected to substrate

G SUFFIX
METAL PACKAGE
CASE 602A

L SUFFIX
CERAMIC PACKAGE
CASE 632 (10-116)

FIGURE 1 – SUPPRESSED-CARRIER OUTPUT WAVEFORM

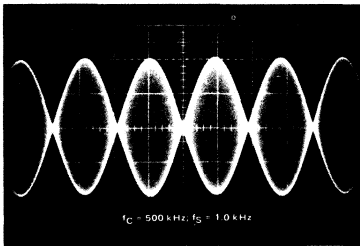


FIGURE 3 – SUPPRESSED-CARRIER SPECTRUM

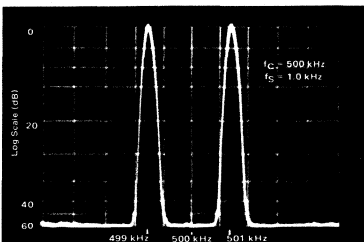


FIGURE 2 – AMPLITUDE-MODULATION OUTPUT WAVEFORM

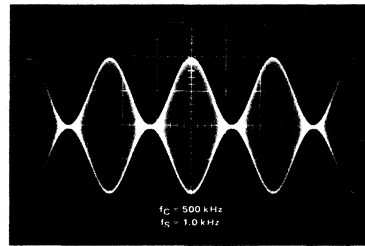


FIGURE 4 – AMPLITUDE-MODULATION SPECTRUM

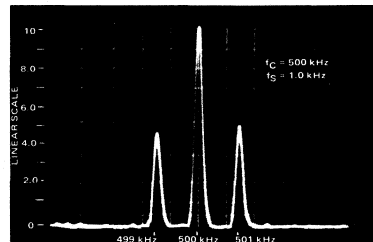
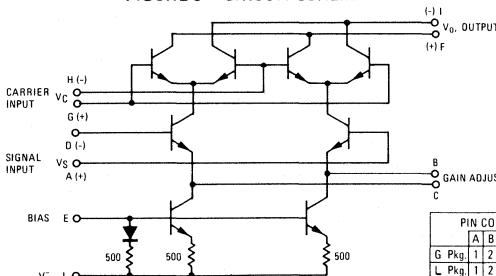
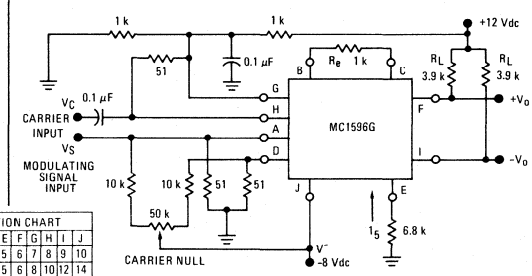


FIGURE 5 – CIRCUIT SCHEMATIC



| PIN CONNECTION CHART | |
|----------------------|------------------------|
| | A B C D E F G H I J |
| G Pkg | 1 2 3 4 5 6 7 8 9 10 |
| L Pkg | 1 2 3 4 5 6 8 10 12 14 |

FIGURE 6 – TYPICAL MODULATOR CIRCUIT



See Packaging Information Section for outline dimensions.

GENERAL OPERATING INFORMATION *

Note 1 – Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R₁ of Figure 7).

Note 2 – Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 24. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Note 3 and Figure 22). Note also that an optimum carrier level is recommended in Figure 24 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 – Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I₅

$$V_S \leq I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 12, V_S corresponds to a maximum value of 1 volt peak.

Note 4 – Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 – Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming V₉ = V₆, I₅ = I₆ = I₉ and ignoring

base current, P_D = 2 I₅ (V₆ – V₁₀) + I₅ (V₅ – V₁₀) where subscripts refer to pin numbers.

Note 6 – Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions. See Note 3 for R_e equation.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_9$$

$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V^- - \phi}{I_5} - 500 \Omega \text{ where: } R_5 \text{ is the resistor between pin 5 and ground}$$

$$\phi = 0.75 \text{ V at } T_A = +25^\circ\text{C}$$

The MC1596 has been characterized for the condition I₅ = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L$$

Note 7 – Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30 \text{ Vdc} \geq [(V_6, V_9) - (V_7, V_8)] \geq 2 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_7, V_8) - (V_1, V_4)] \geq 2.7 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7 \text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_9, \quad V_7 = V_8, \quad V_1 = V_4$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 – Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21C} = \left. \frac{i_o \text{ (each sideband)}}{v_s \text{ (signal)}} \right|_{V_o = 0}$$

Signal transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21S} = \left. \frac{i_o \text{ (signal)}}{v_s \text{ (signal)}} \right|_{V_c = 0.5 \text{ Vdc}, V_o = 0}$$

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

MC1596, MC1496 (continued)

Note 9 – Coupling and Bypass Capacitors C_1 and C_2

Capacitors C_1 and C_2 (Figure 7) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

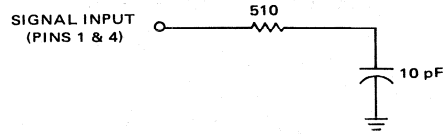
Note 10 – Output Signal, V_o

The output signal is taken from pins 6 and 9, either balanced or single-ended. Figure 14 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Note 11 – Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be

connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternate method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 1 and 4. In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

FIGURE 7 – CARRIER REJECTION AND SUPPRESSION

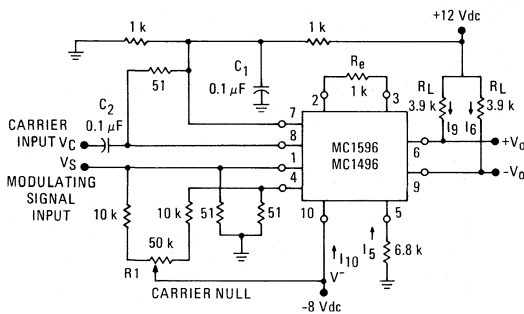


FIGURE 8 – INPUT-OUTPUT IMPEDANCE

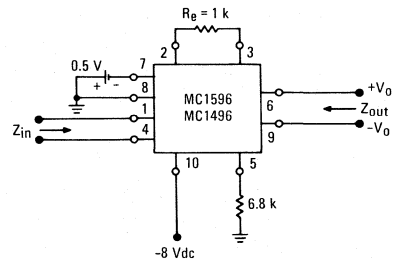


FIGURE 9 – BIAS AND OFFSET CURRENTS

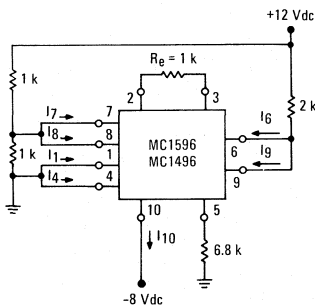
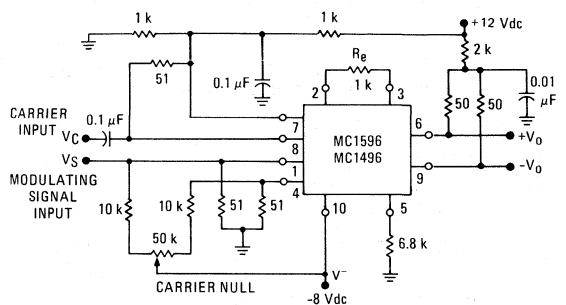


FIGURE 10 – TRANSCONDUCTANCE BANDWIDTH



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TEST CIRCUITS (continued)

FIGURE 11 – COMMON-MODE GAIN

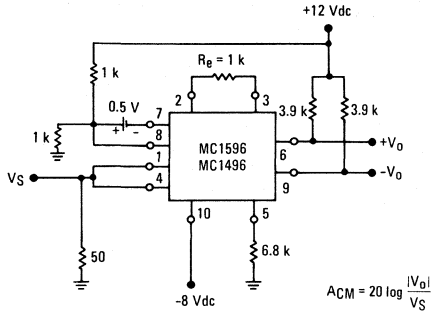
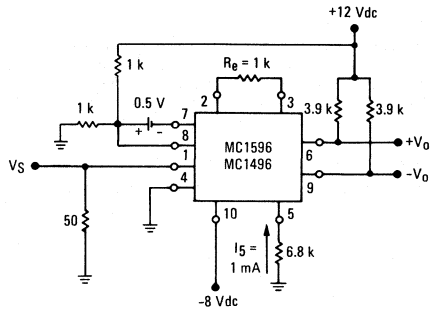


FIGURE 12 – SIGNAL GAIN AND OUTPUT SWING



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 7, $f_C = 500$ kHz (sine wave), $V_C = 60$ mV(rms), $f_S = 1$ kHz, $V_S = 300$ mV(rms), $T_A = +25^\circ\text{C}$ unless otherwise noted.

FIGURE 13 – SIDEBAND OUTPUT versus CARRIER LEVELS

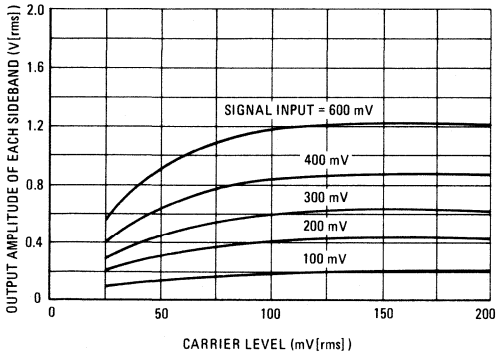


FIGURE 14 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY

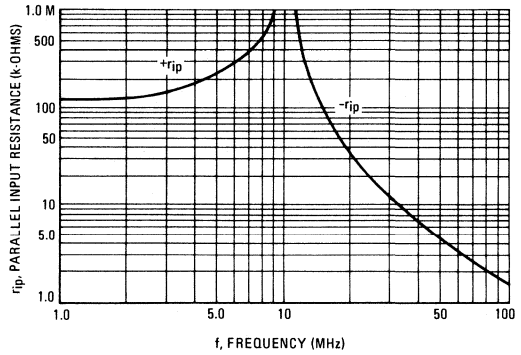


FIGURE 15 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

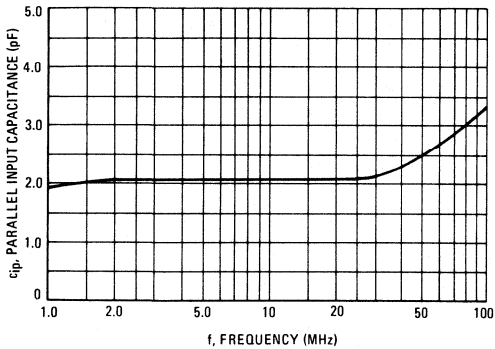
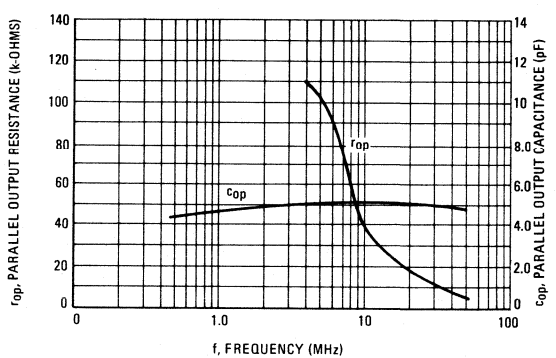


FIGURE 16 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



7

TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 7, $f_c = 500$ kHz (sine wave), $V_C = 60$ mV(rms), $f_S = 1$ kHz, $V_S = 300$ mV(rms), $T_A = +25^\circ\text{C}$ unless otherwise noted.

FIGURE 17 – SIDEBAND AND SIGNAL PORT TRANSMITTANCES versus FREQUENCY

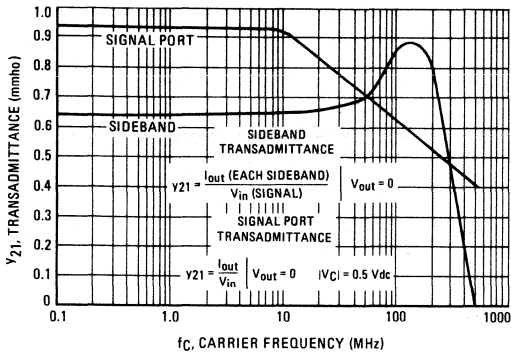


FIGURE 18 – CARRIER SUPPRESSION versus TEMPERATURE

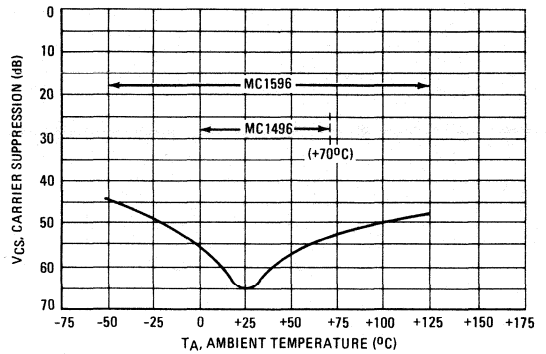


FIGURE 19 – SIGNAL-PORT FREQUENCY RESPONSE

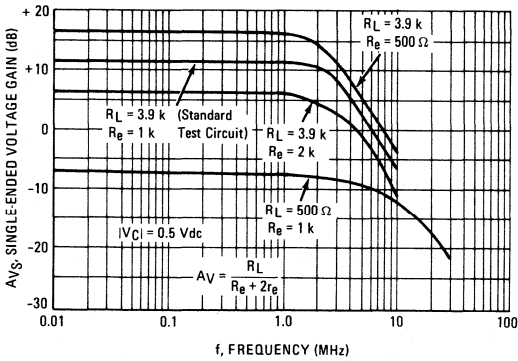


FIGURE 20 – CARRIER SUPPRESSION versus FREQUENCY

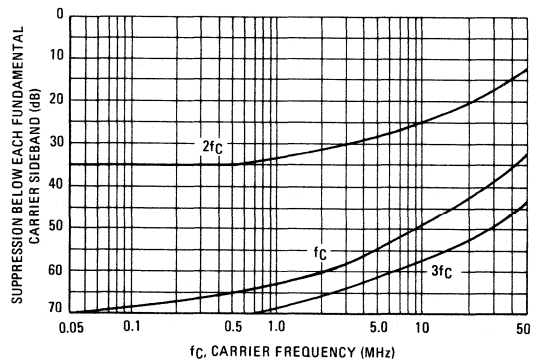


FIGURE 21 – CARRIER FEEDTHROUGH versus FREQUENCY

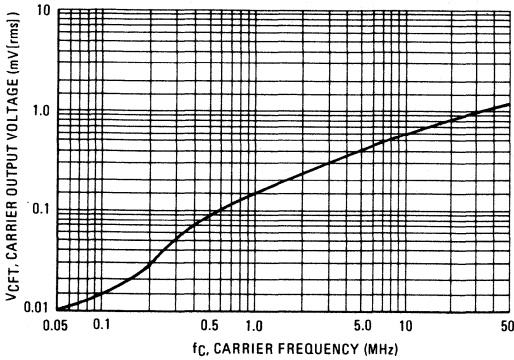
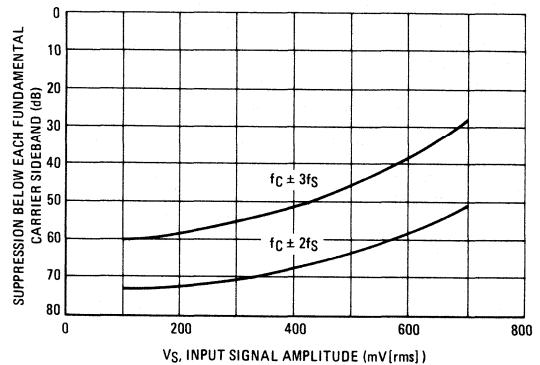


FIGURE 22 – SIDEBAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



TYPICAL CHARACTERISTICS (continued)

FIGURE 23 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

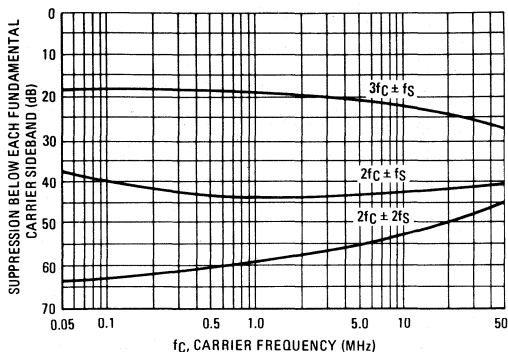
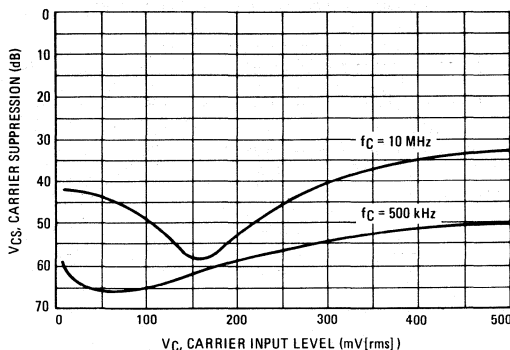


FIGURE 24 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 5.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I_E) (R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions:

- 1) Low-level dc
- 2) High-level dc
- 3) Low-level ac
- 4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

OPERATIONS INFORMATION (continued)

FIGURE 25 – TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES

| Carrier Input Signal (V _C) | Approximate Voltage Gain | Output Signal Frequency(s) |
|--|--|---|
| Low-level dc | $\frac{R_L V_C}{2(R_E + 2r_e) \left(\frac{KT}{q}\right)}$ | f _M |
| High-level dc | $\frac{R_L}{R_E + 2r_e}$ | f _M |
| Low-level ac | $\frac{R_L V_C(\text{rms})}{2\sqrt{2} \left(\frac{KT}{q}\right) (R_E + 2r_e)}$ | f _C ± f _M |
| High-level ac | $\frac{0.637 R_L}{R_E + 2r_e}$ | f _C ± f _M , 3f _C ± f _M , 5f _C ± f _M , . . . |

NOTES:

1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, f_C + f_M and f_C - f_M.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, At +25°C;

$$r_e \approx \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26 \text{ mV at room temperature}$$

APPLICATION INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on pins 7 and 8 should be increased to 1.0 μF. Also, the output filter at pin 9 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing

carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR
(+12 Vdc SINGLE SUPPLY)

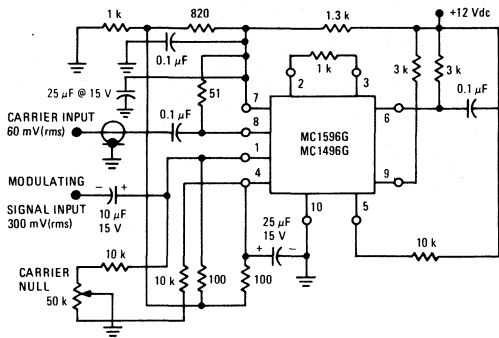


FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

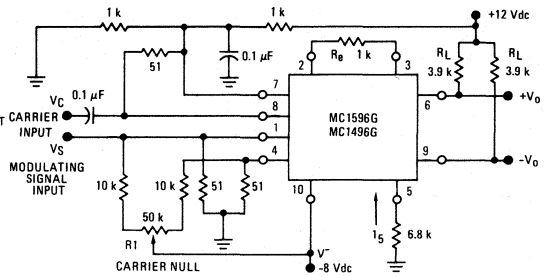


FIGURE 28 – AM MODULATOR CIRCUIT

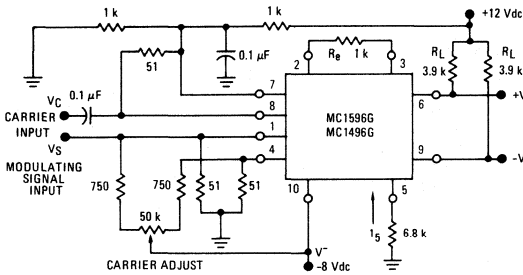


FIGURE 29 – PRODUCT DETECTOR
(+12 Vdc SINGLE SUPPLY)

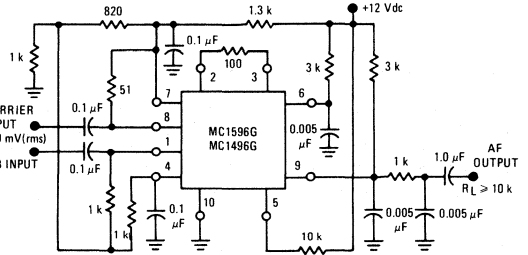


FIGURE 30 – DOUBLY BALANCED MIXER
(BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)

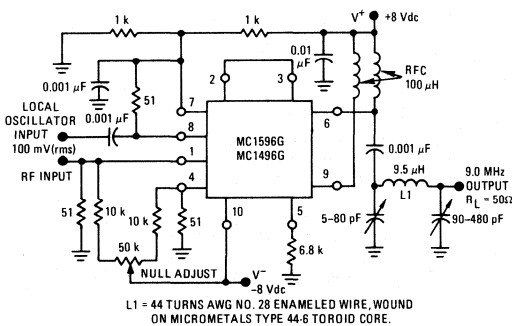
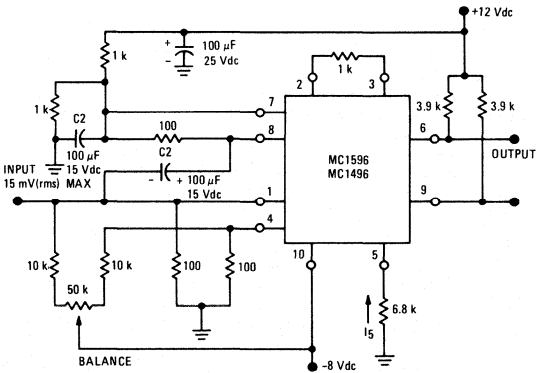


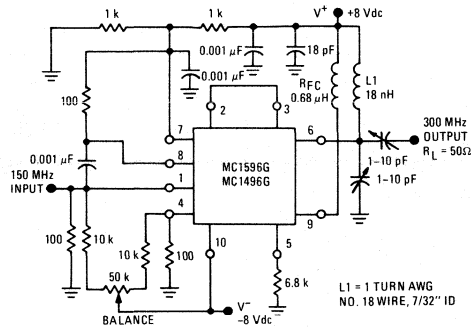
FIGURE 31 – LOW-FREQUENCY DOUBLER



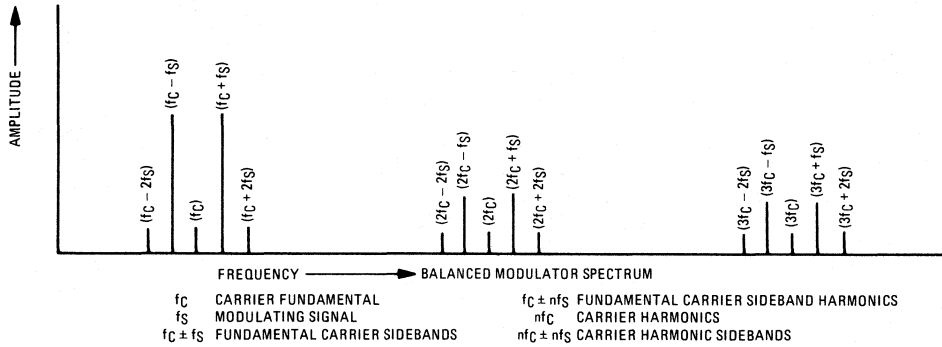
Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TYPICAL APPLICATIONS (continued)

FIGURE 32 – 150 to 300 MHz DOUBLER

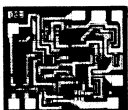


DEFINITIONS



MC1709 MC1709C

MONOLITHIC OPERATIONAL AMPLIFIER



... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics
 $A_{VOL} = 45,000$ typical
- Low Temperature Drift $- \pm 3.0 \mu V/^{\circ}C$
- Large Output Voltage Swing $- \pm 14 V$ typical @ $\pm 15 V$ Supply
- Low Output Impedance $- Z_{out} = 150$ ohms typical

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT MONOLITHIC SILICON

G SUFFIX
METAL PACKAGE
CASE 601
TO-99



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P2 SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116
(MC1709C only)



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1709C only)



PIN CONNECTIONS

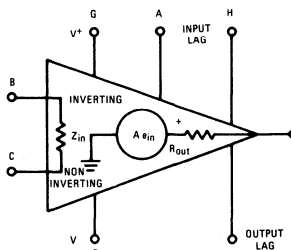
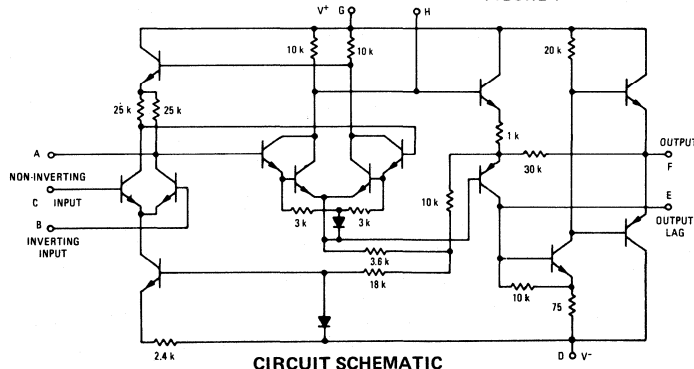
| Schematic | A | B | C | D | E | F | G | H |
|---------------------|---|---|---|---|---|----|----|----|
| "G" & "P1" Packages | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| "F" Package | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| "P2" & "L" Packages | 3 | 4 | 5 | 6 | 9 | 10 | 11 | 12 |

MAXIMUM RATINGS ($T_A = +25^{\circ}C$ unless otherwise noted)

| Rating | Symbol | Value | Unit | |
|--|-----------------------------------|-----------------------------------|-----------------|----------------------------|
| Power Supply Voltage | V^+ | +18 | Vdc | |
| | V^- | -18 | Vdc | |
| Differential Input Signal | V_{in} | ± 5.0 | Volts | |
| Common Mode Input Swing | CMV_{in} | $\pm V^+$ | Volts | |
| Load Current | I_L | 10 | mA | |
| Output Short Circuit Duration | t_S | 5.0 | s | |
| Power Dissipation (Package Limitation) | P_D | 680 | mW | |
| | | Derate above $T_A = +25^{\circ}C$ | 4.6 | mW/ $^{\circ}C$ |
| | | Flat Package | 500 | mW |
| | | Derate above $T_A = +25^{\circ}C$ | 3.3 | mW/ $^{\circ}C$ |
| | | Plastic Dual In-Line Packages | 625 | mW |
| | | Derate above $T_A = +25^{\circ}C$ | 5.0 | mW/ $^{\circ}C$ |
| Ceramic Dual In-Line Package | Derate above $T_A = +25^{\circ}C$ | 750 | mW | |
| | | 6.0 | mW/ $^{\circ}C$ | |
| Operating Temperature Range | MC1709 MC1709C | T_A | -55 to +125 | $^{\circ}C$ |
| | | | 0 to +75 | $^{\circ}C$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^{\circ}C$ | |
| | | | | Metal and Ceramic Packages |
| | | | | Plastic Packages |

7

FIGURE 1



MC1709, MC1709C (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

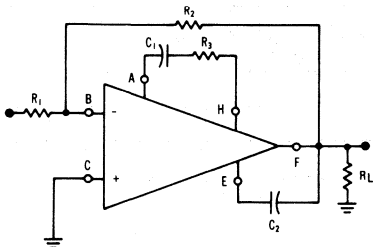
| Characteristic | Symbol | MC1709 | | | MC1709C | | | Unit | |
|--|----------------------------|----------------------|----------------------|------------|----------------------|----------------------|------------|------------------------------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Open Loop Voltage Gain ($R_L = 2.0$ k Ω) ($V_O = \pm 10$ V, $T_A = T_{low}$ to T_{high}) ^② | A_{VOL} | 25,000 | 45,000 | 70,000 | 15,000 | 45,000 | — | — | |
| Output Impedance ($f = 20$ Hz) | Z_{out} | — | 150 | — | — | 150 | — | Ω | |
| Input Impedance ($f = 20$ Hz) | Z_{in} | 150 | 400 | — | 50 | 250 | — | k Ω | |
| Output Voltage Swing ($R_L = 10$ k Ω) ($R_L = 2.0$ k Ω) | V_O | ± 12 ± 10 | ± 14 ± 13 | — | ± 12 ± 10 | ± 14 ± 13 | — | V_{peak} | |
| Input Common-Mode Voltage Swing | CMV_{in} | ± 8 | ± 10 | — | ± 8.0 | ± 10 | — | V_{peak} | |
| Common-Mode Rejection Ratio ($f = 20$ Hz) | CM_{rej} | 70 | 90 | — | 65 | 90 | — | dB | |
| Input Bias Current ($T_A = +25^\circ\text{C}$) ($T_A = T_{low}$) | I_b | — | 0.2 0.5 | 0.5 1.5 | — | 0.3 — | 1.5 2.0 | μA | |
| Input Offset Current ($T_A = +25^\circ\text{C}$) ($T_A = T_{low}$) ($T_A = T_{high}$) | $ I_{io} $ | — | 0.05 | 0.2 | — | 0.1 | 0.5 | μA | |
| Input Offset Voltage ($T_A = +25^\circ\text{C}$) ($T_A = T_{low}$ to T_{high}) | $ V_{io} $ | — | 1.0 | 5.0 | — | 2.0 | 7.5 | mV | |
| Step Response { Gain = 100, 5.0% overshoot, R ₁ = 1.0 k Ω , R ₂ = 100 k Ω , R ₃ = 1.5 k Ω , C ₁ = 100 pF, C ₂ = 3.0 pF | dV_{out}/dt ^① | t_f | — | 0.8 | — | — | 0.8 | — | μs |
| t_{pd} | | — | 0.38 | — | — | 0.38 | — | μs | |
| dV_{out}/dt | | — | 12 | — | — | 12 | — | V/ μs | |
| { Gain = 10, 10% overshoot, R ₁ = 1.0 k Ω , R ₂ = 10 k Ω , R ₃ = 1.5 k Ω , C ₁ = 500 pF, C ₂ = 20 pF | dV_{out}/dt ^① | t_f | — | 0.6 | — | — | 0.6 | — | μs |
| t_{pd} | | — | 0.34 | — | — | 0.34 | — | μs | |
| dV_{out}/dt | | — | 1.7 | — | — | 1.7 | — | V/ μs | |
| { Gain = 1, 5.0% overshoot, R ₁ = 10 k Ω , R ₂ = 10 k Ω , R ₃ = 1.5 k Ω , C ₁ = 5000 pF, C ₂ = 200 pF | dV_{out}/dt ^① | t_f | — | 2.2 | — | — | 2.2 | — | μs |
| t_{pd} | | — | 1.3 | — | — | 1.3 | — | μs | |
| dV_{out}/dt | | — | 0.25 | — | — | 0.25 | — | V/ μs | |
| Average Temperature Coefficient of Input Offset Voltage ($R_S = 50$ Ω , $T_A = T_{low}$ to T_{high}) ($R_S \leq 10$ k Ω , $T_A = T_{low}$ to T_{high}) | $ TC_{V_{io}} $ | — | 3.0 | — | — | 3.0 | — | $\mu\text{V}/^\circ\text{C}$ | |
| DC Power Dissipation (Power Supply = ± 15 V, $V_O = 0$) | P_D | — | 80 | 165 | — | 80 | 200 | mW | |
| Positive Supply Sensitivity (V^- constant) | S^+ | — | 25 | 150 | — | 25 | 200 | $\mu\text{V}/\text{V}$ | |
| Negative Supply Sensitivity (V^+ constant) | S^- | — | 25 | 150 | — | 25 | 200 | $\mu\text{V}/\text{V}$ | |

① dV_{out}/dt = Slew Rate

② $T_{high} = +75^\circ\text{C}$ for MC1709C, $T_{low} = 0^\circ\text{C}$ for MC1709C
 $+125^\circ\text{C}$ for MC1709, -55°C for MC1709

TYPICAL CHARACTERISTICS

FIGURE 2 – TEST CIRCUIT
 $V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$



| Fig. No. | Curve No. | Test Conditions | | | | |
|----------|-----------|-----------------------------|-----------------------------|-----------------------------|---------------------|---------------------|
| | | R ₁ (Ω) | R ₂ (Ω) | R ₃ (Ω) | C ₁ (pF) | C ₂ (pF) |
| 3 | 1 | 10 k | 10 k | 1.5 k | 5.0 k | 200 |
| | 2 | 10 k | 100 k | 1.5 k | 500 | 20 |
| | 3 | 10 k | 1.0 M | 1.5 k | 100 | 3.0 |
| | 4 | 1.0 k | 1.0 M | 0 | 10 | 3.0 |
| 4 | 1 | 1.0 k | 1.0 M | 0 | 10 | 3.0 |
| | 2 | 10 k | 1.0 M | 1.5 k | 100 | 3.0 |
| | 3 | 10 k | 100 k | 1.5 k | 500 | 20 |
| | 4 | 10 k | 10 k | 1.5 k | 5.0 k | 200 |
| 5 | 1 | 0 | ∞ | 1.5 k | 5.0 k | 200 |
| | 2 | 0 | ∞ | 1.5 k | 500 | 20 |
| | 3 | 0 | ∞ | 1.5 k | 100 | 3.0 |
| | 4 | 0 | ∞ | 0 | 10 | 3.0 |

TYPICAL CHARACTERISTICS (continued)
 ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 3 – LARGE SIGNAL SWING
 versus FREQUENCY

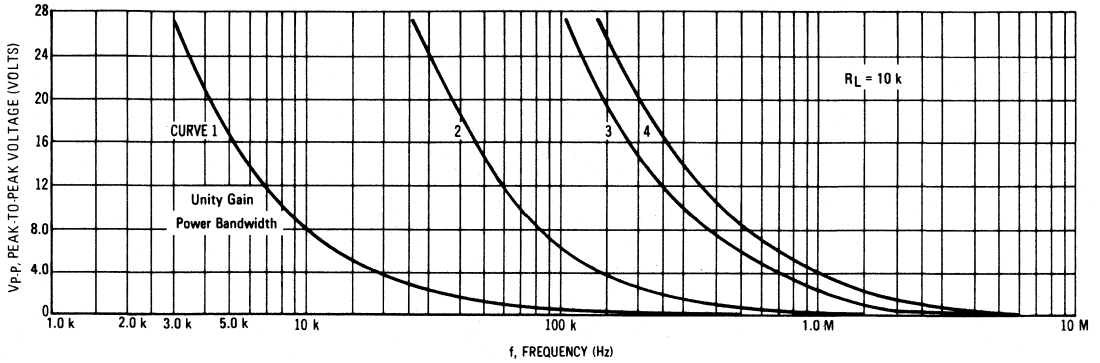


FIGURE 4 – VOLTAGE GAIN
 versus FREQUENCY

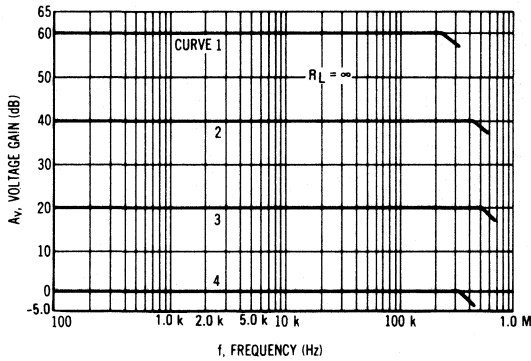


FIGURE 5 – OPEN LOOP
 VOLTAGE GAIN versus FREQUENCY

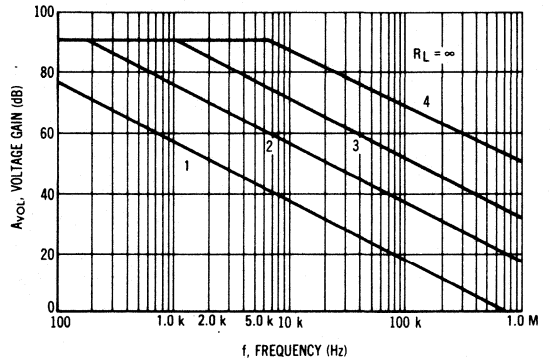


FIGURE 6 – VOLTAGE GAIN
 versus POWER SUPPLY VOLTAGE

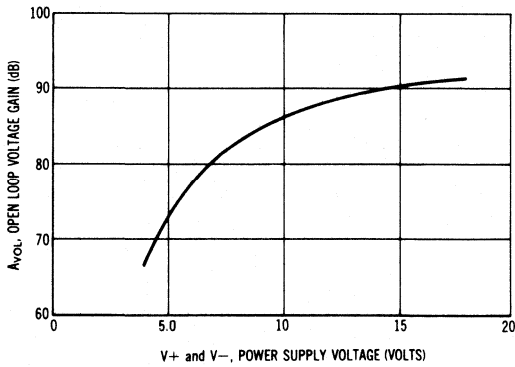
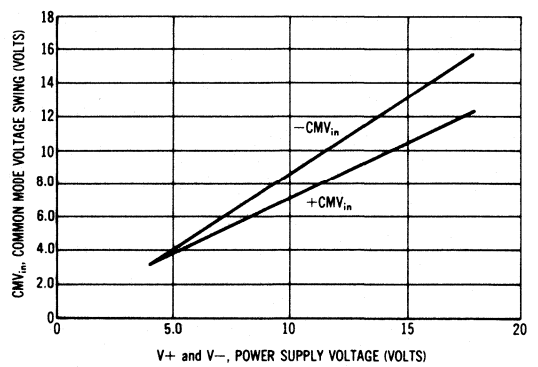


FIGURE 7 – COMMON SWING
 versus POWER SUPPLY VOLTAGE



MC1709, MC1709C (continued)

TYPICAL CHARACTERISTICS (continued)

($V^+ = +15 \text{ Vdc}$, $V^- = -15 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

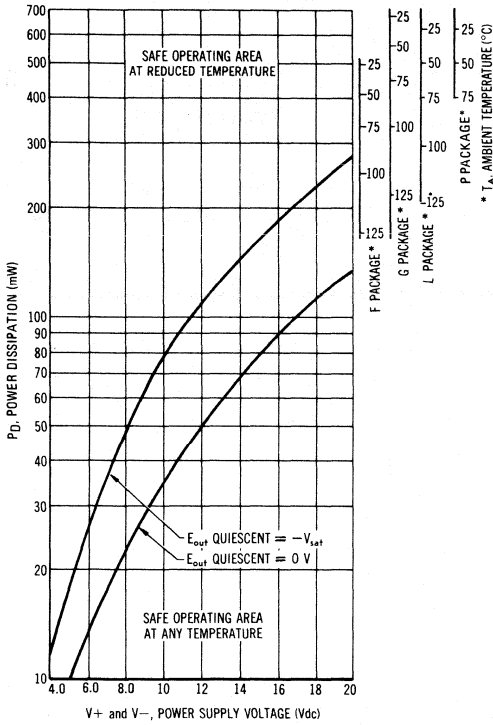


FIGURE 9 – INPUT OFFSET VOLTAGE versus TEMPERATURE

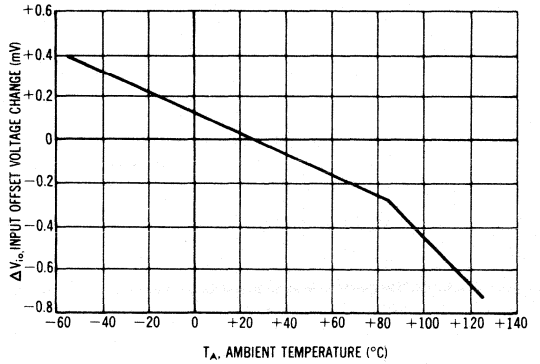
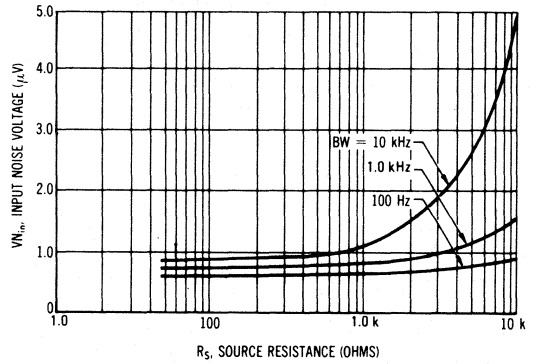


FIGURE 10 – INPUT NOISE VOLTAGE versus SOURCE RESISTANCE



See current MCC1709/1709C data sheet for standard linear chip information.
 See current MCBC1709/MCB1709F data sheet for Beam-Lead device information.
 See current MCCF1709, 1709C data sheet for flip-chip information.

MC1710

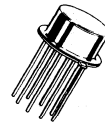
DIFFERENTIAL COMPARATOR

MONOLITHIC DIFFERENTIAL VOLTAGE COMPARATOR

... designed for use in level detection, low-level sensing, and memory applications.

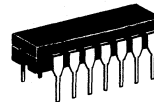
- Differential Input Characteristics –
Input Offset Voltage = 1.0 mV
Offset Voltage Drift = 3.0 $\mu\text{V}/^\circ\text{C}$
- Fast Response Time – 40 ns
- Output Compatible With All Saturating Logic Forms –
 $V_O = +3.2\text{ V to } -0.5\text{ V}$ typical
- Low Output Impedance – 200 ohms

DIFFERENTIAL COMPARATOR INTEGRATED CIRCUIT MONOLITHIC SILICON EPITAXIAL PASSIVATED



G SUFFIX
METAL PACKAGE
CASE 601
TO-99
Lead 4 connected to case

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

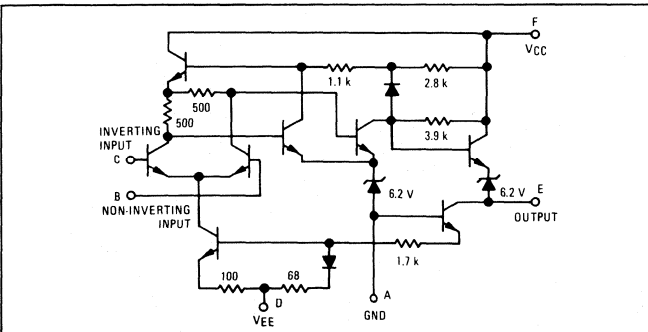
| Rating | Symbol* | Value | Unit | |
|---|--------------|--|------------------|----------------------|
| Power Supply Voltage | V_{CC} max | +14 | Vdc | |
| | V_{EE} max | -7.0 | Vdc | |
| Differential Input Signal Voltage | V_{ID} | ± 5.0 | Volts | |
| Common Mode Input Swing Voltage | V_{ICR} | ± 7.0 | Volts | |
| Peak Load Current | I_L | 10 | mA | |
| Power Dissipation (package limitations) | P_D | Metal Package | 680 | mW |
| | | Derate above $T_A = +25^\circ\text{C}$ | 4.6 | mW/ $^\circ\text{C}$ |
| | | Flat Package | 500 | mW |
| | | Derate above $T_A = +25^\circ\text{C}$ | 3.3 | mW/ $^\circ\text{C}$ |
| | | Ceramic Dual In-Line Package | 625 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | 5.0 | mW/ $^\circ\text{C}$ | | |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ | |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ | |

*Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

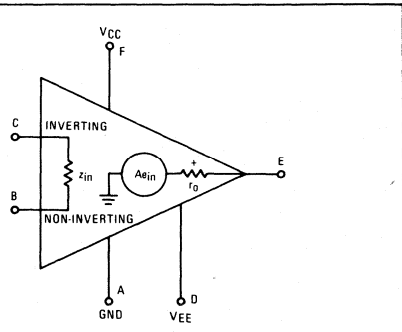
PIN CONNECTIONS

| Schematic | A | B | C | D | E | F |
|-------------|---|---|---|---|---|----|
| "G" Package | 1 | 2 | 3 | 4 | 7 | 8 |
| "F" Package | 1 | 2 | 3 | 5 | 6 | 8 |
| "L" Package | 2 | 3 | 4 | 6 | 9 | 11 |

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT

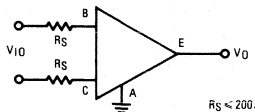
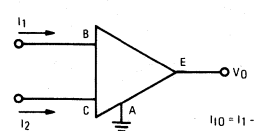
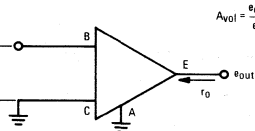
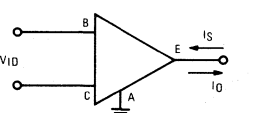
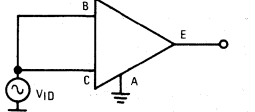
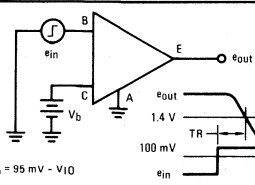
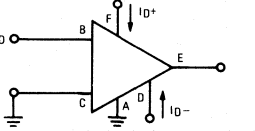


See Packaging Information Section for outline dimensions.

See current MCC1710/1710C data sheet for standard linear chip information.

See current MCBC1710/MCB1710F for beam-lead device information

ELECTRICAL CHARACTERISTICS ($V_{CC} = +12$ Vdc, $V_{EE} = -6$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic Definitions (linear operation) | Characteristic | Symbol* | Min | Typ | Max | Unit |
|--|--|--------------------------|-----------------|---------------|-------------------|------------------------------|
|  <p>$R_S \leq 200\Omega$</p> | Input Offset Voltage $V_O = 1.4$ Vdc, $T_A = +25^\circ\text{C}$ $V_O = 1.8$ Vdc, $T_A = -55^\circ\text{C}$ $V_O = 1.0$ Vdc, $T_A = +125^\circ\text{C}$ | V_{IO} | — — — | 1.0 — — | 2.0 3.0 3.0 | mVdc |
| | Temperature Coefficient of Input Offset Voltage | $\Delta V_{IO}/\Delta T$ | — | 3.0 | — | $\mu\text{V}/^\circ\text{C}$ |
|  <p>$I_{IO} = I_1 - I_2$ $I_{IB} = \frac{I_1 + I_2}{2}$</p> | Input Offset Current $V_O = 1.4$ Vdc, $T_A = +25^\circ\text{C}$ $V_O = 1.8$ Vdc, $T_A = -55^\circ\text{C}$ $V_O = 1.0$ Vdc, $T_A = +125^\circ\text{C}$ | I_{IO} | — — — | 1.0 — — | 3.0 7.0 3.0 | μA dc |
| | Input Bias Current $V_O = 1.4$ Vdc, $T_A = +25^\circ\text{C}$ $V_O = 1.8$ Vdc, $T_A = -55^\circ\text{C}$ $V_O = 1.0$ Vdc, $T_A = +125^\circ\text{C}$ | I_{IB} | — — — | 12 — — | 20 45 20 | μA dc |
|  <p>$A_{VOL} = \frac{e_{out}}{e_{in}}$</p> | Open Loop Voltage Gain $T_A = +25^\circ\text{C}$ $T_A = -55$ to $+125^\circ\text{C}$ | A_{VOL} | 1250 1000 | 1700 — | — — | V/V |
| | Output Resistance | r_o | — | 200 | — | ohms |
|  | Differential Voltage Range | V_{ID} | ± 5.0 | — | — | Vdc |
| | Positive Output Voltage $V_{ID} \geq 5.0$ mV, $0 \leq I_O \leq 5.0$ mA | V_{OH} | 2.5 | 3.2 | 4.0 | Vdc |
| | Negative Output Voltage $V_{ID} \geq -5.0$ mV | V_{OL} | -1.0 | -0.5 | 0 | Vdc |
| | Output Sink Current $V_{ID} \geq -5.0$ mV, $V_O \leq 0$, $T_A = +25^\circ\text{C}$ $V_{ID} \geq -5.0$ mV, $V_O \geq 0$, $T_A = -55^\circ\text{C}$ | I_{OS} | — 2.0 1.0 | 2.5 2.0 | — — | mAdc |
|  | Input Common-Mode Voltage Range | V_{ICR} | ± 5.0 | — | — | Volts |
| | Common-Mode Rejection Ratio $V_{EE} = -7.0$ Vdc, $R_S \leq 200\Omega$ | CMRR | 80 | 100 | — | dB |
|  <p>$V_b = 95$ mV - V_{IO}</p> | Propagation Delay Time For Positive and Negative Going Input Pulse | t_p | — | 40 | — | ns |
|  | Power Supply Current $V_O \leq 0$ Vdc | I_{D+} I_{D-} | — — | 6.4 5.5 | 9.0 7.0 | mAdc |
| | Power Consumption | | — | 115 | 150 | mW |

*Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

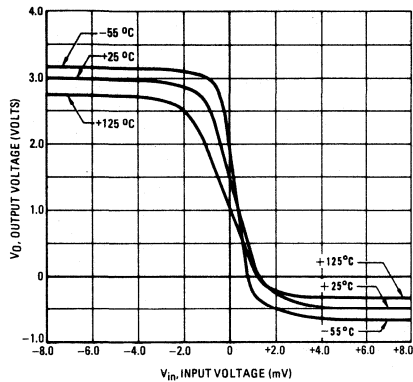


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

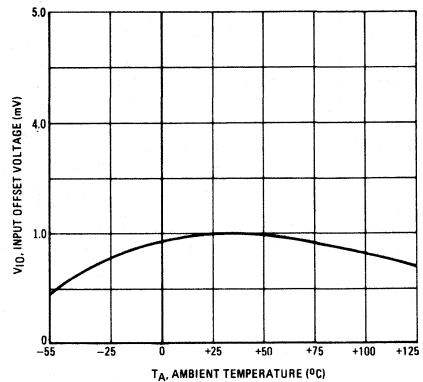


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

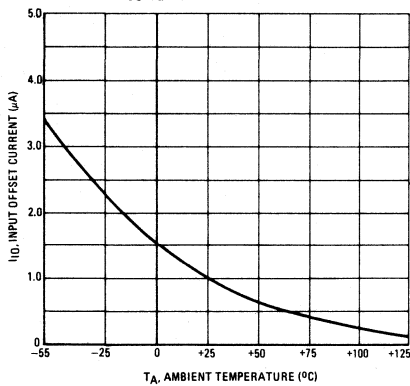


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE

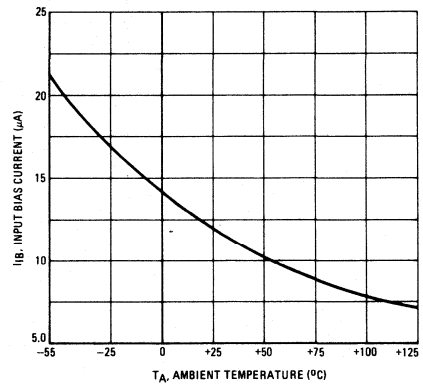


FIGURE 5 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

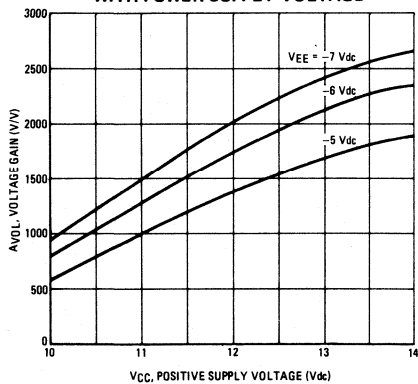
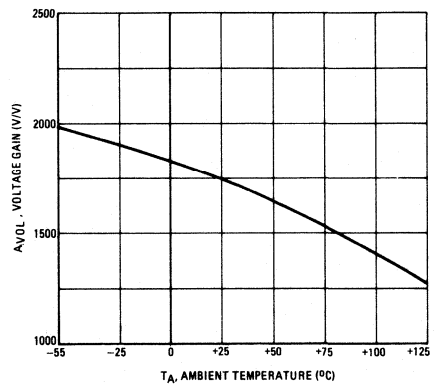


FIGURE 6 – VOLTAGE GAIN versus TEMPERATURE



7

TYPICAL CHARACTERISTICS (Continued)

FIGURE 7 - RESPONSE TIME

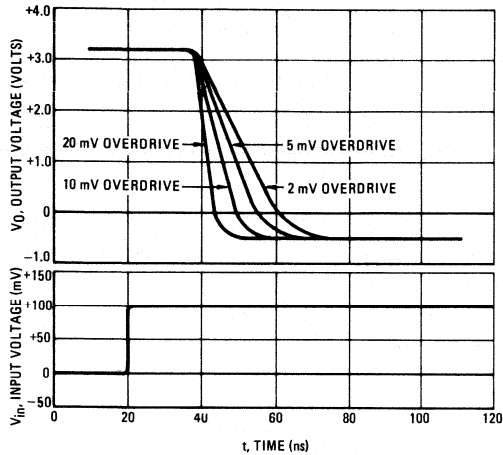


FIGURE 8 - POWER DISSIPATION versus TEMPERATURE

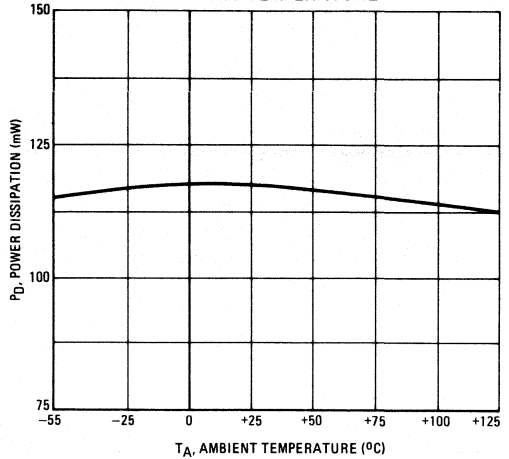


FIGURE 9 - RECOMMENDED SERIES RESISTANCE versus MRTL* LOADS

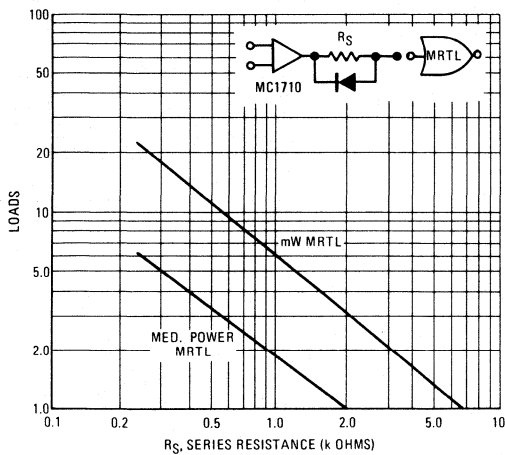
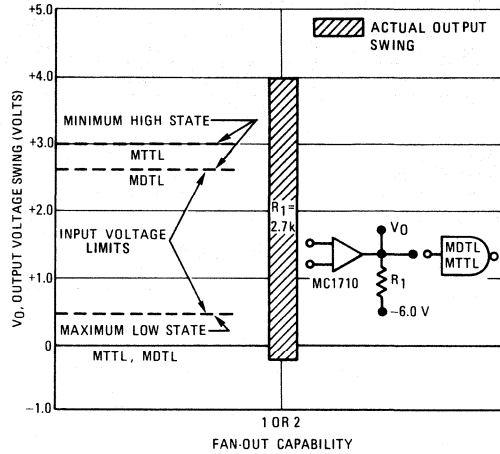


FIGURE 10 - FAN-OUT CAPABILITY WITH MDTL* OR MTTL* OUTPUT SWING



MC1710C

DIFFERENTIAL COMPARATOR

MONOLITHIC DIFFERENTIAL VOLTAGE COMPARATOR

... designed for use in level detection, low-level sensing, and memory applications.

- Differential Input Characteristics –
Input Offset Voltage = 1.5 mV
Offset Voltage Drift = 5.0 $\mu\text{V}/^\circ\text{C}$
- Fast Response Time – 40 ns
- Output Compatible With All Saturating Logic Forms –
 $V_O = +3.2\text{ V to } -0.5\text{ V typical}$
- Low Output Impedance – 200 ohms

DIFFERENTIAL COMPARATOR

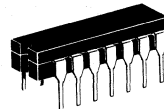
MONOLITHIC SILICON EPITAXIAL PASSIVATED



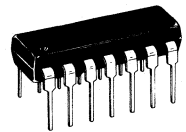
G SUFFIX
METAL PACKAGE
CASE 601-2
TO-99



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|----------------------|-------------|----------------------|
| Power Supply Voltage | V_{CC} V_{EE} | +14 -7.0 | Vdc Vdc |
| Differential-Mode Input Signal Voltage | V_{ID} | ± 5.0 | Volts |
| Common-Mode Input Swing | V_{ICR} | ± 7.0 | Volts |
| Peak Load Current | I_L | 10 | mA |
| Power Dissipation (package limitations) | P_D | | |
| Metal Package | | 680 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 4.6 | mW/ $^\circ\text{C}$ |
| Flat Package | | 500 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 3.3 | mW/ $^\circ\text{C}$ |
| Ceramic and Plastic Dual In-Line Packages | | 625 | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 5.0 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range* | T_A | 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

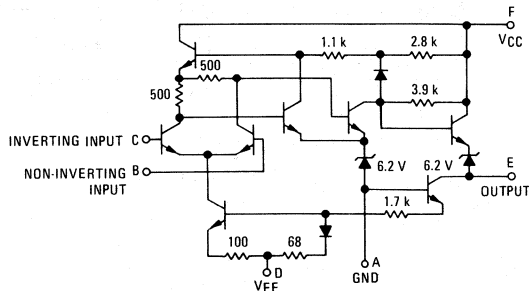
PIN CONNECTIONS

| Schematic | A | B | C | D | E | F |
|----------------------|---|---|---|---|---|----|
| "G" Package | 1 | 2 | 3 | 4 | 7 | 8 |
| "F" Package | 1 | 2 | 3 | 5 | 6 | 8 |
| "L" and "P" Packages | 2 | 3 | 4 | 6 | 9 | 11 |

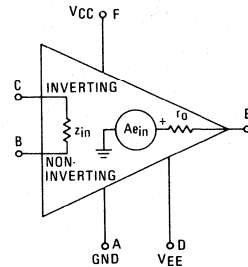
* For full temperature range (-55 $^\circ\text{C}$ to +125 $^\circ\text{C}$) and characteristic curves, see MC1710 data sheet.

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

See current MCC1710/1710C data sheet for standard linear chip information.

MC1710C (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = +12$ Vdc, $V_{EE} = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic Definitions | Characteristic | Symbol | Min | Typ | Max | Unit |
|---|--|--------------------------|-----------|------|-----|------------------------------|
| <p>$R_S \leq 200 \Omega$</p> | Input Offset Voltage $V_O = 1.4$ Vdc, $T_A = +25^\circ\text{C}$ $V_O = 1.5$ Vdc, $T_A = 0^\circ\text{C}$ $V_O = 1.2$ Vdc, $T_A = +70^\circ\text{C}$ | V_{IO} | — | 1.5 | 5.0 | mVdc |
| | Temperature Coefficient of Input Offset Voltage | $\Delta V_{IO}/\Delta T$ | — | 5.0 | — | $\mu\text{V}/^\circ\text{C}$ |
| <p>$I_{IO} = I_1 - I_2$ $I_{IB} = \frac{I_1 + I_2}{2}$</p> | Input Offset Current $V_O = 1.4$ Vdc, $T_A = +25^\circ\text{C}$ $V_O = 1.5$ Vdc, $T_A = 0^\circ\text{C}$ $V_O = 1.2$ Vdc, $T_A = +70^\circ\text{C}$ | I_{IO} | — | 1.0 | 5.0 | μA dc |
| | Input Bias Current $V_O = 1.4$ Vdc, $T_A = +25^\circ\text{C}$ $V_O = 1.5$ Vdc, $T_A = 0^\circ\text{C}$ $V_O = 1.2$ Vdc, $T_A = +70^\circ\text{C}$ | I_{IB} | — | 15 | 25 | 40 |
| <p>$A_{vol} = \frac{e_{out}}{e_{in}}$</p> | Voltage Gain $T_A = +25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$ | A_{vol} | 1000 | 1500 | — | V/V |
| | Output Resistance | r_o | — | 200 | — | ohms |
| | Differential-Mode Voltage Range | V_{IDR} | ± 5.0 | — | — | Vdc |
| | Positive Output Voltage $V_{in} \geq 5.0$ mV, $0 \leq I_O \leq 5.0$ mA | V_{OH} | 2.5 | 3.2 | 4.0 | Vdc |
| | Negative Output Voltage $V_{in} \geq -5.0$ mV | V_{OL} | -1.0 | -0.5 | 0 | Vdc |
| | Output Sink Current $V_{in} \geq 5.0$ mV, $V_O \geq 0$ $T_A = +25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ | I_s | 1.6 | 2.5 | — | mA |
| <p>$R_S \leq 200 \Omega$</p> | Input Common-Mode Range $V_{EE} = -7.0$ Vdc | V_{ICR} | ± 5.0 | — | — | Volts |
| | Common-Mode Rejection Ratio | CMRR | 70 | 100 | — | dB |
| <p>$V_B = 95$ mV-V_{IO}</p> | Propagation Delay Time For Positive and Negative Going Input Pulse | $t_{PHL/LH}$ | — | 40 | — | ns |
| | Power Supply Current $V_O \leq 0$ Vdc | I_{CC} I_{EE} | — | 6.4 | 9.0 | mA |
| | Power Consumption | | — | 110 | 150 | mW |

MC1711

DIFFERENTIAL COMPARATORS

MONOLITHIC DUAL DIFFERENTIAL VOLTAGE COMPARATOR

... designed for use in level detection, low-level sensing, and memory applications.

Typical Characteristics:

- Differential Input –
Input Offset Voltage = 1.0 mV
Offset Voltage Drift = 5.0 $\mu\text{V}/^\circ\text{C}$
- Fast Response Time – 40 ns
- Output Compatible with All Saturating Logic Forms –
 $V_{\text{out}} = +4.5 \text{ V}$ to -0.5 V Typical
- Low Output Impedance – 200 Ohms

DUAL DIFFERENTIAL COMPARATOR INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit | |
|--|--------------------------|---------------------------------------|------------------|----------------------------|
| Power Supply Voltage | V^+ | +14 | Vdc | |
| | V^- | -7.0 | Vdc | |
| Differential Input Signal | V_{in} | ± 5.0 | Volts | |
| Common Mode Input Swing | CMV_{in} | ± 7.0 | Volts | |
| Peak Load Current | I_L | 50 | mA | |
| Power Dissipation (package limitation) | P_D | 680 | mW | |
| | | Derate above $T_A = 25^\circ\text{C}$ | 4.6 | $\text{mW}/^\circ\text{C}$ |
| | | Ceramic Dual In-line Package | 670 | mW |
| Derate above $T_A = 75^\circ\text{C}$ | 6.7 | $\text{mW}/^\circ\text{C}$ | | |
| Flat Package | | 500 | mW | |
| | | Derate above $T_A = 25^\circ\text{C}$ | 3.3 | $\text{mW}/^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ | |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ | |

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

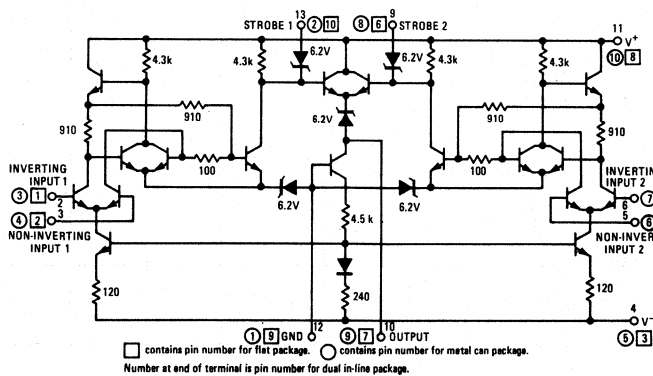


G SUFFIX
METAL PACKAGE
CASE 603-02
TO-100

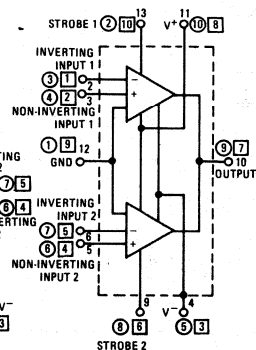
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



CIRCUIT SCHEMATIC



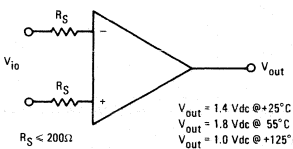
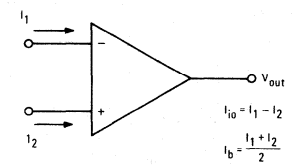
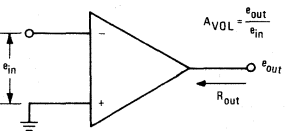
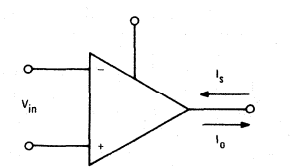
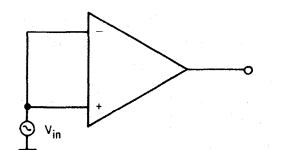
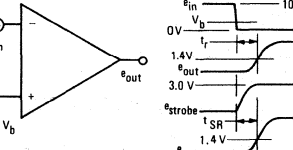
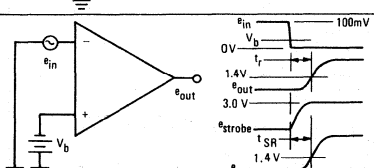
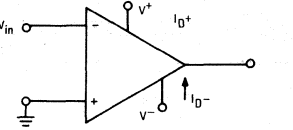
EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.
See current MCC1711/1711C data sheet for standard linear chip information.

MC1711 (continued)

ELECTRICAL CHARACTERISTICS (each comparator) $V^+ = +12$ Vdc, $V^- = -6.0$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic Definitions | Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|----------------------|-----------|------|-----|------------------------------|
|  <p> $V_{out} = 1.4$ Vdc @ $+25^\circ\text{C}$ $V_{out} = 1.8$ Vdc @ 55°C $V_{out} = 1.0$ Vdc @ $+125^\circ\text{C}$ $R_S < 200\Omega$ </p> | Input Offset Voltage $CMV_{in} = 0$ Vdc, $T_A = +25^\circ\text{C}$ $T_A = +25^\circ\text{C}$ $CMV_{in} = 0$ Vdc, $T_A = -55$ to $+125^\circ\text{C}$ $T_A = -55$ to $+125^\circ\text{C}$ | V_{io} | - | 1.0 | 3.5 | mVdc |
| | Temperature Coefficient of Input Offset Voltage | $TC_{V_{io}}$ | - | 5.0 | - | $\mu\text{V}/^\circ\text{C}$ |
|  <p> $I_{io} = I_1 - I_2$ $I_b = \frac{I_1 + I_2}{2}$ </p> | Input Offset Current $V_{out} = 1.4$ Vdc, $T_A = +25^\circ\text{C}$ $V_{out} = 1.8$ Vdc, $T_A = -55^\circ\text{C}$ $V_{out} = 1.0$ Vdc, $T_A = +125^\circ\text{C}$ | I_{io} | - | 0.5 | 10 | μA dc |
| | Input Bias Current $V_{out} = 1.4$ Vdc, $T_A = +25^\circ\text{C}$ $V_{out} = 1.8$ Vdc, $T_A = -55^\circ\text{C}$ $V_{out} = 1.0$ Vdc, $T_A = +125^\circ\text{C}$ | I_b | - | 25 | 75 | μA dc |
|  <p> $A_{VOL} = \frac{e_{out}}{e_{in}}$ </p> | Voltage Gain $T_A = +25^\circ\text{C}$ $T_A = -55$ to $+125^\circ\text{C}$ | A_{VOL} | 750 | 1500 | - | V/V |
| | Output Resistance | R_{out} | - | 200 | - | ohms |
|  | Differential Voltage Range | V_{in} | ± 5.0 | - | - | Vdc |
| | Positive Output Voltage $V_{in} \geq 10$ mVdc, $0 \leq I_o \leq 5.0$ mA | V_{OH} | 2.5 | 3.2 | 5.0 | Vdc |
| | Negative Output Voltage $V_{in} \leq -10$ mVdc | V_{OL} | -1.0 | -0.5 | 0 | Vdc |
| | Strobed Output Level $V_{strobe} \leq 0.3$ Vdc | $V_{OL(st)}$ | -1.0 | - | 0 | Vdc |
| | Output Sink Current $V_{in} \geq -10$ mV, $V_{out} \geq 0$ | I_S | 0.5 | 0.8 | - | mAdc |
|  | Strobe Current $V_{strobe} = 100$ mVdc | I_{st} | - | 1.2 | 2.5 | mAdc |
|  | Input Common Mode Range $V^- = -7.0$ Vdc | CM_{Vin} | ± 5.0 | - | - | Volts |
|  | Response Time $V_b = 5.0$ mV + V_{io} | t_R | - | 40 | - | ns |
| | Strobe Release Time | t_{SR} | - | 12 | - | ns |
|  | Power Supply Current $V_{out} \leq 0$ Vdc | I_{D+} I_{D-} | - | 8.6 | - | mAdc |
| | Power Consumption | | - | 130 | 200 | mW |

TYPICAL CHARACTERISTICS

FIGURE 1 - VOLTAGE TRANSFER CHARACTERISTICS

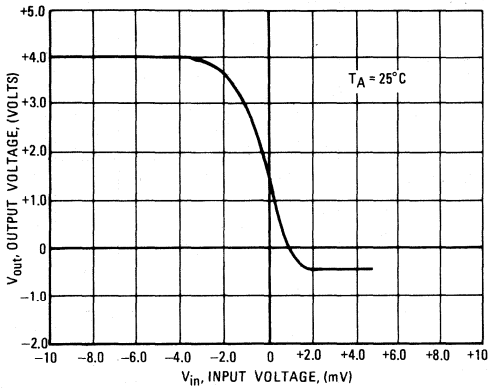


FIGURE 2 - INPUT BIAS CURRENT versus TEMPERATURE

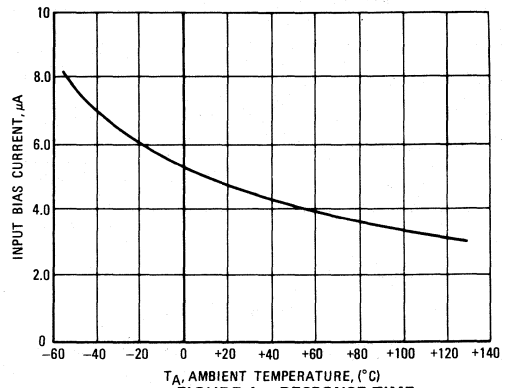


FIGURE 3 - VOLTAGE GAIN versus TEMPERATURE

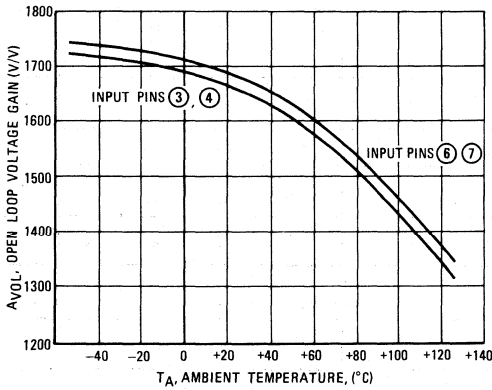


FIGURE 4 - RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

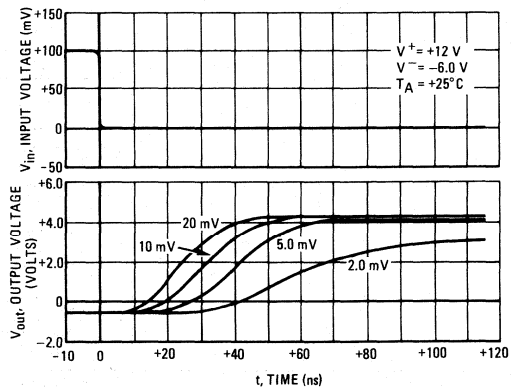


FIGURE 5 - VOLTAGE GAIN VARIATION WITH POWER SUPPLY VOLTAGE

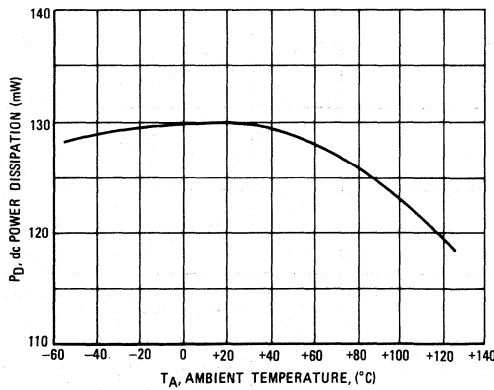
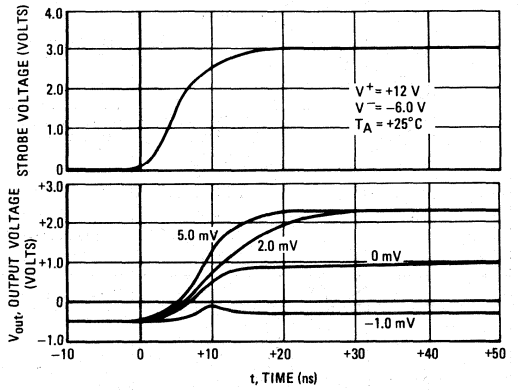


FIGURE 6 - STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



7

FIGURE 7 – COMMON MODE PULSE RESPONSE

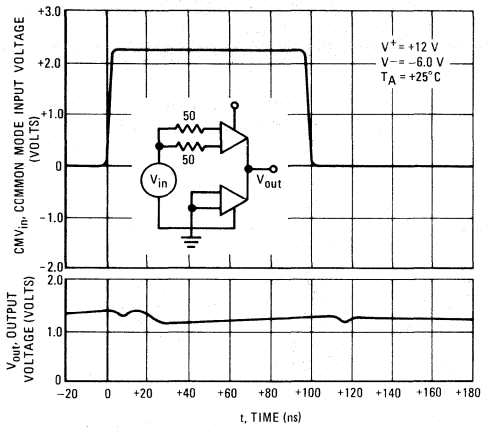


FIGURE 8 – OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

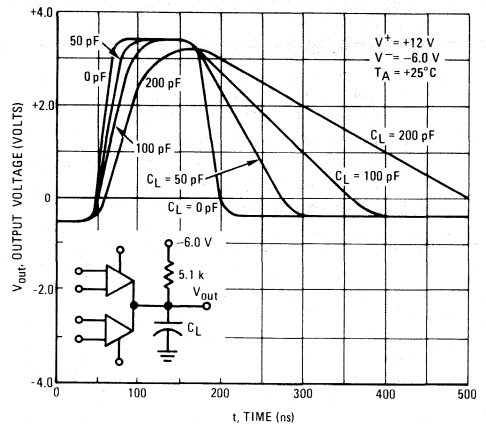


FIGURE 9 – SERIES RESISTANCE versus MRTL FAN-OUTS

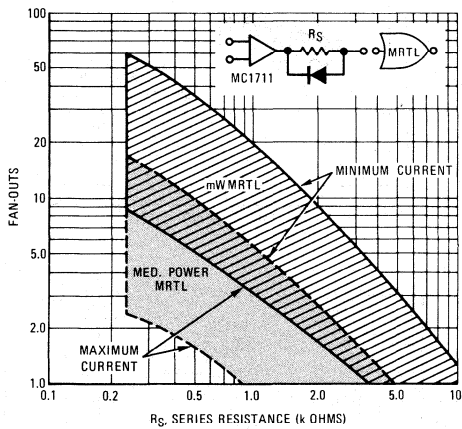
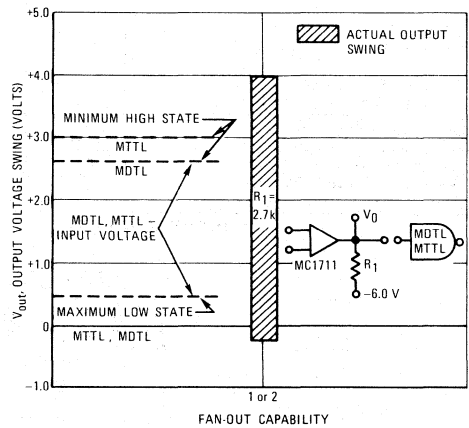


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



MC1711C

DIFFERENTIAL COMPARATORS

MONOLITHIC DUAL DIFFERENTIAL VOLTAGE COMPARATOR

... designed for use in level detection, low-level sensing, and memory applications.

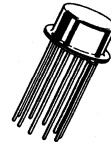
Typical Characteristics:

- Differential Input
Input Offset Voltage = 1.0 mV
Offset Voltage Drift = 5.0 $\mu\text{V}/^\circ\text{C}$
- Fast Response Time – 40 ns
- Output Compatible with All Saturating Logic Forms
 $V_{\text{out}} = +4.5 \text{ V}$ to -0.5 V typical
- Low Output Impedance – 200 ohms

DUAL DIFFERENTIAL COMPARATOR INTEGRATED CIRCUIT MONOLITHIC SILICON EPITAXIAL PASSIVATED

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|-------------------|---------------------------------------|------------------|
| Power Supply Voltage | V^+ | +14 | Vdc |
| | V^- | -7.0 | Vdc |
| Differential Input Signal | V_{in} | ± 5.0 | Volts |
| Common Mode Input Swing | CMV_{in} | ± 7.0 | Volts |
| Peak Load Current | I_L | 50 | mA |
| Power Dissipation (package limitation) | P_D | 680 | mW |
| | | Derate above $T_A = 25^\circ\text{C}$ | 4.6 |
| Flat Package | | 500 | mW |
| | | Derate above $T_A = 25^\circ\text{C}$ | 3.3 |
| Ceramic Dual In-Line Package | | 625 | mW |
| | | Derate above $T_A = 25^\circ\text{C}$ | 5.0 |
| Operating Temperature Range | T_A | 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |



G SUFFIX
METAL PACKAGE
CASE 603-02
TO-100

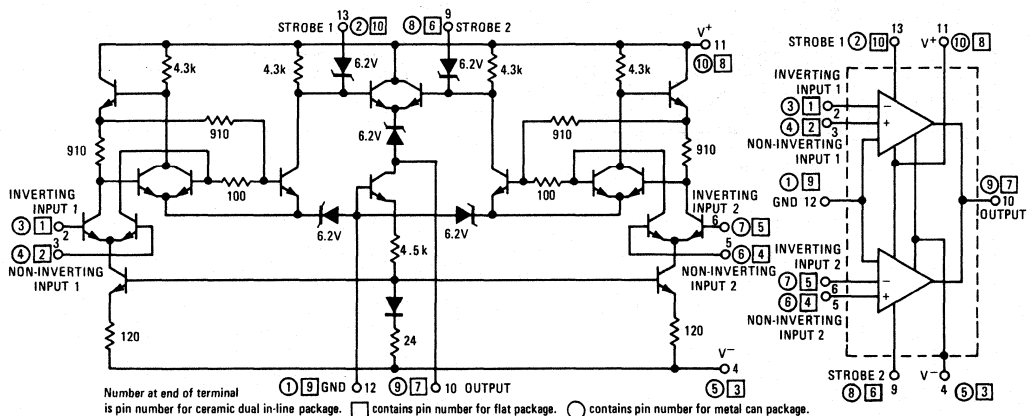
F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

CIRCUIT SCHEMATIC

EQUIVALENT CIRCUIT

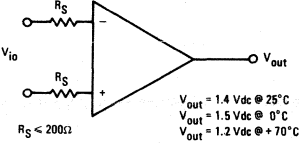
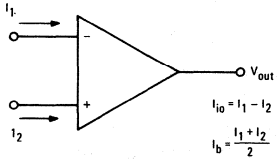
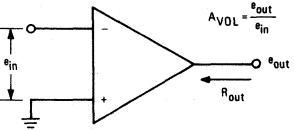
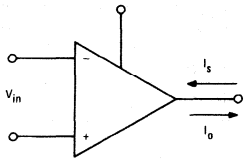
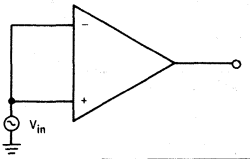
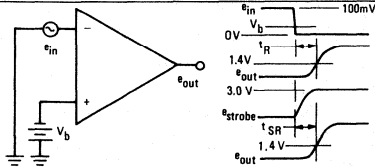
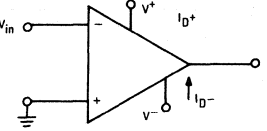


See Packaging Information Section for outline dimensions.

See current MCC1711/1711C data sheet for standard linear chip information.

MC1711C (continued)

ELECTRICAL CHARACTERISTICS (each comparator) $V^+ = +12$ Vdc, $V^- = -6.0$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic Definitions | Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|--------------|-----------|------|-----|------------------------------|
|  <p> V_{io} $R_S < 200\Omega$ $V_{out} = 1.4$ Vdc @ 25°C $V_{out} = 1.5$ Vdc @ 0°C $V_{out} = 1.2$ Vdc @ $+70^\circ\text{C}$ </p> | Input Offset Voltage $CMV_{in} = 0$ Vdc, $T_A = +25^\circ\text{C}$ $CMV_{in} \neq 0$ Vdc, $T_A = +25^\circ\text{C}$ $CMV_{in} = 0$ Vdc, $T_A = 0$ to $+70^\circ\text{C}$ $CMV_{in} \neq 0$ Vdc, $T_A = 0$ to $+70^\circ\text{C}$ | V_{io} | - | 1.0 | 5.0 | mVdc |
| | Temperature Coefficient of Input Offset Voltage | TC_{Vio} | - | 5.0 | - | $\mu\text{V}/^\circ\text{C}$ |
|  <p> I_{io} $I_{io} = I_1 - I_2$ $I_b = \frac{I_1 + I_2}{2}$ </p> | Input Offset Current $V_{out} = 1.4$ Vdc, $T_A = +25^\circ\text{C}$ $V_{out} = 1.5$ Vdc, $T_A = 0^\circ\text{C}$ $V_{out} = 1.2$ Vdc, $T_A = +70^\circ\text{C}$ | I_{io} | - | 0.5 | 15 | μA dc |
| | Input Bias Current $V_{out} = 1.4$ Vdc, $T_A = +25^\circ\text{C}$ $V_{out} = 1.5$ Vdc, $T_A = 0^\circ\text{C}$ $V_{out} = 1.2$ Vdc, $T_A = +70^\circ\text{C}$ | I_b | - | 25 | 100 | μA dc |
|  <p> $A_{VOL} = \frac{e_{out}}{e_{in}}$ R_{out} </p> | Voltage Gain $T_A = +25^\circ\text{C}$ $T_A = -55$ to $+125^\circ\text{C}$ | A_{VOL} | 700 | 1500 | - | V/V |
| | Output Resistance | R_{out} | - | 200 | - | ohms |
|  <p> V_{in} I_s I_o </p> | Differential Voltage Range Positive Output Voltage $V_{in} \geq 10$ mVdc, $0 \leq I_o \leq 5.0$ mA Negative Output Voltage $V_{in} \geq -10$ mVdc | V_{in} | ± 5.0 | - | - | Vdc |
| | Strobed Output Level $V_{strobe} \leq 0.3$ Vdc | $V_{OL(st)}$ | -1.0 | - | 0 | Vdc |
| | Output Sink Current $V_{in} \geq -10$ mV, $V_{out} \geq 0$ | I_S | 0.5 | 0.8 | - | mA dc |
|  <p> V_{in} </p> | Strobe Current $V_{strobe} = 100$ mVdc | I_{st} | - | 1.2 | 2.5 | mA dc |
| | Input Common Mode Range $V^- = -7.0$ Vdc | CM_{Vin} | ± 5.0 | - | - | Volts |
|  <p> e_{in}, V_b, e_{out}, e_{strobe} t_R, t_{SR} </p> | Response Time $V_b = 5.0$ mV + V_{io} | t_R | - | 40 | - | ns |
| | Strobe Release Time | t_{SR} | - | 12 | - | ns |
|  <p> V_{in}, V^+, I_{D^+}, V^-, I_{D^-} </p> | Power Supply Current $V_{out} \leq 0$ Vdc | I_{D^+} | - | 8.6 | - | mA dc |
| | Power Consumption | I_{D^-} | - | 3.9 | - | mA dc |
| | Power Consumption | | - | 130 | 200 | mW |

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

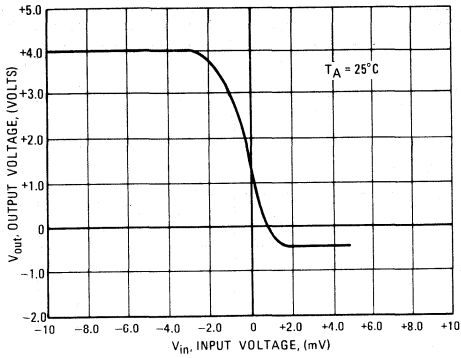


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

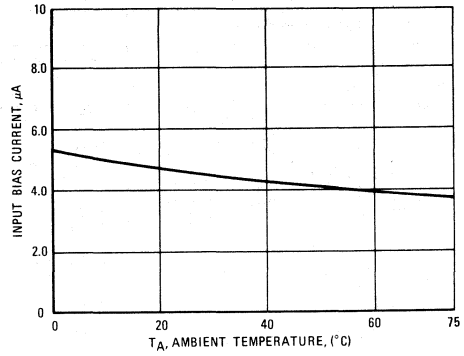


FIGURE 3 – VOLTAGE GAIN versus TEMPERATURE

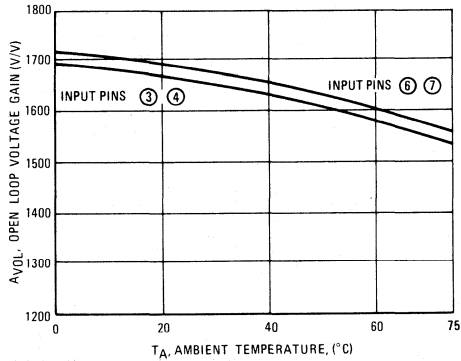


FIGURE 4 – RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

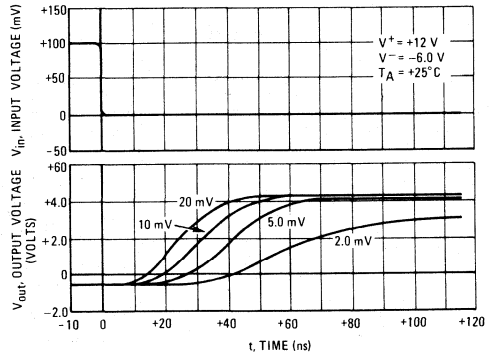


FIGURE 5 – VOLTAGE GAIN VARIATION WITH POWER SUPPLY VOLTAGE

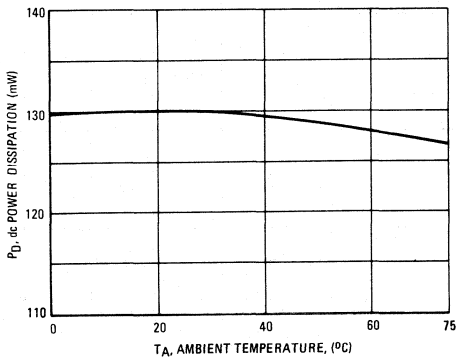
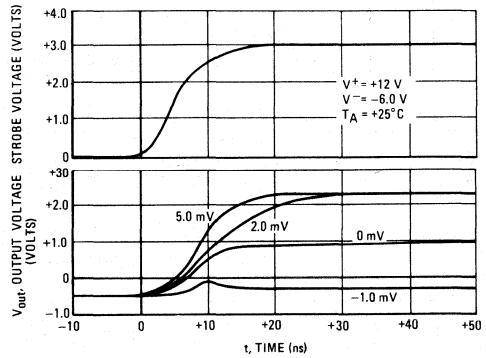


FIGURE 6 – STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



7

MC1711C (continued)

FIGURE 7 – COMMON-MODE PULSE RESPONSE

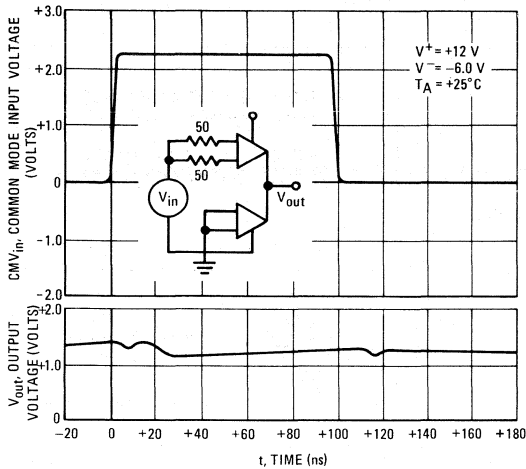


FIGURE 8 – OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

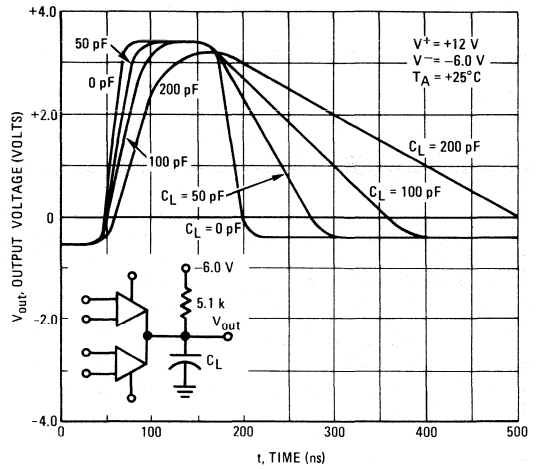


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL* LOADS

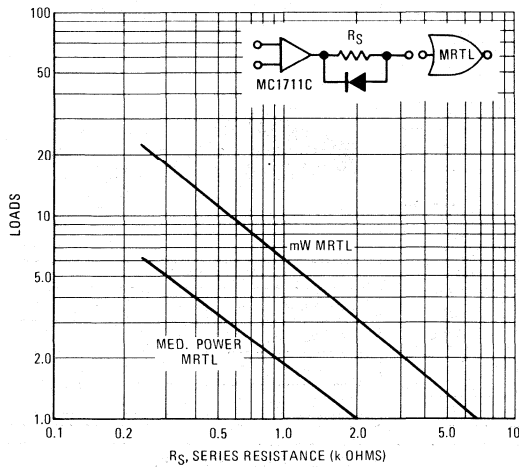
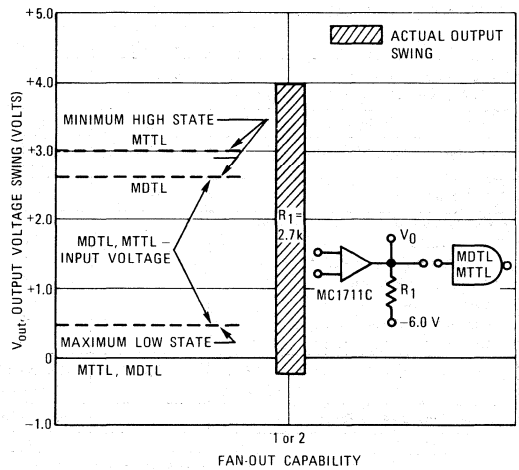


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL* OR MTTL* OUTPUT SWING



MC1712 MC1712C

OPERATIONAL AMPLIFIERS

MONOLITHIC WIDEBAND DC AMPLIFIER

... designed for use as an operational amplifier utilizing operating characteristics as a function of the external feedback components.

- Open Loop Gain $A_{VOL} = 3600$ typical
- Low Temperature Drift $-\pm 2.5 \mu V/^\circ C$
- Output Voltage Swing $-\pm 5.3 V$ typical @ $+12 V$ and $-6 V$ Supplies
- Low Output Impedance $-Z_{out} = 200$ ohms typical

WIDEBAND DC AMPLIFIER INTEGRATED CIRCUIT MONOLITHIC SILICON EPITAXIAL PASSIVATED



G SUFFIX
METAL PACKAGE
CASE 601
TO-99
Lead 4 connected to case

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

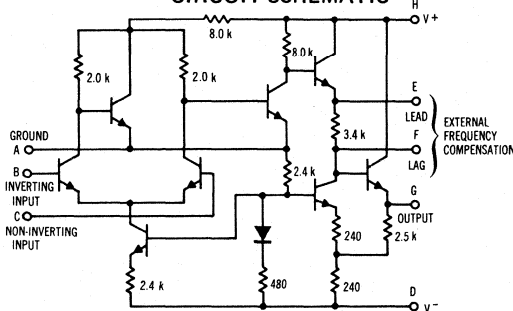
MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---------------|-------------------------|----------------|
| Power Supply Voltage (Total between V^+ and V^- terminals) | $ V^+ + V^- $ | 21 | Vdc |
| Differential Input Signal | V_{in} | ± 5.0 | Volts |
| Common Mode Input Swing | CMV_{in} | +1.5 -6.0 | Volts |
| Peak Load Current | I_L | 50 | mA |
| Power Dissipation (Package Limitation) | P_D | | |
| Metal Package | | 680 | mW |
| Derate above $T_A = +25^\circ C$ | | 4.6 | mW/ $^\circ C$ |
| Flat Ceramic Package | | 500 | mW |
| Derate above $T_A = +25^\circ C$ | | 3.3 | mW/ $^\circ C$ |
| Dual In-Line Ceramic Package | | 625 | mW |
| Derate above $T_A = +25^\circ C$ | | 5.0 | mW/ $^\circ C$ |
| Operating Temperature Range MC1712 MC1712C | T_A | -55 to +125 0 to +75 | $^\circ C$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ C$ |

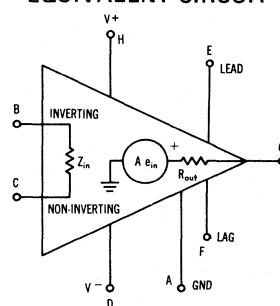
PIN CONNECTIONS

| Schematic | A | B | C | D | E | F | G | H |
|-------------|---|---|---|---|---|----|----|----|
| "G" Package | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| "F" Package | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 10 |
| "L" Package | 3 | 4 | 5 | 6 | 9 | 10 | 12 | 13 |

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

MC1712, MC1712C (continued)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

| Characteristic | Symbol | MC1712 | | | MC1712C | | | Unit |
|---|--|------------------------------|---|---|--------------------------------------|---|---|--|
| | | Min | Typ | Max | Min | Typ | Max | |
| Open-Loop Voltage Gain (R _L = 100 kΩ) (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc, V _O = ±2.5 V) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc, V _O = ±5.0 V) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc, V _O = ±5.0 Vdc, T _A = T _{low} ①, T _{high} ①) (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc, V _O = ±2.5 V, T _A = T _{low} to T _{high}) | A _{VOL} | 800 2500 | 900 3600 | 1500 6000 | 500 2000 | 800 3400 | 1500 6000 | V/V |
| Output Impedance (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc, f = 20 Hz) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc, f = 20 Hz) | Z _{out} | - | 300 200 | 700 500 | - | 300 200 | 800 600 | ohms |
| Input Impedance (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc, f = 20 Hz) (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc, f = 20 Hz, T _A = T _{low} , T _{high}) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc, f = 20 Hz) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc, f = 20 Hz, T _A = T _{low} , T _{high}) | Z _{in} | 22 8.0 16 6.0 | 70 - 40 - | - - - - | 16 10 - | 55 32 - | - - - | k ohms |
| Output Voltage Swing (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc, R _L = 100 kΩ) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc, R _L = 100 kΩ) (V ⁺ = +6.0 Vdc, V ⁻ = -3.0 Vdc, R _L = 10 kΩ) (V ⁺ = +12 Vdc, V ⁻ = -6.0 Vdc, R _L = 10 kΩ) | V _O | ±2.5 ±5.0 ±1.5 ±3.5 | ±2.7 ±5.3 ±2.0 ±4.0 | - - - - | ±2.5 ±5.0 ±1.5 ±3.5 | ±2.7 ±5.3 ±2.0 ±4.0 | - - - - | V _{peak} |
| Input Common-Mode Voltage Swing (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc) | CMV _{in} | +0.5 -1.5 +0.5 -4.0 | - - - - | - - - - | +0.5 -1.5 +0.5 -4.0 | - - - - | - - - - | V _{peak} |
| Common-Mode Rejection Ratio (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc, f ≤ 1.0 kHz) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc, f = 1.0 kHz) | CM _{rej} | 80 80 | 100 100 | - - | 70 70 | 95 95 | - - | dB |
| Input Bias Current T _A = +25°C (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc) $I_b = \frac{I_1 + I_2}{2}$, T _A = T _{low} (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc) | I _b | - - - - | 1.2 2.0 2.5 4.0 | 3.5 5.0 7.5 10 | - - - - | 1.5 2.5 2.5 4.0 | 5.0 7.5 8.0 12 | μA |
| Input Offset Current (I _{io} = I ₁ - I ₂) (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc) (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc, T _A = T _{low} to T _{high}) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc, T _A = T _{low} to T _{high}) | I _{io} | - - - - | 0.1 - 0.2 - | 0.5 1.5 - 1.5 | - - 0.5 - | - - 0.5 - | 2.0 2.5 2.0 2.5 | μA |
| Input Offset Voltage (R _S = 2.0 kΩ) (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc) (V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc, T _A = T _{low} , T _{high}) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc, T _A = T _{low} , T _{high}) | V _{io} | - - - - | 1.3 - 1.1 - | 3.0 4.0 2.0 3.0 | - - 1.5 - | - - 1.5 - | 6.0 7.5 5.0 6.5 | mV |
| Step Response (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc) (Gain = 100, V _{in} = 1.0 mV, R ₁ = 1.0 kΩ, R ₂ = 100 kΩ, C ₂ = 50 pF, R ₃ = ∞, C ₁ = open) (V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc) (Gain = 1.0, V _{in} = 10 mV, R ₁ = 10 kΩ, R ₂ = 10 kΩ, C ₁ = 0.01 μF, R ₃ = 20Ω, C ₂ = open) | V _{os} t _f dV _{out} /dt ② V _{os} t _f dV _{out} /dt ② | - - - - - - | 20 10 10 12 10 25 16 1.5 | 40 30 - - 50 120 - - | - - - - - - - - | 20 10 12 10 25 16 1.5 | 40 30 - - 50 120 - - | % ns V/μs % ns ns V/μs |
| Average Temperature Coefficient of Input Offset Voltage (R _S = 50Ω) (T _A = +25°C to T _{high}) (T _A = T _{low} to +25°C) (T _A = T _{low} , T _{high}) | TC _{Vio} | - - - | 2.5 2.0 - | - - - | - - - | - - 5.0 | - - - | μV/°C |
| Average Temperature Coefficient Input Offset Current (T _A = +25°C to T _{high}) (T _A = T _{low} to +25°C) | TC _{Iio} | - - | 0.05 1.5 | - - | - - | 4.0 6.0 | - - | nA/°C |
| DC Power Dissipation (V _{out} = 0, V ⁺ = 6.0 Vdc, V ⁻ = -3.0 Vdc) (V _{out} = 0, V ⁺ = 12 Vdc, V ⁻ = -6.0 Vdc) | P _D | - - | 17 70 | 30 120 | - - | 17 70 | 30 120 | mW |
| Positive Supply Sensitivity (V ⁻ constant = -6.0 Vdc, V ⁺ = 12 Vdc to 6.0 Vdc) | S ⁺ | - | 60 | 200 | - | 60 | 300 | μV/V |
| Negative Supply Sensitivity (V ⁺ constant = 12 Vdc, V ⁻ = -6.0 Vdc to -3.0 Vdc) | S ⁻ | - | 60 | 200 | - | 60 | 300 | μV/V |

① T_{low} = 0°C for MC1712C, T_{high} = +75°C for MC1712C
-55°C for MC1712 +125°C for MC1712

② dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

($V^+ = 12 \text{ Vdc}$, $V^- = -6.0 \text{ Vdc}$, $T_A = +25^\circ\text{C}$)

FIGURE 1 – OPEN LOOP GAIN versus POWER SUPPLY VARIATIONS

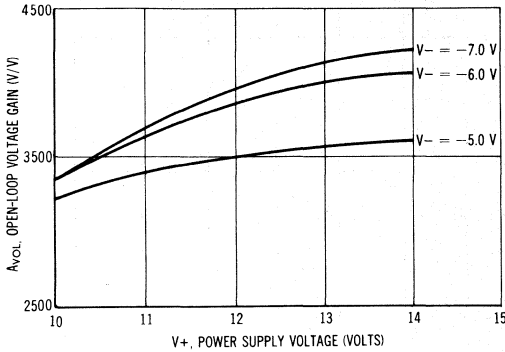


FIGURE 2 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

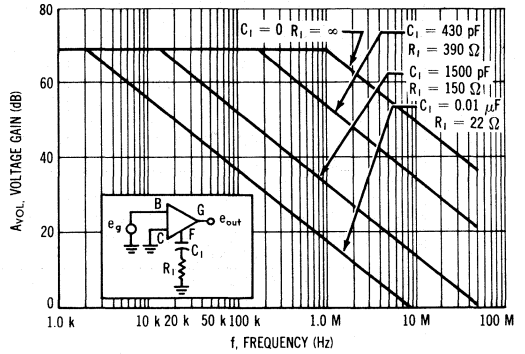


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

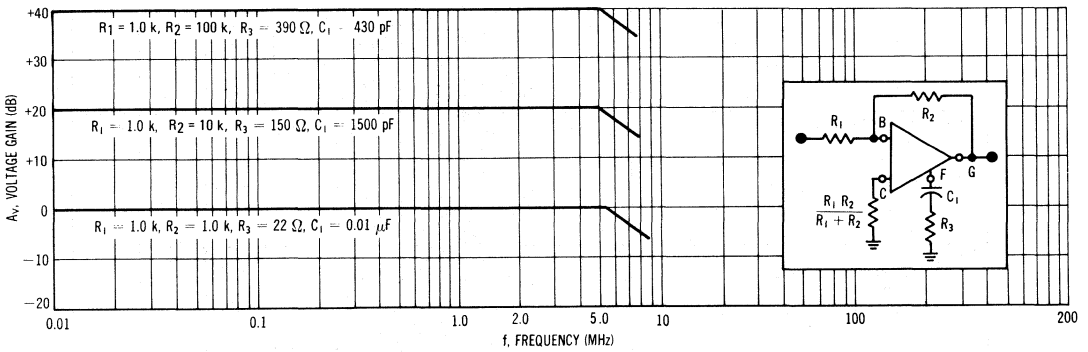


FIGURE 4 – MAXIMUM OUTPUT SWING versus FREQUENCY

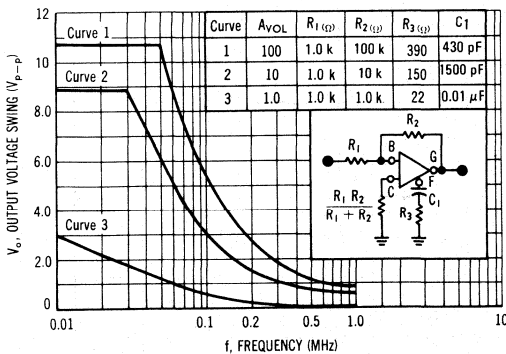
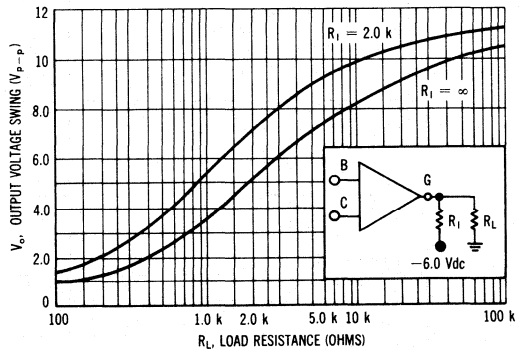


FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



7

TYPICAL CHARACTERISTICS(continued)

FIGURE 6 – INPUT BIAS CURRENT versus TEMPERATURE

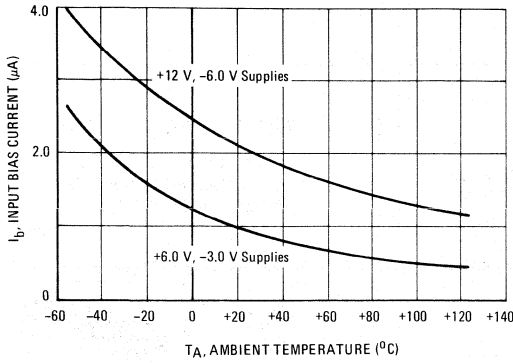


FIGURE 7 – INPUT OFFSET CURRENT versus TEMPERATURE

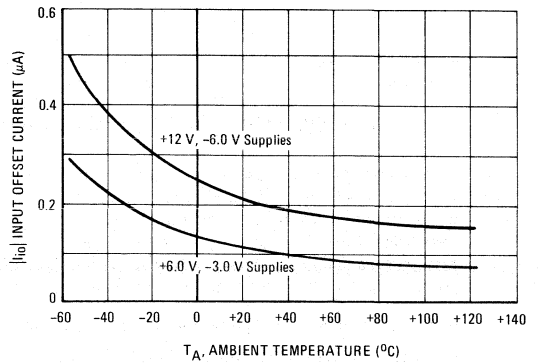


FIGURE 8 – INPUT OFFSET VOLTAGE versus TEMPERATURE

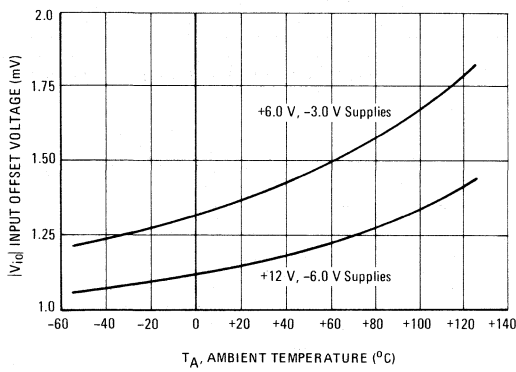
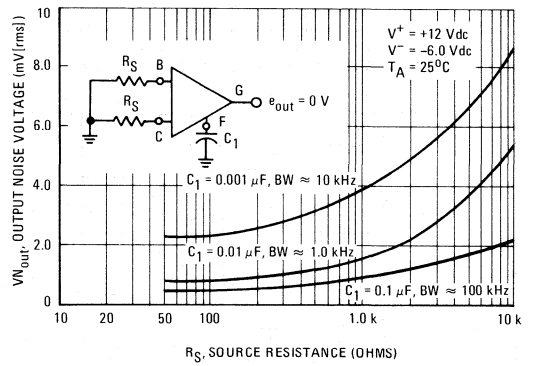


FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE IMPEDANCE



POSITIVE VOLTAGE REGULATORS

MC1723 MC1723C

MONOLITHIC VOLTAGE REGULATOR

The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mA dc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (-55°C to +125°C) and the MC1723C over the commercial temperature range (0 to +75°C)

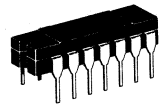
- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mA dc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short-Circuit Protection

VOLTAGE REGULATOR

MONOLITHIC SILICON
EPITAXIAL PASSIVATED
INTEGRATED CIRCUIT



Pin 5 connected to case through substrate.
G SUFFIX
METAL PACKAGE
CASE 603-03



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

FIGURE 1 — TYPICAL CIRCUIT CONNECTION
(7 < V_O < 37)

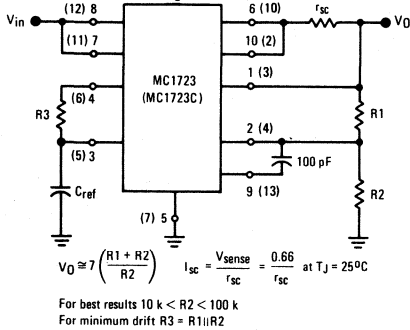


FIGURE 2 — TYPICAL NPN CURRENT BOOST CONNECTION

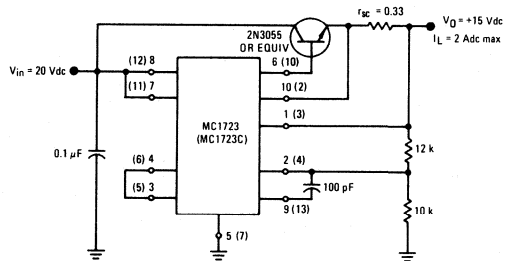
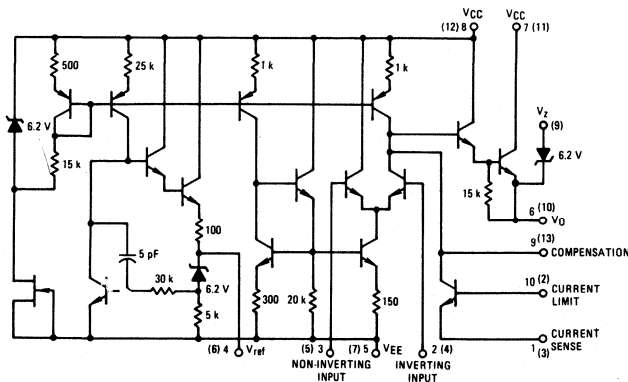
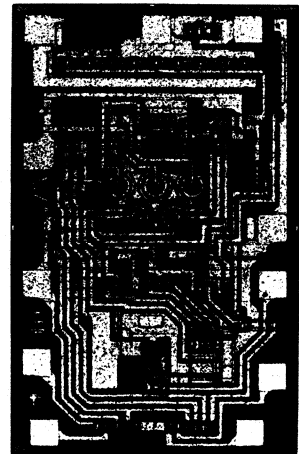


FIGURE 3 — CIRCUIT SCHEMATIC



PIN NUMBERS ADJACENT TO TERMINALS ARE FOR THE METAL PACKAGE;
PIN NUMBERS IN PARENTHESIS ARE FOR THE CERAMIC DUAL IN-LINE PACKAGE.



See Packaging Information Section for outline dimensions.

See current MCC1723/1723C data sheet for standard linear chip information.
See current MCBC1723/MCB1723F data sheet for beam-lead chip information.

MC1723, MC1723C (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|-----------------------------------|-------------|-------------------|
| Pulse Voltage from V _{CC} to V _{EE} (50 ms) | MC1723 V _{in(p)} | 50 | V _{peak} |
| Continuous Voltage from V _{CC} to V _{EE} | V _{in} | 40 | V _d c |
| Input-Output Voltage Differential | V _{in} -V _O | 40 | V _d c |
| Maximum Output Current | I _L | 150 | mAdc |
| Current from V _{ref} | I _{ref} | 15 | mAdc |
| Power Dissipation and Thermal Characteristics | | | |
| Metal Package | | | |
| T _A = +25°C | P _D | 0.8 | Watt |
| Derate above T _A = +25°C | 1/θ _{JA} | 5.4 | mW/°C |
| Thermal Resistance, Junction to Air | θ _{JA} | 185 | °C/W |
| T _C = +25°C | P _D | 2.1 | Watts |
| Derate above T _A = +25°C | 1/θ _{JC} | 14 | mW/°C |
| Thermal Resistance, Junction to Case | θ _{JC} | 70 | °C/W |
| Dual In-Line Ceramic Package | | | |
| Derate above T _A = +25°C | P _D | 1.0 | Watt |
| Thermal Resistance, Junction to Air | 1/θ _{JA} | 6.7 | mW/°C |
| | θ _{JA} | 150 | °C/W |
| Operating and Storage Junction Temperature Range | | | |
| Metal Package | T _J , T _{stg} | -65 to +150 | °C |
| Dual In-Line Ceramic Package | | -65 to +175 | |

OPERATING TEMPERATURE RANGE

| Ambient Temperature | MC1723C MC1723 | T _A | °C |
|---------------------|-------------------|----------------|-------------------------|
| | | | 0 to +75 -55 to +125 |

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} = 12 V_dc, V_O = 5 V_dc, I_L = 1 mAdc, r_{sc} = 0, C₁ = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 1)

| Characteristic | Symbol* | MC1723 | | | MC1723C | | | Unit |
|---|---------------------------------|--------|-------|-------|---------|-------|-------|------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage Range | V _{in} | 9.5 | — | 40 | 9.5 | — | 40 | V _d c |
| Output Voltage Range | V _O | 2.0 | — | 37 | 2.0 | — | 37 | V _d c |
| Input-Output Voltage Differential | V _{in} -V _O | 3.0 | — | 38 | 3.0 | — | 38 | V _d c |
| Reference Voltage | V _{ref} | 6.95 | 7.15 | 7.35 | 6.80 | 7.15 | 7.50 | V _d c |
| Standby Current Drain (I _L = 0, V _{in} = 30 V) | I _{IB} | — | 2.3 | 3.5 | — | 2.3 | 4.0 | mAdc |
| Output Noise Voltage (f = 100 Hz to 10 kHz) | V _n | — | 20 | — | — | 20 | — | μV(rms) |
| C _{ref} = 0 | | — | 2.5 | — | — | 2.5 | — | |
| C _{ref} = 5.0 μF | | — | — | — | — | — | — | |
| Average Temperature Coefficient of Output Voltage (T _{low} ① < T _A < T _{high} ②) | TCV _O | — | 0.002 | 0.015 | — | 0.003 | 0.015 | %/°C |
| Line Regulation | Reg _{in} | — | 0.01 | 0.1 | — | 0.01 | 0.1 | %V _O |
| (T _A = +25°C) { 12 V < V _{in} < 15 V | | — | 0.02 | 0.2 | — | 0.1 | 0.5 | |
| (T _{low} ① < T _A < T _{high} ②) | | — | — | 0.3 | — | — | 0.3 | |
| 12 V < V _{in} < 15 V | | — | — | — | — | — | — | |
| Load Regulation (1.0 mA < I _L < 50 mA) | Reg _{load} | — | 0.03 | 0.15 | — | 0.03 | 0.2 | %V _O |
| T _A = +25°C | | — | — | 0.6 | — | — | 0.6 | |
| T _{low} ① < T _A < T _{high} ② | | — | — | — | — | — | — | |
| Ripple Rejection (f = 50 Hz to 10 kHz) | Rej _R | — | 74 | — | — | 74 | — | dB |
| C _{ref} = 0 | | — | 86 | — | — | 86 | — | |
| C _{ref} = 5.0 μF | | — | — | — | — | — | — | |
| Short Circuit Current Limit (r _{sc} = 10 Ω, V _O = 0) | I _{sc} | — | 65 | — | — | 65 | — | mAdc |
| Long Term Stability | ΔV _O /Δt | — | 0.1 | — | — | 0.1 | — | %/1000 Hr |

*Symbols conform to JEDEC Bulletin No. 1 where applicable.

① T_{low} = 0°C for MC1723C
= -55°C for MC1723

② T_{high} = +75°C for MC1723C
= +125°C for MC1723

TYPICAL CHARACTERISTICS

($V_{in} = 12 \text{ Vdc}$, $V_O = 5.0 \text{ Vdc}$, $I_L = 1.0 \text{ mA}$, $r_{sc} = 0$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 4 – MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

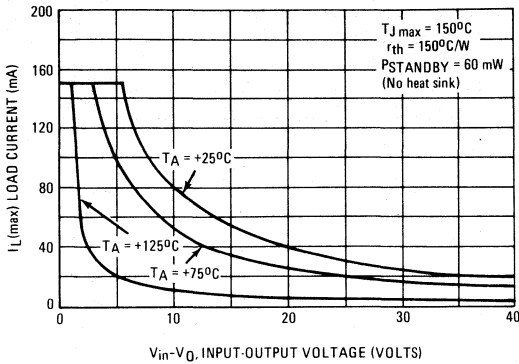


FIGURE 5 – LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

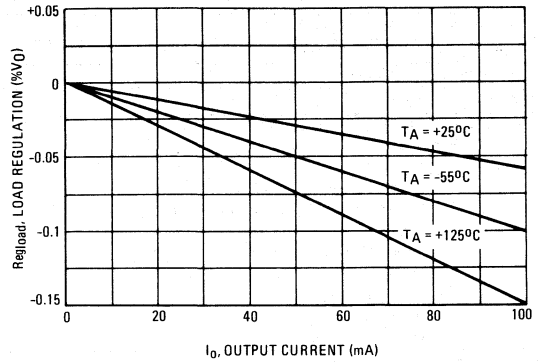


FIGURE 6 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

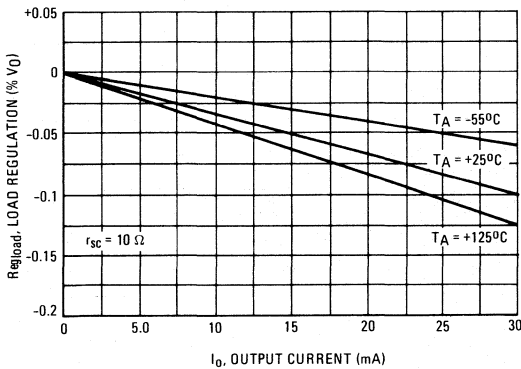


FIGURE 7 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

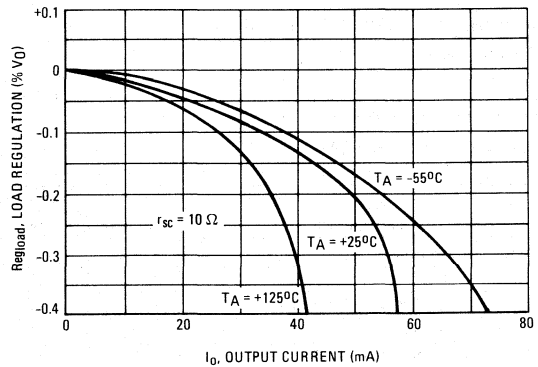


FIGURE 8 – CURRENT LIMITING CHARACTERISTICS -

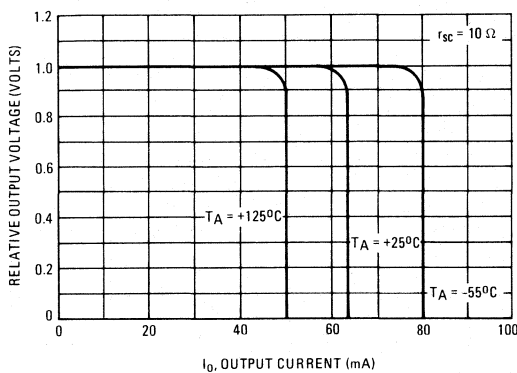
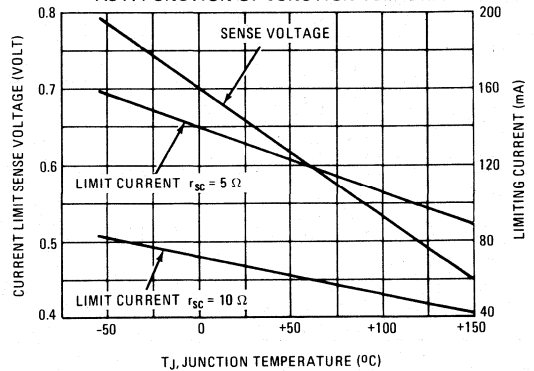


FIGURE 9 – CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

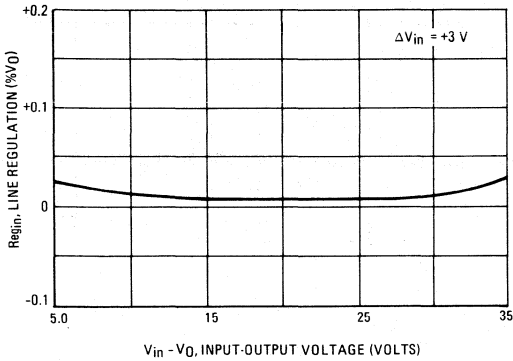


FIGURE 11 – LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

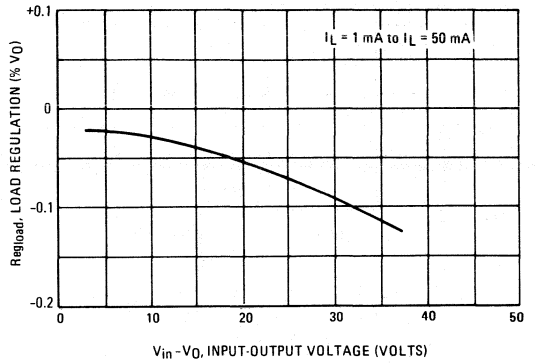


FIGURE 12 – STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

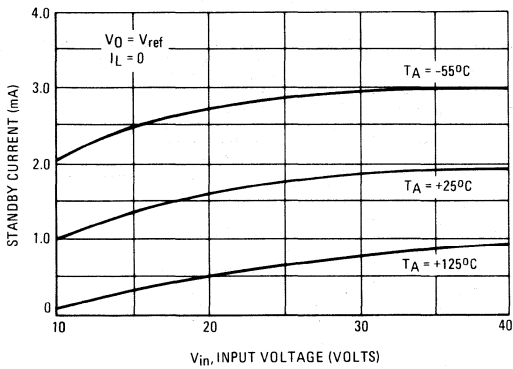


FIGURE 13 – LINE TRANSIENT RESPONSE

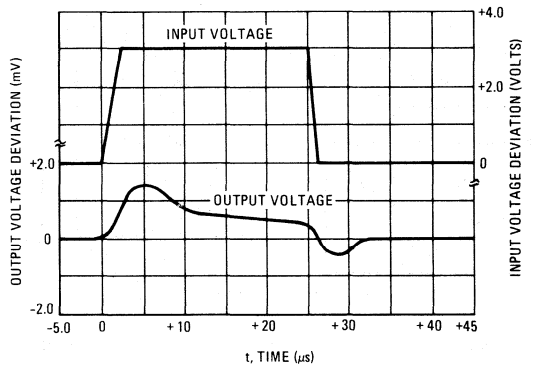


FIGURE 14 – LOAD TRANSIENT RESPONSE

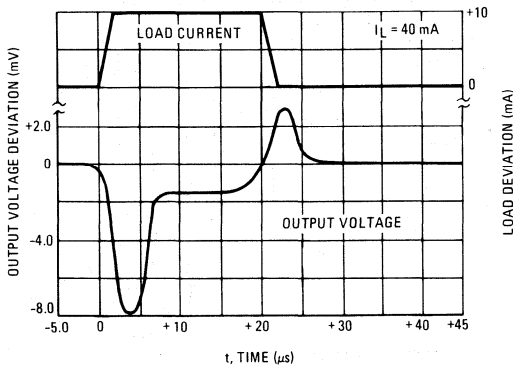
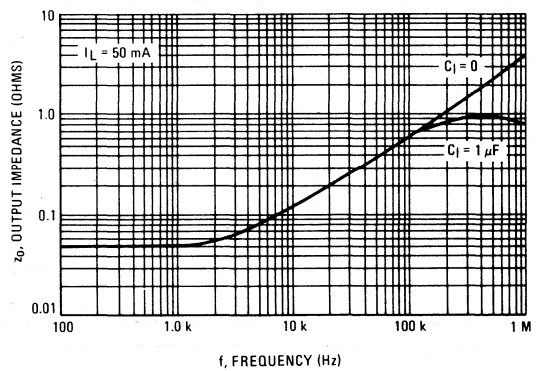


FIGURE 15 – OUTPUT IMPEDANCE AS FUNCTION OF FREQUENCY

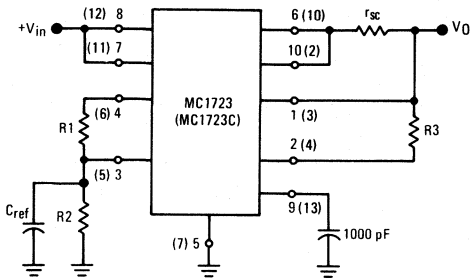


MC1723, MC1723C (continued)

TYPICAL APPLICATIONS

Pin numbers adjacent to terminals are for the metal package; pin numbers in parenthesis are for the ceramic dual in-line package.

FIGURE 16 – TYPICAL CONNECTION FOR $2 < V_O < 7$



$$V_O \cong 7 \left[\frac{R_2}{R_1 + R_2} \right] \quad I_{sc} = \frac{V_{sense}}{r_{sc}} \cong \frac{0.66}{r_{sc}} \text{ at } T_J = +25^\circ\text{C}$$

For best results $10 \text{ k} < R_1 + R_2 < 100 \text{ k}$.
For minimum drift $R_3 = R_1 || R_2$.

FIGURE 17 – MC1723,C FOLDBACK CONNECTION

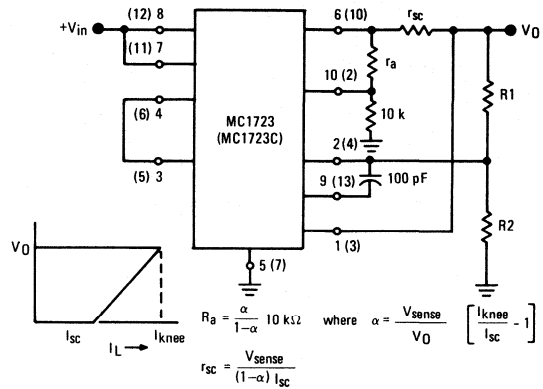


FIGURE 18 – +5 V, 1-AMPERE SWITCHING REGULATOR

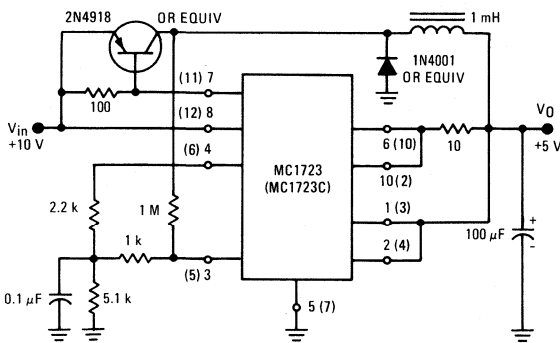


FIGURE 19 – +5 V, 1-AMPERE HIGH EFFICIENCY REGULATOR

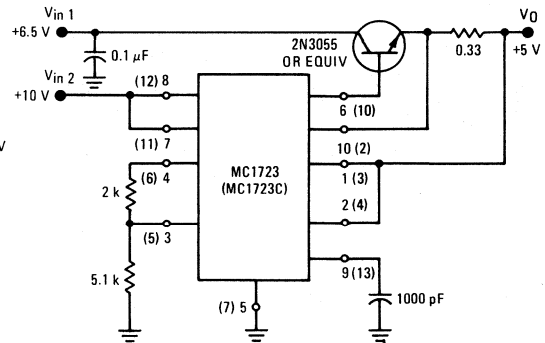


FIGURE 20 – +15 V, 1-AMPERE REGULATOR WITH REMOTE SENSE

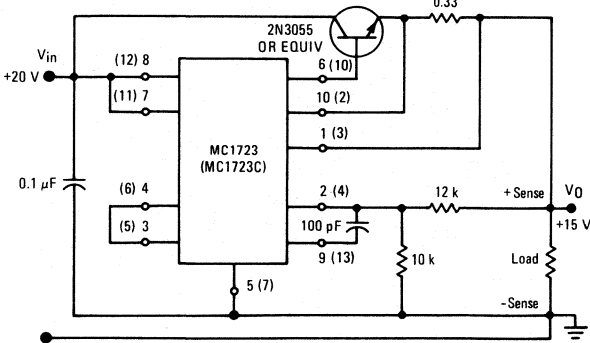
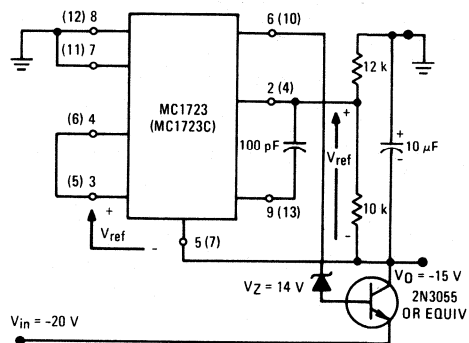


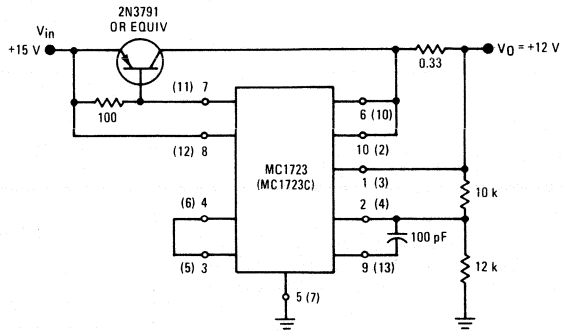
FIGURE 21 – -15 V NEGATIVE REGULATOR



MC1723, MC1723C (continued)

TYPICAL APPLICATIONS (continued)

FIGURE 22 — +12 V, 1-AMPERE REGULATOR
USING PNP CURRENT BOOST



Pin numbers adjacent to terminals are for the metal package; pin numbers in parenthesis are for the ceramic dual in-line package.

MC1733 MC1733C

MONOLITHIC DIFFERENTIAL VIDEO AMPLIFIER

... a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

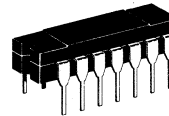
- Bandwidth — 120 MHz typical @ $A_{VD} = 10$
- Rise Time — 2.5 ns typical @ $A_{VD} = 10$
- Propagation Delay Time — 3.6 ns typical @ $A_{VD} = 10$

DIFFERENTIAL VIDEO WIDEBAND AMPLIFIER

MONOLITHIC SILICON
INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 603-02
TO-100



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 — BASIC CIRCUIT

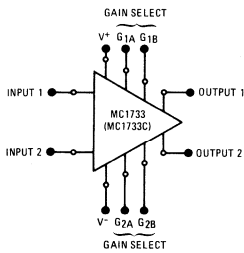


FIGURE 2 — VOLTAGE GAIN
ADJUST CIRCUIT

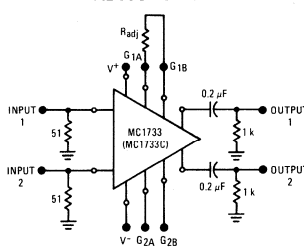
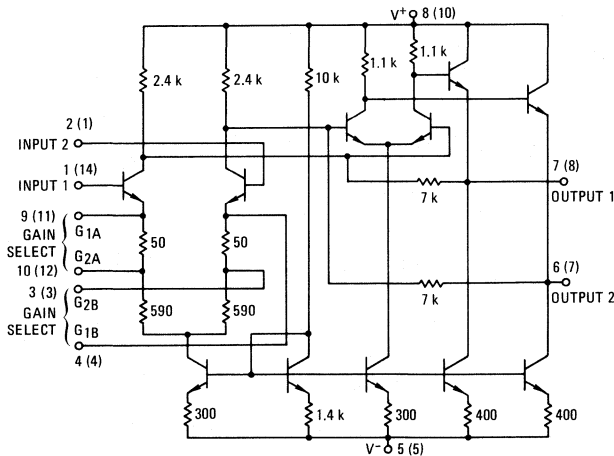
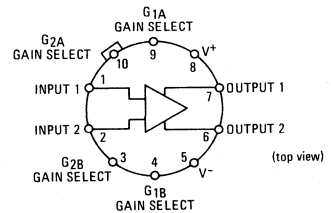


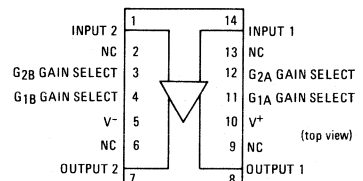
FIGURE 3 — CIRCUIT SCHEMATIC



CONNECTION DIAGRAMS



G SUFFIX, METAL PACKAGE
Pin 5 connected to case.



L SUFFIX, CERAMIC PACKAGE

MC1733, MC1733C (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|-------------------------------------|----------------|-------------------------|------------------|
| Power Supply Voltage | V^+ V^- | +8.0 -8.0 | Volts |
| Differential Input Voltage | V_{in} | ± 5.0 | Volts |
| Common-Mode Input Voltage | CMV_{in} | ± 6.0 | Volts |
| Output Current | I_o | 10 | mA |
| Internal Power Dissipation (Note 1) | P_D | 500 500 | mW |
| Operating Temperature Range | T_A | 0 to +75 -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

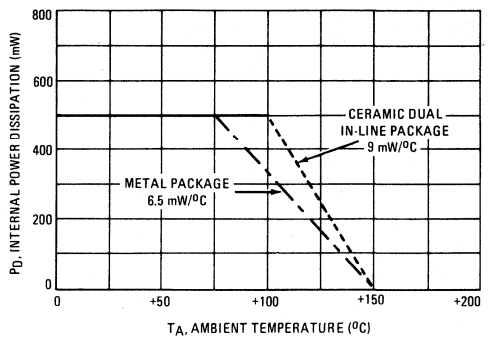
ELECTRICAL CHARACTERISTICS ($V^+ = +6.0\text{ Vdc}$, $V^- = -6.0\text{ Vdc}$, at $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MC1733 | | | MC1733C | | | Units |
|---|------------|-----------|------|-----|-----------|------|-----|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential Voltage Gain | A_{vd} | 300 | 400 | 500 | 250 | 400 | 600 | |
| Gain 1 (Note 2) | | 90 | 100 | 110 | 80 | 100 | 120 | |
| Gain 2 (Note 3) | | 9.0 | 10 | 11 | 8.0 | 10 | 12 | |
| Gain 3 (Note 4) | | — | — | — | — | — | — | |
| Bandwidth ($R_s = 50\ \Omega$) | BW | — | 40 | — | — | 40 | — | MHz |
| Gain 1 | | — | 90 | — | — | 90 | — | |
| Gain 2 | | — | 120 | — | — | 120 | — | |
| Gain 3 | | — | — | — | — | — | — | |
| Rise Time ($R_s = 50\ \Omega$, $V_o = 1\text{ Vp-p}$) | t_r | — | 10.5 | — | — | 10.5 | — | ns |
| Gain 1 | | — | 4.5 | 10 | — | 4.5 | 12 | |
| Gain 2 | | — | 2.5 | — | — | 2.5 | — | |
| Gain 3 | | — | — | — | — | — | — | |
| Propagation Delay ($R_s = 50\ \Omega$, $V_o = 1\text{ Vp-p}$) | t_{pd} | — | 7.5 | — | — | 7.5 | — | ns |
| Gain 1 | | — | 6.0 | 10 | — | 6.0 | 10 | |
| Gain 2 | | — | 3.6 | — | — | 3.6 | — | |
| Gain 3 | | — | — | — | — | — | — | |
| Input Resistance | R_{in} | — | 4.0 | — | — | 4.0 | — | k Ω |
| Gain 1 | | 20 | 30 | — | 10 | 30 | — | |
| Gain 2 | | — | 250 | — | — | 250 | — | |
| Gain 3 | | — | — | — | — | — | — | |
| Input Capacitance (Gain 2) | C_{in} | — | 2.0 | — | — | 2.0 | — | pF |
| Input Offset Current | $ I_{io} $ | — | 0.4 | 3.0 | — | 0.4 | 5.0 | μA |
| Input Bias Current | I_b | — | 9.0 | 20 | — | 9.0 | 30 | μA |
| Input Noise Voltage ($R_s = 50\ \Omega$, BW = 1 kHz to 10 MHz) | V_n | — | 12 | — | — | 12 | — | $\mu\text{V(rms)}$ |
| Input Voltage Range | V_{in} | ± 1.0 | — | — | ± 1.0 | — | — | V |
| Common-Mode Rejection Ratio | CM_{rej} | 60 | 86 | — | 60 | 86 | — | dB |
| Gain 2 ($V_{CM} = \pm 1\text{ V}$, $f \leq 100\text{ kHz}$) | | — | 60 | — | — | 60 | — | |
| Gain 2 ($V_{CM} = \pm 1\text{ V}$, $f = 5\text{ MHz}$) | | — | — | — | — | — | — | |
| Supply Voltage Rejection Ratio | S^+, S^- | 50 | 70 | — | 50 | 70 | — | dB |
| Gain 2 ($\Delta V_s = \pm 0.5\text{ V}$) | | — | — | — | — | — | — | |
| Output Offset Voltage | V_{oo} | — | 0.6 | 1.5 | — | 0.6 | 1.5 | V |
| Gain 1 | | — | 0.35 | 1.0 | — | 0.35 | 1.5 | |
| Gain 2 and Gain 3 | | — | — | — | — | — | — | |
| Output Common-Mode Voltage | CMV_o | 2.4 | 2.9 | 3.4 | 2.4 | 2.9 | 3.4 | V |
| Output Voltage Swing | V_o | 3.0 | 4.0 | — | 3.0 | 4.0 | — | V _{p-p} |
| Output Sink Current | I_o | 2.5 | 3.6 | — | 2.5 | 3.6 | — | mA |
| Output Resistance | R_{out} | — | 20 | — | — | 20 | — | Ω |
| Power Supply Current | I_D | — | 18 | 24 | — | 18 | 24 | mA |

NOTES

- Note 1: Derate metal package at 6.5 mW/°C for operation at ambient temperatures above 75°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 100°C (see Figure 4). If operation at high ambient temperatures is required (MC1733) a heatsink may be necessary to limit maximum junction temperature to 150°C. Thermal resistance, junction-to-case, for the metal package is 69.4°C per Watt.
- Note 2: Gain Select pins G_{1A} and G_{1B} connected together.
- Note 3: Gain Select pins G_{2A} and G_{2B} connected together.
- Note 4: All Gain Select pins open.

FIGURE 4 – MAXIMUM ALLOWABLE POWER DISSIPATION



TYPICAL CHARACTERISTICS

(V⁺ = +6.0 Vdc, V⁻ = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE

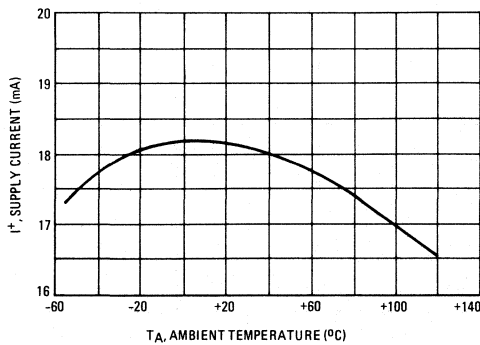
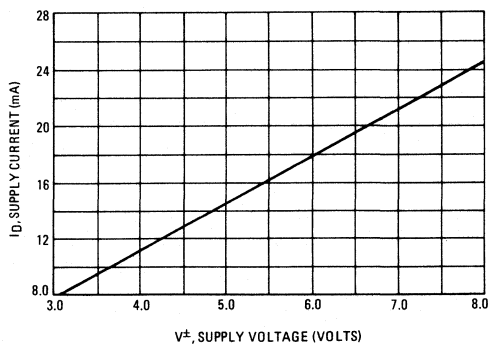


FIGURE 6 – SUPPLY CURRENT versus SUPPLY VOLTAGE



7

TYPICAL CHARACTERISTICS (continued)
 ($V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 7 – GAIN versus TEMPERATURE

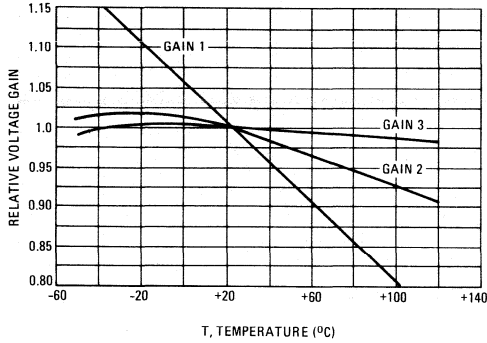


FIGURE 8 – GAIN versus FREQUENCY

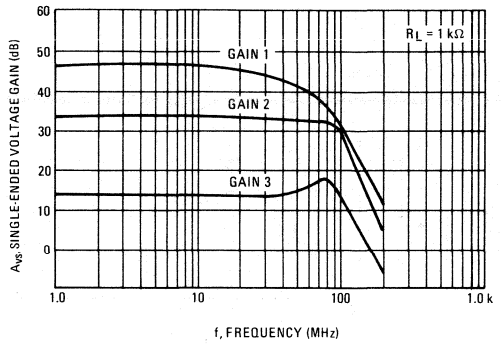


FIGURE 9 – GAIN versus SUPPLY VOLTAGE

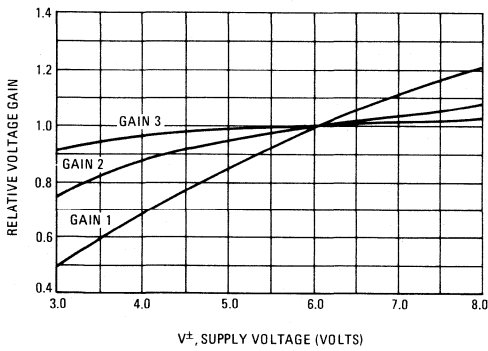


FIGURE 10 – GAIN versus R_{ADJUST}

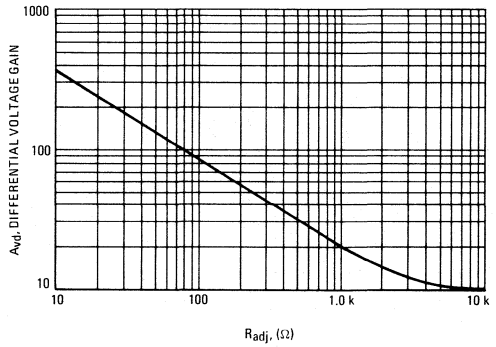


FIGURE 11 – GAIN versus FREQUENCY and SUPPLY VOLTAGE

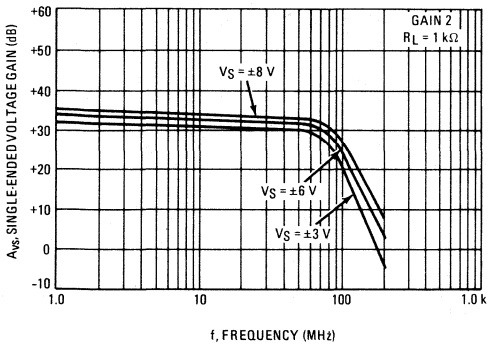
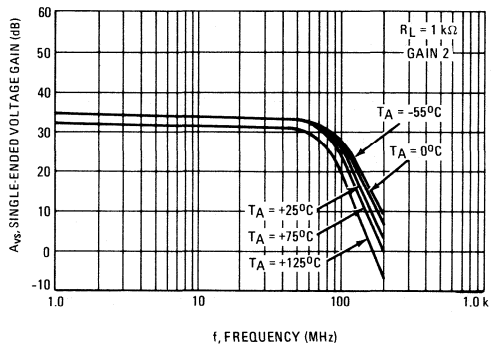


FIGURE 12 – GAIN versus FREQUENCY and TEMPERATURE



TYPICAL CHARACTERISTICS (continued)
 ($V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 13 – PULSE RESPONSE versus GAIN

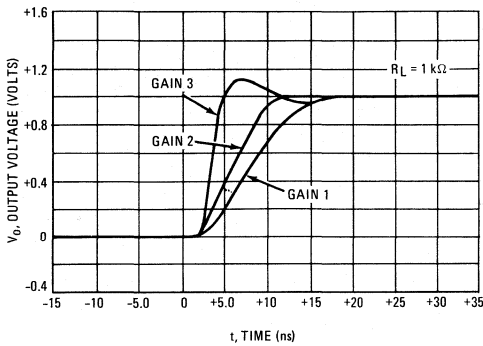


FIGURE 14 – PULSE RESPONSE versus SUPPLY VOLTAGE

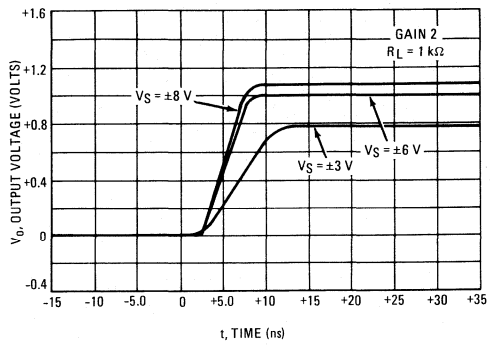


FIGURE 15 – PULSE RESPONSE versus TEMPERATURE

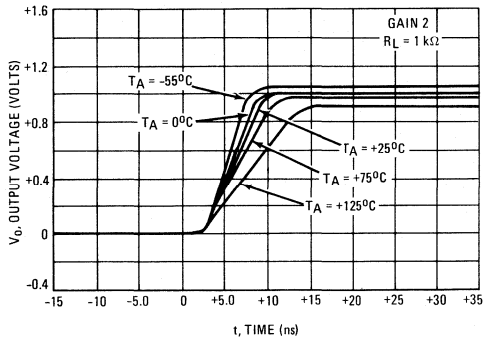


FIGURE 16 – DIFFERENTIAL OVERDRIVE RECOVERY TIME

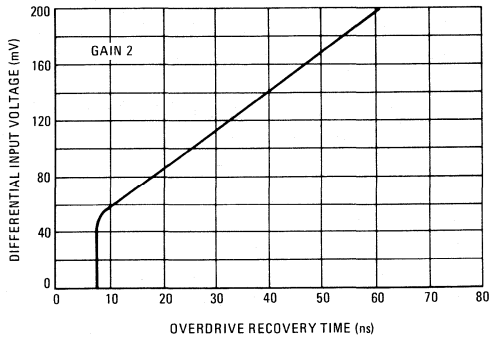


FIGURE 17 – PHASE SHIFT versus FREQUENCY

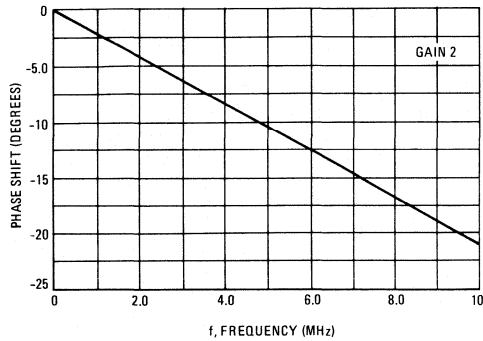
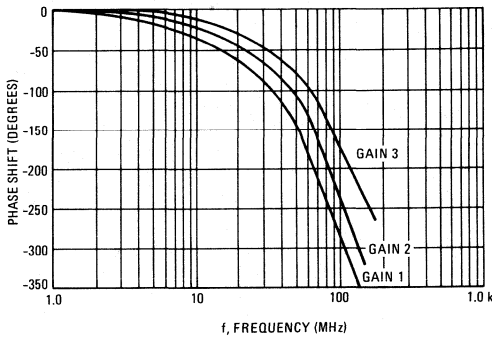


FIGURE 18 – PHASE SHIFT versus FREQUENCY



7

TYPICAL CHARACTERISTICS (continued)
 ($V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 19 – INPUT RESISTANCE versus TEMPERATURE

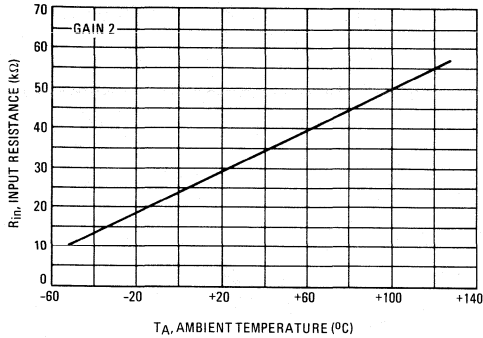


FIGURE 20 – INPUT NOISE VOLTAGE

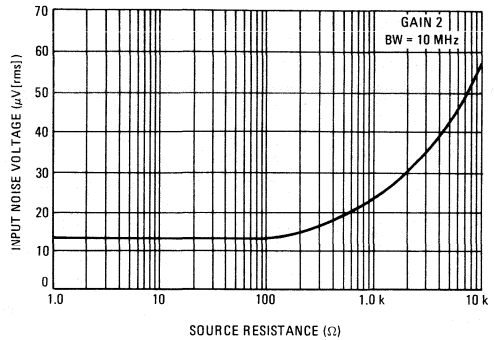


FIGURE 21 – OUTPUT VOLTAGE SWING and SINK CURRENT versus SUPPLY VOLTAGE

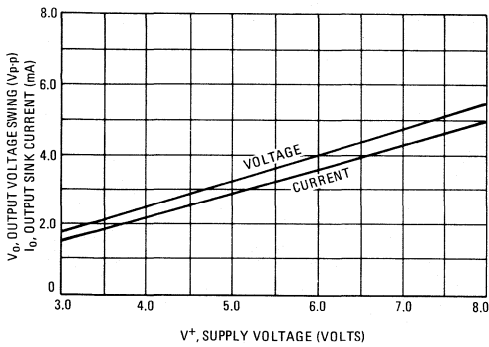


FIGURE 22 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

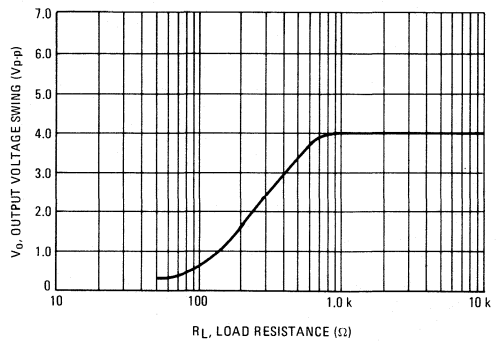


FIGURE 23 – OUTPUT VOLTAGE SWING versus FREQUENCY

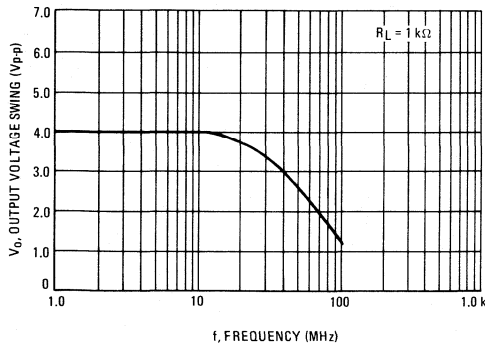
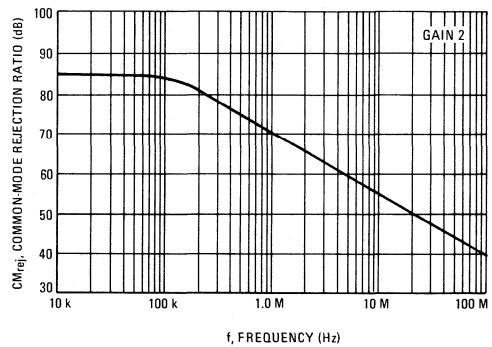


FIGURE 24 – COMMON-MODE REJECTION RATIO



MC1741 MC1741C

OPERATIONAL AMPLIFIERS

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

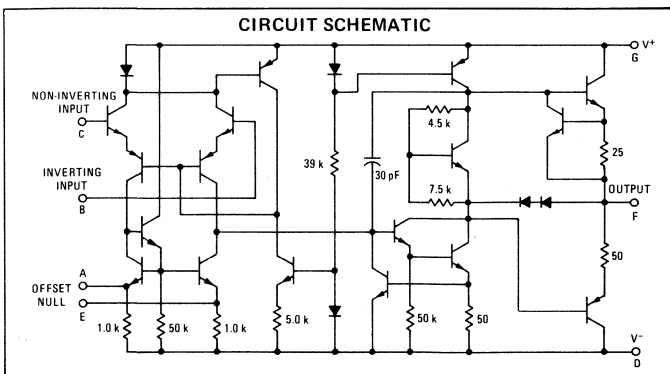
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | | Unit |
|--|----------------|-------------|-------------|----------------------|
| | | MC1741C | MC1741 | |
| Power Supply Voltage | V^+ V^- | +18 -18 | +22 -22 | Vdc Vdc |
| Differential Input Signal | V_{in} | ± 30 | | Volts |
| Common Mode Input Swing (Note 1) | CMV_{in} | ± 15 | | Volts |
| Output Short Circuit Duration (Note 2) | t_S | Continuous | | |
| Power Dissipation (Package Limitation) | P_D | | | |
| Metal Can | | 680 | | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 4.6 | | mW/ $^\circ\text{C}$ |
| Flat Package | | 500 | | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 3.3 | | mW/ $^\circ\text{C}$ |
| Plastic Dual In-Line Packages | | 625 | | mW |
| Derate above $T_A = +25^\circ\text{C}$ | | 5.0 | | mW/ $^\circ\text{C}$ |
| Ceramic Dual In-Line Package | | 750 | | mW/ $^\circ\text{C}$ |
| Derate above $T_A = +25^\circ\text{C}$ | | 6.0 | | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | 0 to +75 | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | | $^\circ\text{C}$ |
| Metal, Flat and Ceramic Packages | | -55 to +125 | | |

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.



See Packaging Information Section for outline dimensions.
See current MCBC1741/MCB1741F data sheet for beam-lead chip information.
See current MCCF1741,C data sheet for flip-chip information.

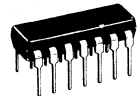
OPERATIONAL AMPLIFIER MONOLITHIC SILICON INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 601
TO-99



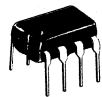
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P2 SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116
(MC1741C only)



F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

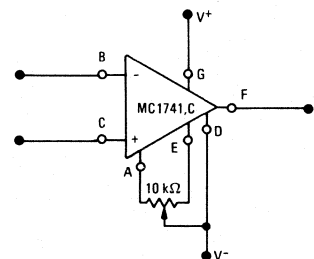
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1741C only)



PIN CONNECTIONS

| Schematic | A | B | C | D | E | F | G |
|---------------------|---|---|---|---|---|----|----|
| "G" & "P1" Packages | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| "F" Package | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| "P2" & "L" Packages | 3 | 4 | 5 | 6 | 9 | 10 | 11 |

FIGURE 1 - OFFSET ADJUST CIRCUIT



MC1741, MC1741C (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = 15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MC1741 | | | MC1741C (4) | | | Unit |
|--|--|----------------------------------|---------------------------|-------------|----------------------------------|---------------------------|-------------|--|
| | | Min | Typ | Max | Min | Typ | Max | |
| Open Loop Voltage Gain ($R_L = 2.0$ k Ω) ($V_O = \pm 10$ V, $T_A = +25^\circ\text{C}$) ($V_O = \pm 10$ V, $T_A = T_{low}$ (1) to T_{high} (2)) | AVOL | 50,000 25,000 | 200,000 — | — — | 20,000 15,000 | 100,000 — | — — | — |
| Output Impedance ($f = 20$ Hz) | Z_O | — | 75 | — | — | 75 | — | Ω |
| Input Impedance ($f = 20$ Hz) | Z_{in} | 0.3 | 1.0 | — | 0.3 | 1.0 | — | Meg Ω |
| Output Voltage Swing ($R_L = 10$ k Ω , $T_A = +25^\circ\text{C}$) ($R_L = 2.0$ k Ω , $T_A = +25^\circ\text{C}$) ($R_L = 2.0$ k Ω , $T_A = T_{low}$ (1) to T_{high} (2)) | V_O | ± 12 ± 10 ± 10 | ± 14 ± 13 — | — — — | ± 12 ± 10 ± 10 | ± 14 ± 13 — | — — — | V_{peak} |
| Input Common-Mode Voltage Swing | CMV _{in} | ± 12 | ± 13 | — | ± 12 | ± 13 | — | V_{peak} |
| Common-Mode Rejection Ratio ($f = 20$ Hz) | CM _{rej} | 70 | 90 | — | 70 | 90 | — | dB |
| Input Bias Current ($T_A = +25^\circ\text{C}$) ($T_A = T_{low}$ (1)) | I_b | — | 0.2 0.5 | 0.5 1.5 | — | 0.2 — | 0.5 0.8 | μA |
| Input Offset Current ($T_A = +25^\circ\text{C}$) ($T_A = T_{low}$ (1) to T_{high} (2)) | $ I_{io} $ | — | 0.03 — | 0.2 0.5 | — | 0.03 — | 0.2 0.3 | μA |
| Input Offset Voltage ($R_S = \leq 10$ k Ω) ($T_A = +25^\circ\text{C}$) ($T_A = T_{low}$ (1) to T_{high} (2)) | $ V_{io} $ | — | 1.0 — | 5.0 6.0 | — | 2.0 — | 6.0 7.5 | mV |
| Step Response Gain = 100, $R_1 = 1.0$ k Ω , $R_2 = 100$ k Ω , $R_3 = 1.0$ k Ω | t_f t_{pd} dV_{out}/dt (3) | — | 29 8.5 1.0 | — — — | — | 29 8.5 1.0 | — — — | μs μs V/ μs |
| Gain = 10, $R_1 = 1.0$ k Ω , $R_2 = 10$ k Ω , $R_3 = 1.0$ k Ω | t_f t_{pd} dV_{out}/dt (3) | — | 3.0 1.0 1.0 | — — — | — | 3.0 1.0 1.0 | — — — | μs μs V/ μs |
| Gain = 1, $R_1 = 10$ k Ω , $R_2 = 10$ k Ω , $R_3 = 5.0$ k Ω | t_f t_{pd} dV_{out}/dt (3) | — | 0.6 0.38 0.8 | — — — | — | 0.6 0.38 0.8 | — — — | μs μs V/ μs |
| Average Temperature Coefficient of Input Offset Voltage ($R_S = 50$ Ω , $T_A = T_{low}$ (1) to T_{high} (2)) ($R_S = 10$ k Ω , $T_A = T_{low}$ (1) to T_{high} (2)) | $ TC_{V_{io}} $ | — | 3.0 6.0 | — — | — | 3.0 6.0 | — — | $\mu\text{V}/^\circ\text{C}$ |
| Average Temperature Coefficient of Input Offset Current ($T_A = T_{low}$ (1) to T_{high} (2)) | $ TC_{I_{io}} $ | — | 50 | — | — | 50 | — | $\text{pA}/^\circ\text{C}$ |
| DC Power Dissipation (Power Supply = ± 15 V, $V_O = 0$) | P_D | — | 50 | 85 | — | 50 | 85 | mW |
| Positive Supply Sensitivity (V^- constant) | S^+ | — | 30 | 150 | — | 30 | 150 | $\mu\text{V}/\text{V}$ |
| Negative Supply Sensitivity (V^+ constant) | S^- | — | 30 | 150 | — | 30 | 150 | $\mu\text{V}/\text{V}$ |
| Power Bandwidth ($A_V = 1$, $R_L = 2.0$ k Ω , THD = 5%, $V_O = 20$ V _{p-p}) | PBW | — | 10 | — | — | 10 | — | kHz |

(1) $T_{low} = 0^\circ\text{C}$ for MC1741C
 $= -55^\circ\text{C}$ for MC1741

(2) $T_{high} = +75^\circ\text{C}$ for MC1741C
 $= +125^\circ\text{C}$ for MC1741

(3) $dV_{out}/dt =$ Slew Rate

(4) Plastic package offered in limited temperature range only.

TYPICAL CHARACTERISTICS

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 2 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

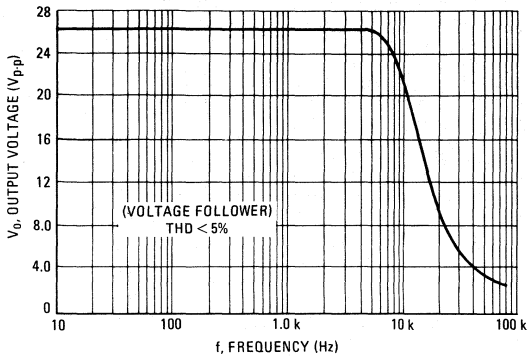


FIGURE 3 – OPEN LOOP FREQUENCY RESPONSE

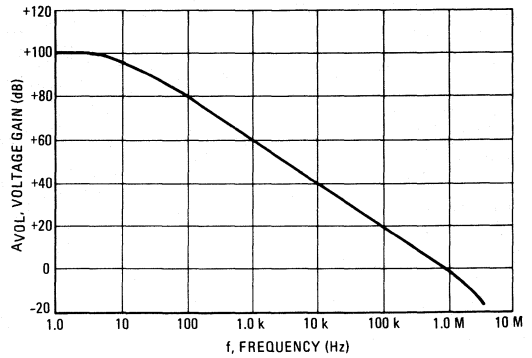


FIGURE 4 – OUTPUT NOISE versus SOURCE RESISTANCE

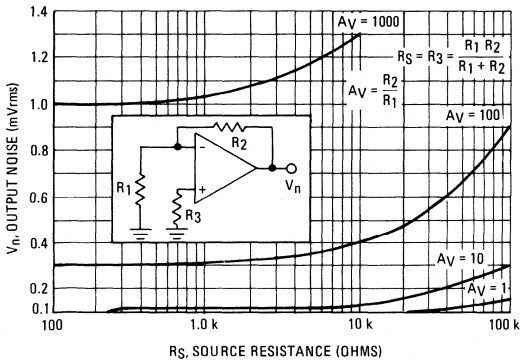
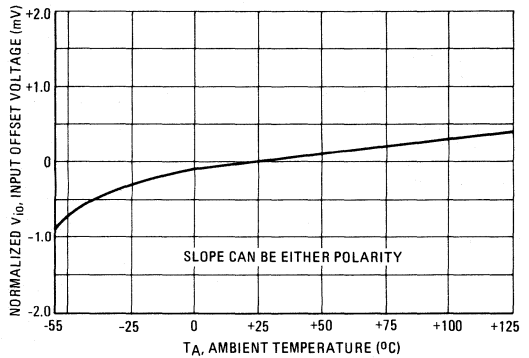


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE



7

FIGURE 6 – INPUT OFFSET CURRENT versus TEMPERATURE

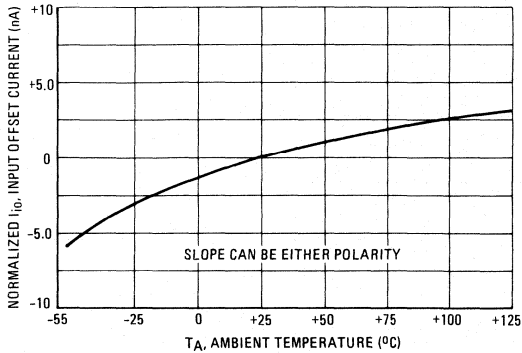


FIGURE 7 – INPUT BIAS CURRENT versus TEMPERATURE

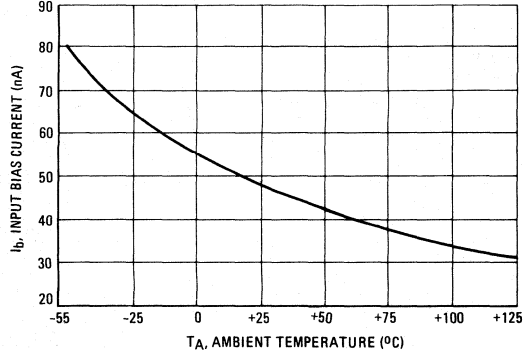


FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

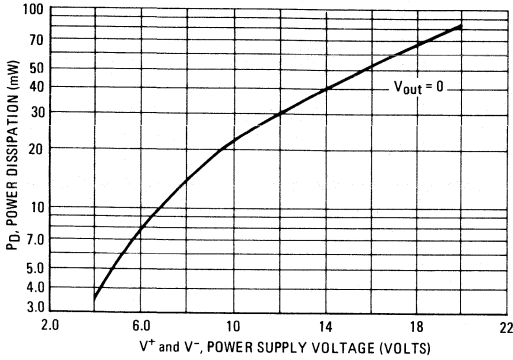


FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

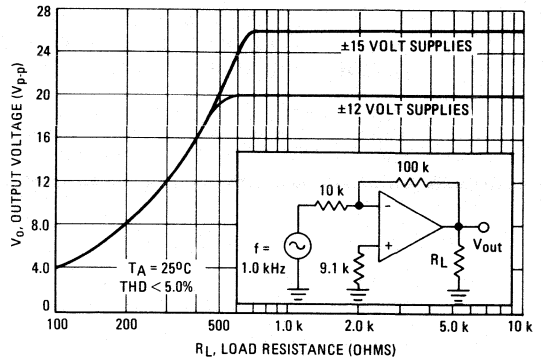
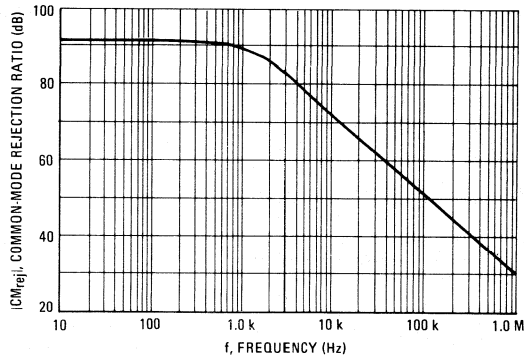


FIGURE 10 – COMMON-MODE REJECTION RATIO versus FREQUENCY



MC1747L MC1747CL

OPERATIONAL AMPLIFIER

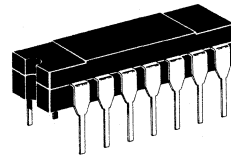
DUAL MC1741 INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. The MC1747L and MC1747CL are functionally, electrically, and pin-for-pin equivalent to the $\mu A747$ and $\mu A747C$ respectively.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch-Up
- Offset Voltage Null Capability

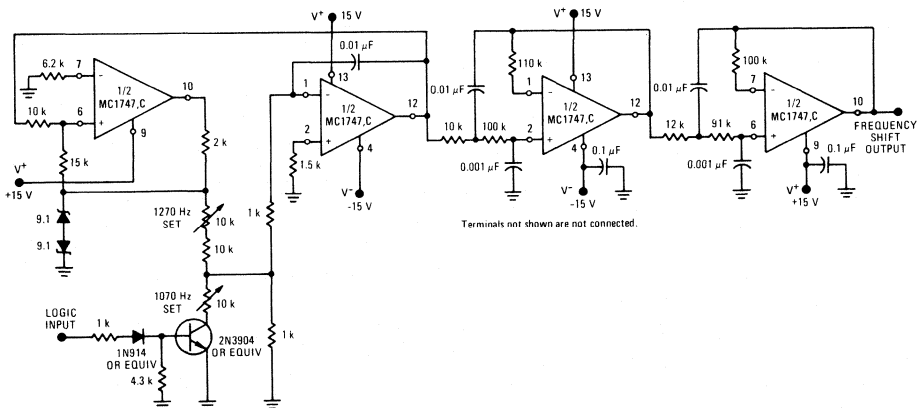
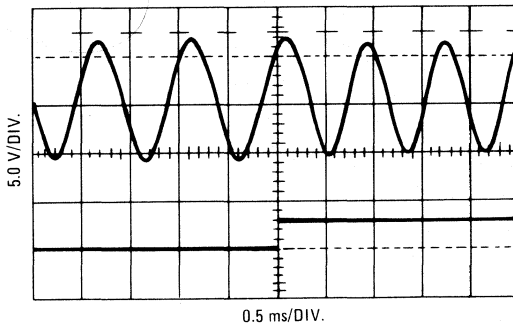
(DUAL MC1741) DUAL OPERATIONAL AMPLIFIER

MONOLITHIC SILICON
INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 - TYPICAL FREQUENCY-SHIFT
KEYER TONE GENERATOR



See Packaging Information Section for outline dimensions.

MC1747L, MC1747CL (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | MC1747L | MC1747CL | Unit |
|---|----------------------------------|-------------|-------------|-------------|
| Power Supply Voltage | V ⁺ V ⁻ | +22 -22 | +18 -18 | Vdc |
| Differential Input Signal ① | V _{in} | ± 30 | | Volts |
| Common-Mode Input Swing ② | CMV _{in} | ± 15 | | Volts |
| Output Short Circuit Duration | t _S | Continuous | | |
| Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T _A = +60°C | P _D | 750 6.0 | | mW mW/°C |
| Voltage (Measurement between Offset Null and V ⁻) | | ± 0.5 | | Volts |
| Operating Temperature Range | T _A | -55 to +125 | 0 to +75 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V⁺ = +15 Vdc, V⁻ = -15 Vdc, T_A = +25°C unless otherwise noted)

| Characteristics | Symbol | MC1747L | | | MC1747CL | | | Unit |
|---|---|------------------|------------------|--------------------|------------------|-------------------|-------------------|-----------------|
| | | Min | Typ | Max | Min | Typ | Min | |
| Input Bias Current T _A = +25°C T _A = T _{high} ③ T _A = T _{low} ③ | I _b | — | 80 30 300 | 500 500 1500 | — | 80 30 30 | 500 800 800 | nAdc |
| Input Offset Current T _A = +25°C T _A = T _{high} T _A = T _{low} | I _{io} | — | 20 7.0 85 | 200 200 500 | — | 20 7.0 7.0 | 200 300 300 | nAdc |
| Input Offset Voltage (R _S ≤ 10 kΩ) T _A = +25°C T _A = T _{low} to T _{high} | V _{io} | — | 1.0 1.0 | 5.0 6.0 | — | 1.0 1.0 | 6.0 7.5 | mVdc |
| Offset Voltage Adjustment Range | | — | ± 15 | — | — | ± 15 | — | mV |
| Differential Input Impedance (Open-loop, f = 20 Hz) Parallel Input Resistance Parallel Input Capacitance | R _p C _p | 0.3 | 2.0 | — | 0.3 | 2.0 | — | Megohms pF |
| Common-Mode Input Voltage Swing T _{low} ≤ T _A ≤ T _{high} | CMV _{in} | ± 12 | ± 13 | — | ± 12 | ± 13 | — | Volts |
| Common-Mode Rejection Ratio (R _S = 10 kΩ) T _{low} ≤ T _A ≤ T _{high} | CM _{rej} | 70 | 90 | — | 70 | 90 | — | dB |
| Open-Loop Voltage Gain T _A = +25°C T _A = T _{low} to T _{high} } (V _o = ± 10 V, R _L = 2.0 kΩ) | AVOL | 50,000 25,000 | 200,000 — | — | 25,000 15,000 | 200,000 — | — | Volts |
| Transient Response (Unity Gain) (V _{in} = 20 mV, R _L = 2.0 kΩ, C _L ≤ 100 pF) Rise Time Overshoot Percentage | t _r | — | 0.3 5.0 | — | — | 0.3 5.0 | — | μs % |
| Slew Rate (Unity Gain) | dV _o /dt | — | 0.5 | — | — | 0.5 | — | V/μs |
| Output Impedance | Z _o | — | 75 | — | — | 75 | — | ohms |
| Short-Circuit Output Current | I _{sc} | — | 25 | — | — | 25 | — | mAdc |
| Channel Separation | | — | 120 | — | — | 120 | — | dB |
| Output Voltage Swing (T _{low} ≤ T _A ≤ T _{high}) R _L = 10 kΩ R _L = 2.0 kΩ | V _o | ± 12 ± 10 | ± 14 ± 13 | — | ± 12 ± 10 | ± 14 ± 13 | — | V _{pk} |
| Power Supply Sensitivity (T _{low} to T _{high}) V ⁻ = Constant, R _S ≤ 10 kΩ V ⁺ = Constant, R _S ≤ 10 kΩ | S ⁺ S ⁻ | — | 30 30 | 150 150 | — | 30 30 | 150 150 | μV/V |
| Power Supply Current (each amplifier) T _A = +25°C T _A = T _{low} T _A = T _{high} | I _D ⁺ , I _D ⁻ | — | 1.7 20 1.5 | 2.8 3.3 2.5 | — | 1.7 2.0 2.0 | 2.8 3.3 3.3 | mAdc |
| DC Power Dissipation (each amplifier) T _A = +25°C T _A = T _{low} T _A = T _{high} | P _D | — | 50 60 45 | 85 100 75 | — | 50 60 60 | 85 100 100 | mW |

- ① For supply voltages of less than ± 15 V, the maximum differential input voltage is equal to ± (V⁺ + |V⁻|).
 ② For supply voltages of less than ± 15 V, the maximum input voltage is equal to the supply voltage (+V⁺, -|V⁻|).
 ③ T_{low}: 0°C for MC1747CL
 -55°C for MC1747L
 T_{high}: +75°C for MC1747CL
 +125°C for MC1747L

MC1747L, MC1747CL (continued)

FIGURE 2 – CIRCUIT SCHEMATIC

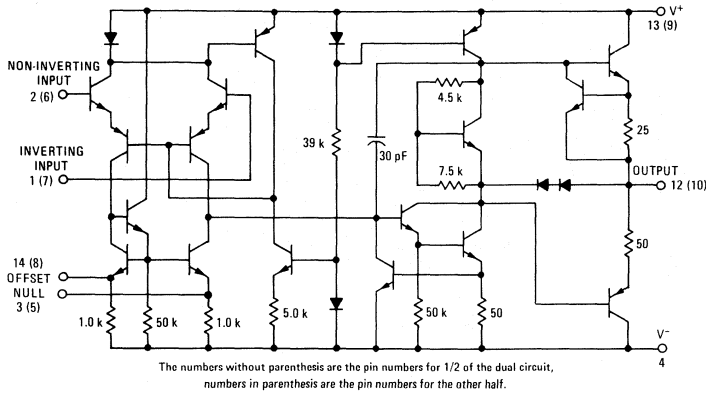
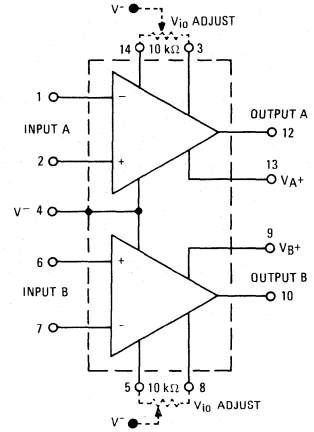


FIGURE 3 – EQUIVALENT CIRCUIT WITH OFFSET ADJUST



TYPICAL CHARACTERISTICS

($V^+ = +15 \text{ Vdc}$, $V^- = -15 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus POWER-SUPPLY VOLTAGE

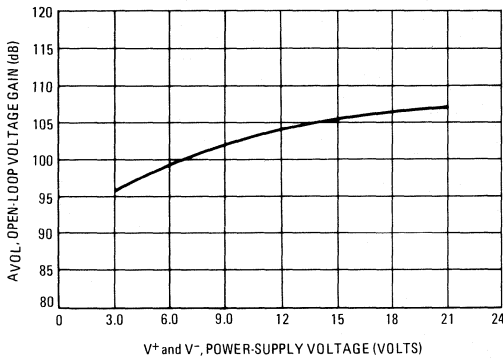


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

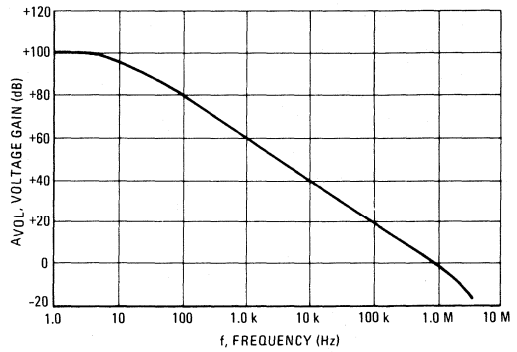


FIGURE 6 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

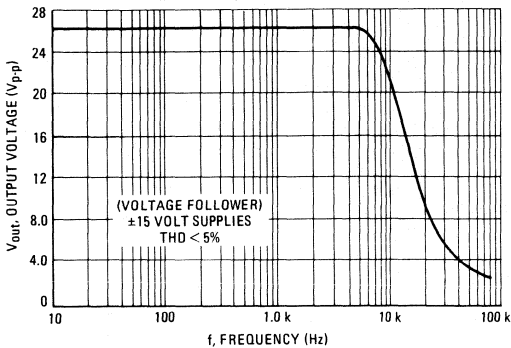
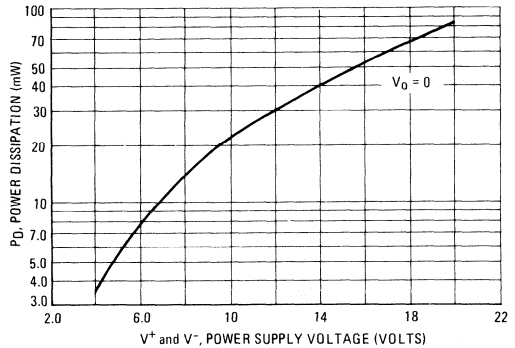


FIGURE 7 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 8 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

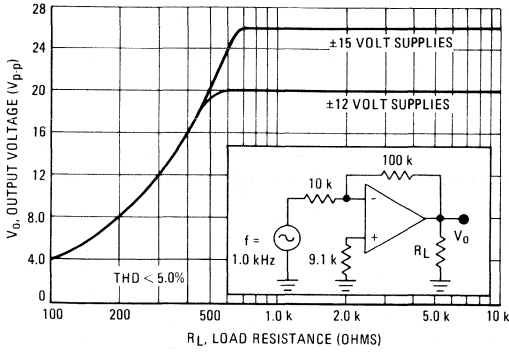


FIGURE 9 – OUTPUT NOISE versus SOURCE RESISTANCE

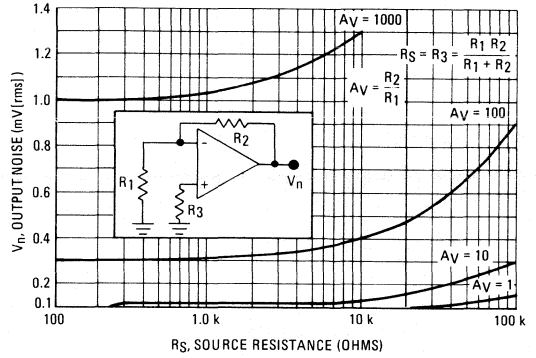
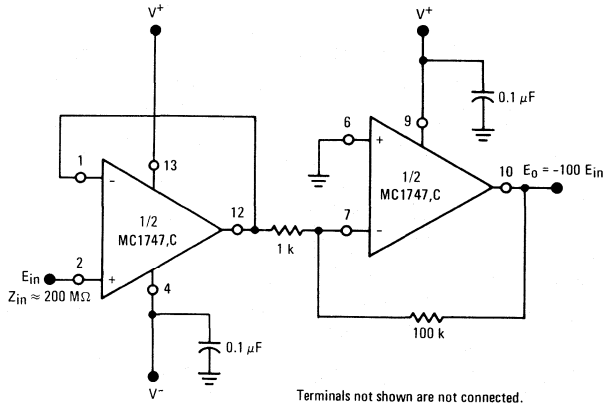


FIGURE 10 – HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER



MC1748G
MC1748CG

HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Noncompensated MC1741G
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

METAL PACKAGE
CASE 601
TO-99

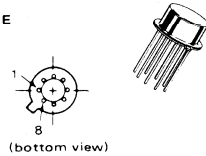


FIGURE 1 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

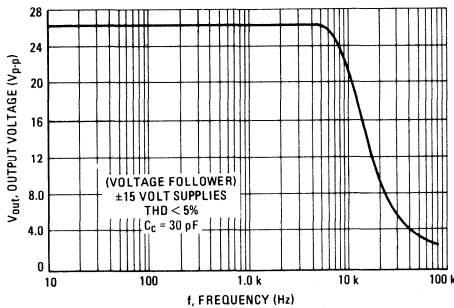


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

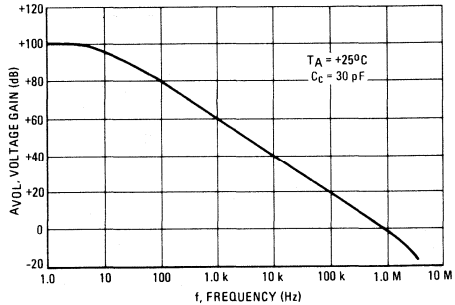


FIGURE 3 – CIRCUIT SCHEMATIC

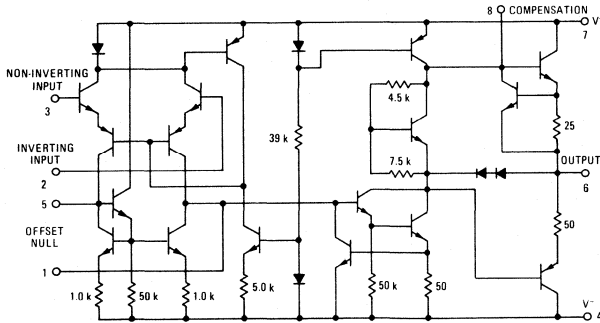
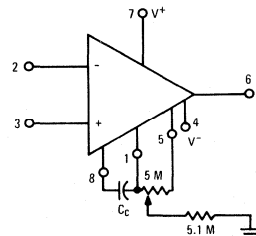


FIGURE 4 – OFFSET ADJUST AND FREQUENCY COMPENSATION



See Packaging Information Section for outline dimensions.
See current MCC1748/1748C data sheet for standard linear chip information.

MC1748G, MC1748CG (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | MC1748G | MC1748CG | Unit |
|---|----------------------------------|-------------|-------------|-------------|
| Power Supply Voltage | V ⁺ V ⁻ | +22 -22 | +18 -18 | Vdc |
| Differential Input Signal | V _{in} | ±30 | | Volts |
| Common-Mode Input Swing ① | CMV _{in} | ±15 | | Volts |
| Output Short Circuit Duration | t _S | Continuous | | |
| Power Dissipation (Package Limitation) Derate above T _A = +25°C | P _D | 680 4.6 | | mW mW/°C |
| Operating Temperature Range | T _A | -55 to +125 | 0 to +75 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V⁺ = +15 Vdc, V⁻ = -15 Vdc, T_A = +25°C unless otherwise noted)

| Characteristics | Symbol | MC1748G | | | MC1748CG | | | Unit |
|--|--|------------------|-------------------|--------------|------------------|-------------------|--------------|------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current T _A = +25°C T _A = T _{low} to T _{high} ② | I _b | - | 0.08 0.3 | 0.5 1.5 | - | 0.08 - | 0.5 0.8 | μAdc |
| Input Offset Current T _A = +25°C T _A = T _{low} to T _{high} | I _{io} | - | 0.02 0.08 | 0.2 0.5 | - | 0.02 - | 0.2 0.3 | μAdc |
| Input Offset Voltage (R _S ≤ 10 k Ω) T _A = +25°C T _A = T _{low} to T _{high} | V _{io} | - | 1.0 - | 5.0 6.0 | - | 1.0 - | 6.0 7.5 | mVdc |
| Differential Input Impedance (Open-Loop, f = 20 Hz) Parallel Input Resistance Parallel Input Capacitance | R _p C _p | 0.3 - | 2.0 1.4 | - - | 0.3 - | 2.0 1.4 | - - | Megohm pF |
| Common-Mode Input Impedance (f = 20 Hz) | Z _(in) | - | 200 | - | - | 200 | - | Megohms |
| Common-Mode Input Voltage Swing | CMV _{in} | ±12 | ±13 | - | ±12 | ±13 | - | V _{pk} |
| Common-Mode Rejection Ratio (f = 100 Hz) | CM _{rej} | 70 | 90 | - | 70 | 90 | - | dB |
| Open-Loop Voltage Gain, (V _O = ±10 V, R _L = 2.0 k ohms) T _A = +25°C T _A = T _{low} to T _{high} | A _{VOL} | 50,000 25,000 | 200,000 - | - - | 20,000 15,000 | 200,000 - | - - | V/V |
| Step Response (V _{in} = 20 mV, C _c = 30 pF, R _L = 2 k Ω, C _L = 100 pF) Rise Time Overshoot Percentage Slew Rate | t _r dV _{out} /dt | - | 0.3 5.0 0.8 | - - - | - - - | 0.3 5.0 0.8 | - - - | μs % V/μs |
| Output Impedance (f = 20 Hz) | Z _{out} | - | 75 | - | - | 75 | - | ohms |
| Short-Circuit Output Current | I _{SC} | - | 25 | - | - | 25 | - | mA _{dc} |
| Output Voltage Swing (R _L = 10 k ohms) R _L = 2 k ohms (T _A = T _{low} to t _{high}) | V _O | ±12 ±10 | ±14 ±13 | - - | ±12 ±10 | ±14 ±13 | - - | V _{pk} |
| Power Supply Sensitivity V ⁻ = constant, R _S ≤ 10 k ohms V ⁺ = constant, R _S ≤ 10 k ohms | S ⁺ S ⁻ | - | 30 30 | 150 150 | - | 30 30 | 150 150 | μV/V |
| Power Supply Current | I _D ⁺ I _D ⁻ | - | 1.67 1.67 | 2.83 2.83 | - | 1.67 1.67 | 2.83 2.83 | mA _{dc} |
| DC Quiescent Power Dissipation (V _O = 0) | P _D | - | 50 | 85 | - | 50 | 85 | mW |

① For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage.

② T_{low}: 0°C for MC1748CG
-55°C for MC1748G
T_{high}: +75°C for MC1748CG
+125°C for MC1748G

MC3301P

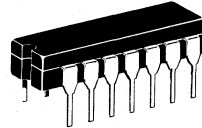
OPERATIONAL AMPLIFIER

MONOLITHIC QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER FOR AUTOMOTIVE APPLICATIONS

These internally compensated operational amplifiers are designed specifically for single positive power supply applications found in automotive and consumer electronics. Each MC3301P contains four independent amplifiers — making it ideal for automotive safety, pollution, and comfort controls. Some typical applications are tachometer, voltage regulator, logic circuits, power control and other similar usages.

- Wide Operating Temperature Range — -40 to +85°C
- Single-Supply Operation — +4.0 to +28 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth — 4.0 MHz typical
- Low Input Bias Current — 50 nA typical
- High Open-Loop Gain — 2000 V/V typical

MONOLITHIC QUAD OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT EPITAXIAL PASSIVATED



PLASTIC PACKAGE
CASE 646
(TO-116)

FIGURE 1 — EQUIVALENT CIRCUIT

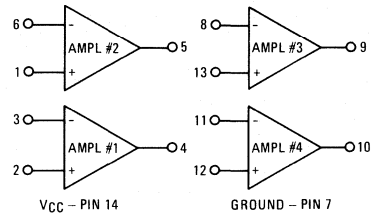


FIGURE 2 — SMALL-SIGNAL TRANSIENT RESPONSE

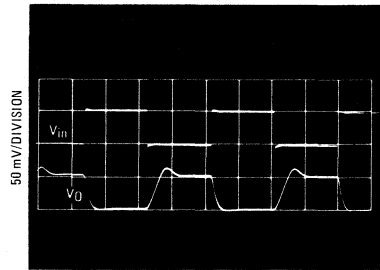
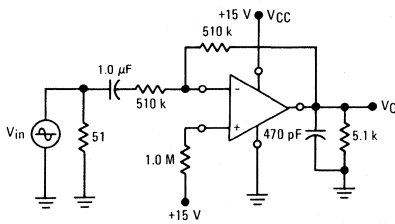


FIGURE 3 — INVERTING AMPLIFIER

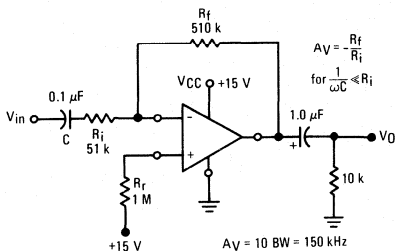
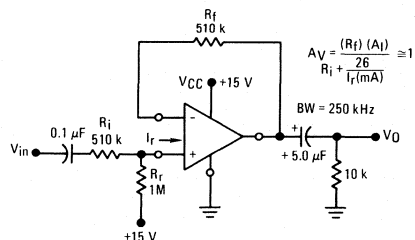


FIGURE 4 — NONINVERTING AMPLIFIER



MC3301P (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---------------------|-------------|-------------|
| Power Supply Voltage | V _{CC} | +28 | Vdc |
| Noninverting Input Current | I _r | 5.0 | mA |
| Sink Current | I _{sink} | 50 | mA |
| Source Current | I _{source} | 50 | mA |
| Power Dissipation (Package Limitation) Derate above T _A = +25°C | P _D | 625 5.0 | mW mW/°C |
| Operating Temperature Range | T _A | -40 to +85 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS [V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C (each amplifier) unless otherwise noted]

| Characteristic | Fig.No. | Note | Symbol | Min | Typ | Max | Unit |
|---|---------|------|---|----------------|---------------------|---------------|---------|
| Open-Loop Voltage Gain T _A = +25°C -40°C ≤ T _A ≤ +85°C | 5 | | A _{vol} | 1000 — | 2000 1600 | — — | V/V |
| Quiescent Power Supply Current (Total for four amplifiers) Noninverting inputs open Noninverting inputs grounded | 6 | 1 | I _{DO} I _{DG} | — — | 6.9 7.8 | 10 14 | mAdc |
| Input Bias Current, R _L = ∞ T _A = +25°C -40°C ≤ T _A ≤ +85°C | 7 | 2 | I _{IB} | — — | 50 100 | 300 — | nAdc |
| Current Mirror Gain (I _r = 200 μAdc) | 7 | 3 | A _I | 0.80 | 0.98 | 1.16 | A/A |
| Current Mirror Gain Drift -40°C ≤ T _A ≤ +85°C | | | | — | ±2.5 | — | % |
| Output Current Source Capability (V _{OH} = 0.4 Vdc) (V _{OH} = 9.0 Vdc) Sink Capability (V _{OL} = 0.4 Vdc) | 8 | | I _{source} I _{sink} | 3.0 0.5 | 10 0.87 | — — | mAdc |
| Output Voltage High Voltage Low Voltage (Inverting Input Driven) (Noninverting Input Driven) | 6 | | V _{OH} V _{OL(inv)} V _{OL(non)} | 13.5 — — | 14.2 0.03 0.6 | — 0.1 — | Vdc |
| Input Resistance (Inverting input only) | | | R _{in} | 0.1 | 1.0 | — | Meg Ω |
| Slew Rate (C _L = 100 pF, R _L = 5.0 k) | | | SR | — | 0.6 | — | V/μs |
| Unity Gain Bandwidth | | 4 | BW | — | 4.0 | — | MHz |
| Phase Margin | | 4 | φ _m | — | 70 | — | Degrees |
| Power Supply Rejection (f = 100 Hz) | | | PSSR | — | 55 | — | dB |
| Channel Separation (f = 1.0 kHz) | | | e _{o1} /e _{o2} | — | 65 | — | dB |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

NOTES:

- The quiescent current drain will increase approximately 0.3 mA for each inverting or noninverting input that is grounded.
- Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" — as with a conventional IC operational amplifier. As such this

- input does not have a requirement for input bias current.
- Current mirror gain is defined as the current demanded at the inverting input divided by the current into the noninverting input.
- Bandwidth and phase margin are defined with respect to the voltage gain from the inverting input to the output.

TYPICAL CHARACTERISTICS
 ($V_{CC} = +15\text{ Vdc}$, $R_L = 5.0\text{ k}\Omega$, $T_A = +25^\circ\text{C}$
 [each amplifier] unless otherwise noted.)

FIGURE 5 – OPEN-LOOP VOLTAGE GAIN

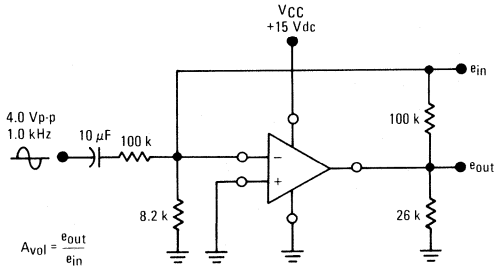


FIGURE 6 – QUIESCENT POWER SUPPLY CURRENT

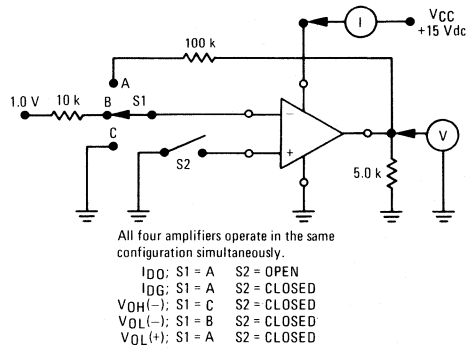


FIGURE 7 – INPUT BIAS CURRENT AND CURRENT MIRROR GAIN

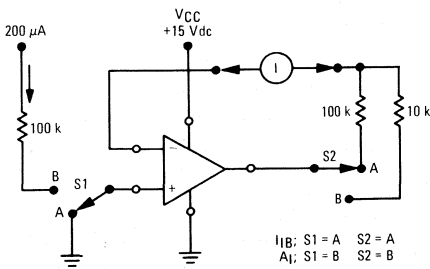
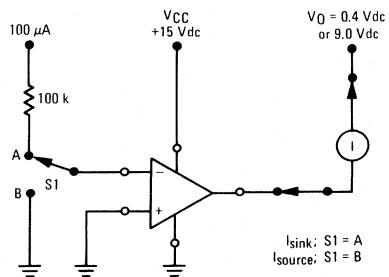


FIGURE 8 – OUTPUT CURRENT



TYPICAL CHARACTERISTICS
 ($V_{CC} = +15\text{ Vdc}$, $R_L = 5.0\text{ k}\Omega$, $T_A = +25^\circ\text{C}$
 [each amplifier] unless otherwise noted.)

FIGURE 9 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

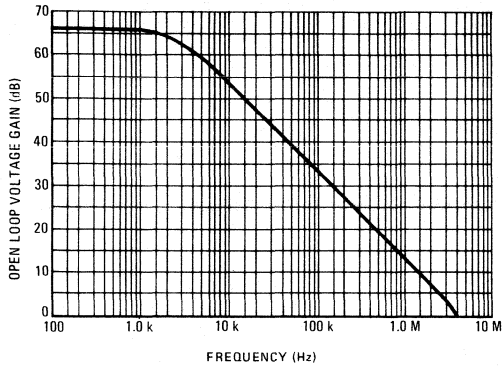


FIGURE 10 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

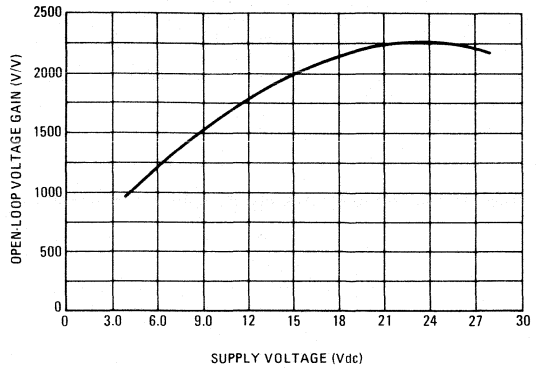


FIGURE 11 – OUTPUT RESISTANCE versus FREQUENCY

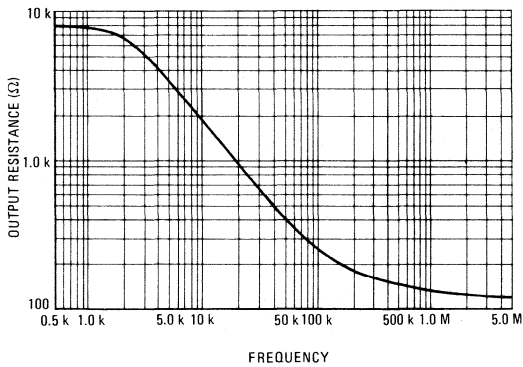


FIGURE 12 – SUPPLY CURRENT versus SUPPLY VOLTAGE

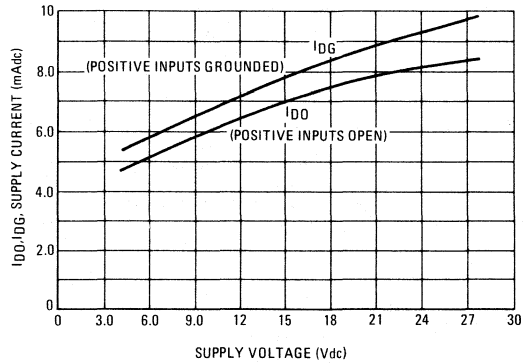


FIGURE 13 – LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

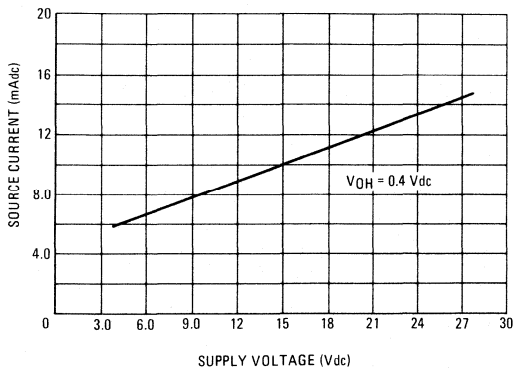
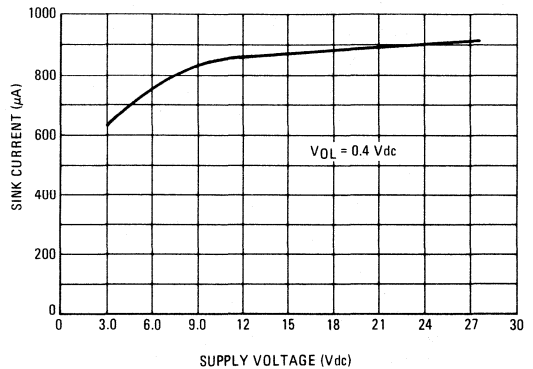


FIGURE 14 – LINEAR SINK CURRENT versus SUPPLY VOLTAGE



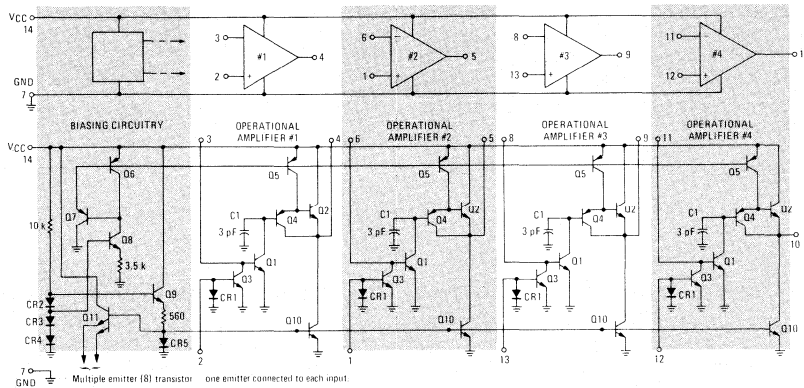
OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased class A by the current source I_2 . The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled

linear operation at the output. The sink current of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 volt resulting in an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18 on the following page. No external compensation is required.

FIGURE 15
BLOCK DIAGRAM



A noninverting input is obtained by adding a current mirror as shown in Figure 17. Essentially all current which enters the non-inverting input, I_r , flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_r . Since the alpha

current gain of Q3 ≈ 1 , its collector current is approximately equal to I_r also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 16 – A BASIC GAIN STAGE

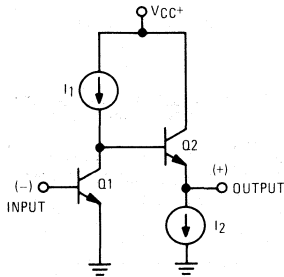
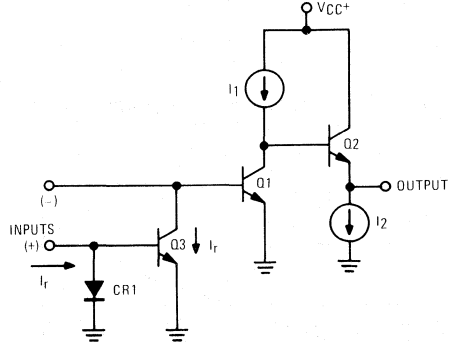


FIGURE 17 – OBTAINING A NONINVERTING INPUT



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19, see next page. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor

Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 15) provides circuit protection from signals that are negative with respect to ground.

7

OPERATION AND APPLICATIONS (continued)

FIGURE 18 — A BASIC OPERATIONAL AMPLIFIER

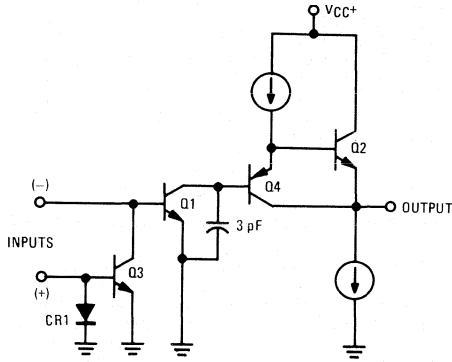
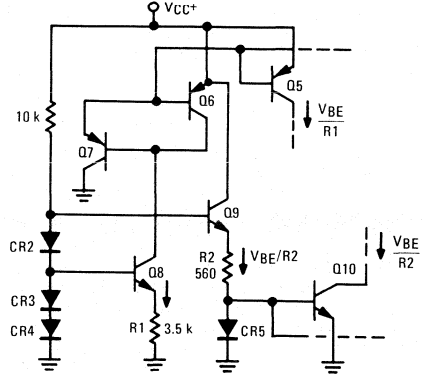


FIGURE 19 — BIASING CIRCUITRY



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing

A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4 (see the first page of this specification). The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the non-inverting input current be in the 10 μ A to 200 μ A range.

B. V_{CC} Reference Voltage (see Figures 3 and 4)

The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r , allowing the input current, I_r , to be within the range of 10 μ A to 200 μ A. Choosing the feedback resistor, R_f , to be equal to $\frac{1}{2} R_r$ will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows the maximum dynamic range of the output voltage.

C. Reference Voltage other than V_{CC} (see Figure 20)

The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC} . By setting $R_f = R_r$, (still keeping I_r between 10 μ A and 200 μ A) the output dc level will be equal to V_r . The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_1)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_1\right) \phi$$

where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_1 is the current mirror gain.

2. Gain Determination

A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

FIGURE 20 — INVERTING AMPLIFIER WITH ARBITRARY REFERENCE

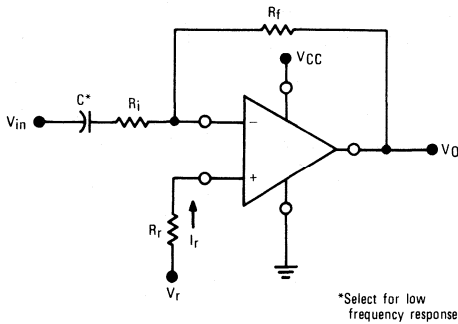
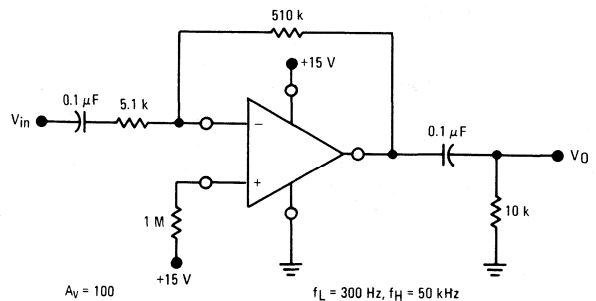


FIGURE 21 — INVERTING AMPLIFIER WITH $A_v = 100$ AND $V_r = V_{CC}$



NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i , in the same manner as for a conventional operational amplifier:

$$A_v = - \frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 4.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 400 kHz with 20 dB of closed loop gain or 40 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

B. Noninverting Amplifier

The MC3301P may be used in the noninverting mode (see Figure 4, first page). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes. The noninverting ac gain expression is given by:

$$A_v = \frac{(R_f)(A_1)}{R_i + \frac{26}{I_r}(\text{mA})}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For $R_f = 510 \text{ k}\Omega$ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 22 – TACHOMETER CIRCUIT

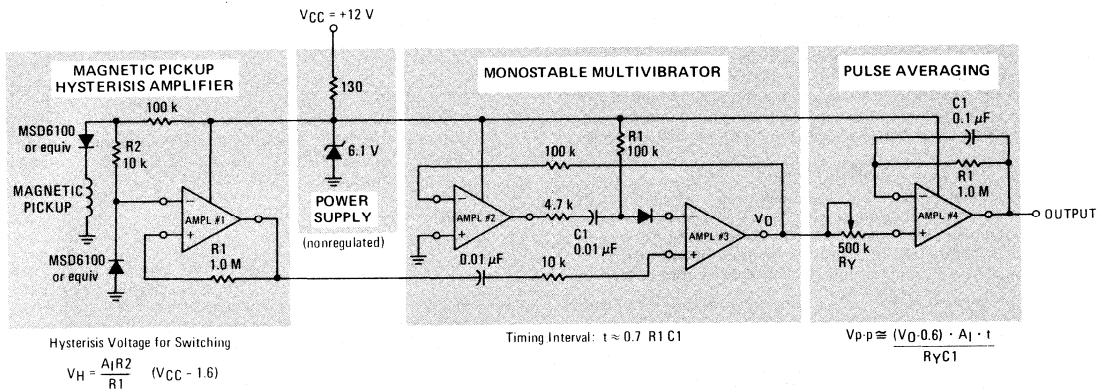


FIGURE 23 – VOLTAGE REGULATOR

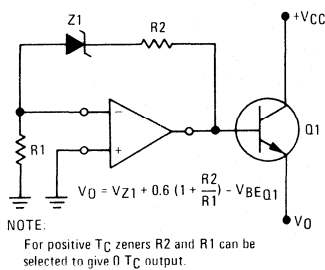
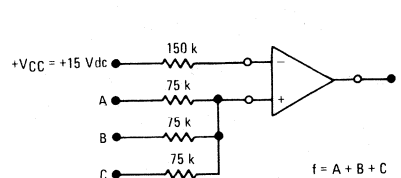


FIGURE 24 – LOGIC "OR" GATE



TYPICAL APPLICATIONS (continued)

FIGURE 25 – LOGIC "NAND" GATE (Large Fan-In)

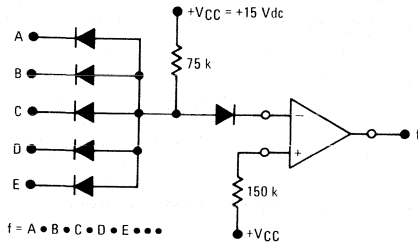


FIGURE 26 – LOGIC "NOR" GATE

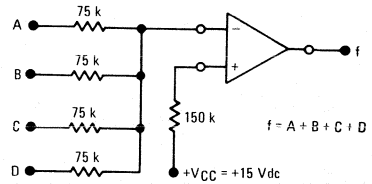


FIGURE 27 – R-S FLIP-FLOP

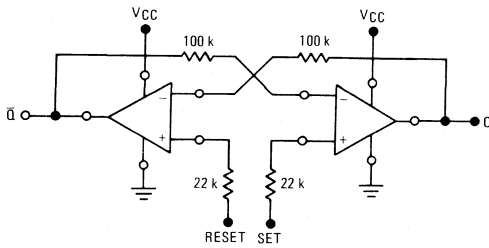


FIGURE 28 – ASTABLE MULTIVIBRATOR

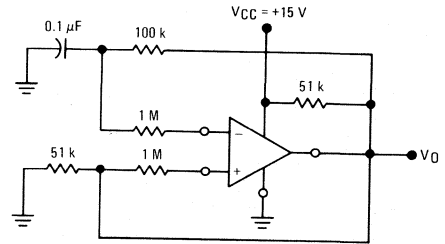


FIGURE 29 – POSITIVE-EDGE DIFFERENTIATOR

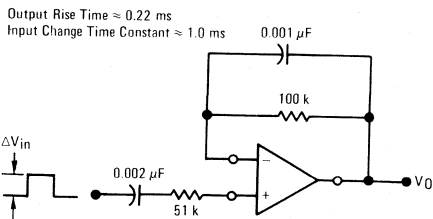
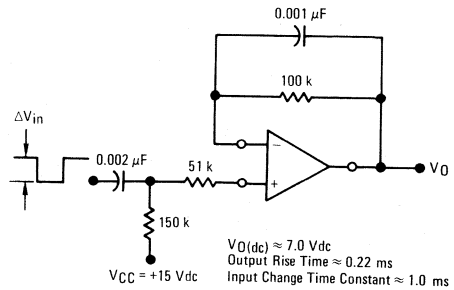


FIGURE 30 – NEGATIVE-EDGE DIFFERENTIATOR



MC3302P

QUAD COMPARATOR

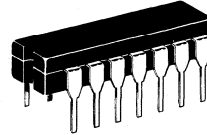
Product Preview

MONOLITHIC QUAD SINGLE-SUPPLY COMPARATOR

These comparators are designed specifically for single positive-power-supply Consumer and Industrial electronic applications. Each MC3302P contains four independent comparators – suiting it ideally for usages requiring high density and low-cost.

- Wide Operating Temperature Range – -40 to +85°C
- Single-Supply Operation – +2.0 to +28 Vdc
- Differential Input Voltage = $\pm V_{CC}$
- Compare Voltages at Ground Potential
- M TTL Compatible
- Low Current Drain – 600 μA @ $V_{CC} = 5.0$ Vdc
- Outputs can be Connected to Give the Implied AND Function

MONOLITHIC QUAD COMPARATOR INTEGRATED CIRCUIT EPITAXIAL PASSIVATED



CASE 646
TO-116
PLASTIC PACKAGE

MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|--|-----------|-------------------|----------------------|
| Power Supply Range | V_{CC} | +2.0 to +28 | Vdc |
| Output Sink Current (See Note 1) | I_O | 20 | mA |
| Different Input Voltage | V_{IDR} | $\pm V_{CC}$ | Vdc |
| Common-Mode Input Voltage Range (See Note 2) | V_{ICR} | -0.3 to $+V_{CC}$ | Vdc |
| Power Dissipation (Package Limitation) Derate above $T_A = +25^\circ C$ | P_D | 625 5.0 | mW mW/ $^\circ C$ |
| Operating Temperature Range | T_A | -40 to +85 | $^\circ C$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ C$ |

- Note 1. Requires an external resistor, R_L , to limit current below maximum rating.
 Note 2. If either (+) or (-) inputs of any comparator go more than several tenths of a volt below ground, a parasitic transistor turns "on" causing high input current and possible faulty outputs.

FIGURE 1 – EQUIVALENT CIRCUIT

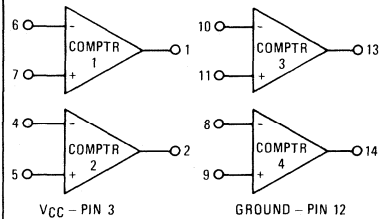
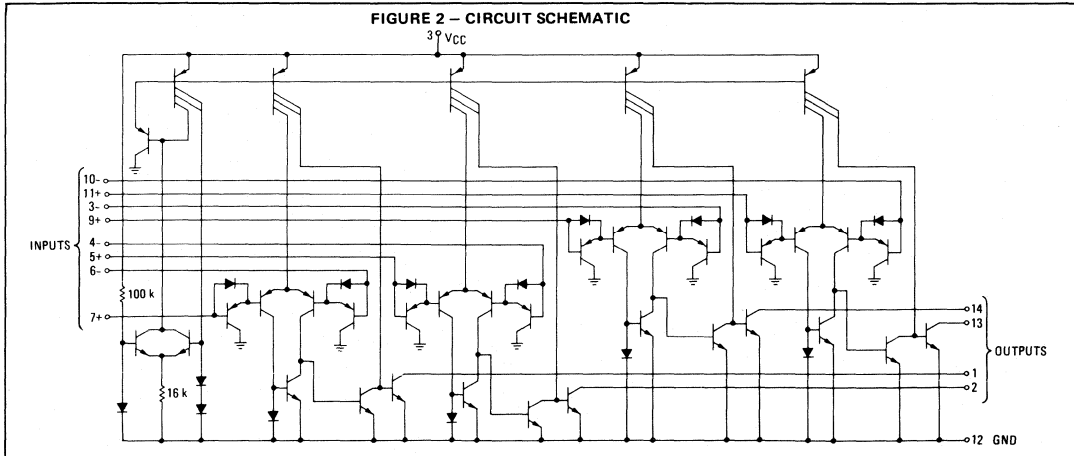


FIGURE 2 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MC3302P (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ [each comparator] unless otherwise noted.)

| Characteristic | Fig. No. | Symbol | Min | Typ | Max | Unit |
|---|----------|------------------------|--------------|-------------------|-------------------|--------------------------------------|
| Power Supply Current (total for four comparators) $V_{CC} = 5.0\text{ V}$ $V_{CC} = 15\text{ V}$ $V_{CC} = 28\text{ V}$ } (S1 = A, S2 = A) | 3 | I_D | — | 0.6 0.7 0.8 | 1.5 1.5 1.5 | mAdc |
| Output Voltage Low ($I_O = 1.6\text{ mA}$) $V_{CC} = 5.0\text{ V}$ $V_{CC} = 15\text{ V}$ } (S1 = B, S2 = B) | 3 | V_{OL} | — | 150 150 | 400 400 | mVdc |
| Output Sink Current $T_A = -40^\circ\text{C}$, $V_{OL} = 400\text{ mV}$ | — | I_O | — | 6.0 | — | mAdc |
| Output Leakage Current V_O high, S1 = A, S2 = C | 3 | I_{off} | — | — | 10 | μAdc |
| Input Bias Current (both inputs) (S1 = A, B; S2 = A) Temperature Coefficient | 3 | I_{IB} TCI_{IB} | — | 30 0.16 | 500 — | nAdc nA/ $^\circ\text{C}$ |
| Input Offset Current Temperature Coefficient | 3 | I_{IO} TCI_{IO} | — | 3.0 0.035 | 100 — | nAdc nA/ $^\circ\text{C}$ |
| Input Offset Voltage ($V_{IO} = [V_{ref} - V_{in}]$) $V_{ref} = 1.2\text{ Vdc}$ Temperature Coefficient | 4 | V_{IO} TCV_{IO} | — | 3.0 7.0 | 10 — | mVdc $\mu\text{V}/^\circ\text{C}$ |
| Common-Mode Input Voltage Range $V_{in} = 50\text{ mVp-p}$, $V_{CC} = 28\text{ Vdc}$ | 5 | V_{ICR} | 26 | — | — | Vdc |
| Common-Mode Rejection Ratio | — | CMRR | — | 60 | — | dB |
| Differential Input Voltage Range (S1 = A, B; S2 = A) | 3 | V_{IDR} | $\pm V_{CC}$ | — | — | Vdc |
| Transconductance | — | — | — | 2.0 | — | mhos |
| Voltage Gain ($R_L = 15\text{ kilohms}$) | — | A_{vol} | — | 30,000 | — | V/V |
| Propagation Delay Time | — | t_d | — | 2.0 | — | μs |
| Slew Rate | — | t_{SR-} t_{SR+} | — | 200 50 | — | V/ μs |

Symbols conform to JEDEC Bulletin No. 1 when applicable.

TEST CIRCUITS (1/4 Circuit Shown)

FIGURE 3 – DC TEST CIRCUIT

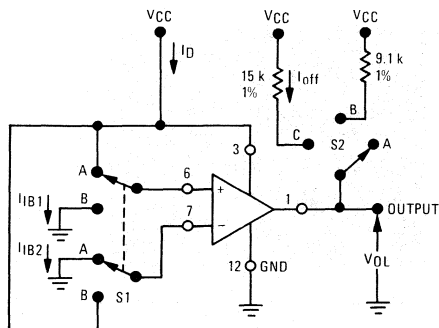


FIGURE 4 – INPUT OFFSET VOLTAGE

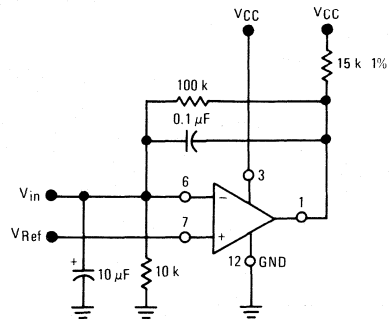
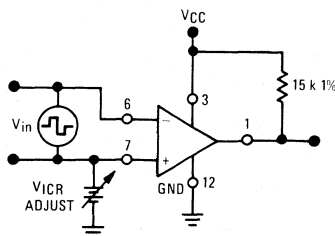


FIGURE 5 – INPUT COMMON-MODE VOLTAGE RANGE



MC3401P

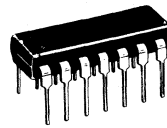
Specifications and Applications Information

MONOLITHIC QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER

These internally compensated operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each MC3401P device contains four independent amplifiers — making it ideal for applications such as active filters, multi-channel amplifiers, tachometer, oscillator and other similar usages.

- Single-Supply Operation — +5.0 Vdc to +18 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth — 5.0 MHz typical
- Low Input Bias Current — 50 nA typical
- High Open-Loop Gain — 1000 V/V minimum

MONOLITHIC QUAD OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT
EPITAXIAL PASSIVATED



PLASTIC PACKAGE
CASE 646
(TO-116)

FIGURE 1 — EQUIVALENT CIRCUIT

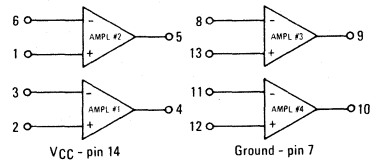
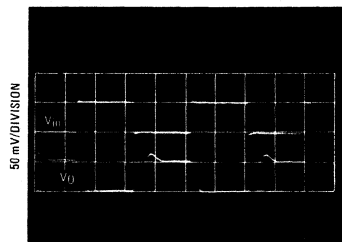
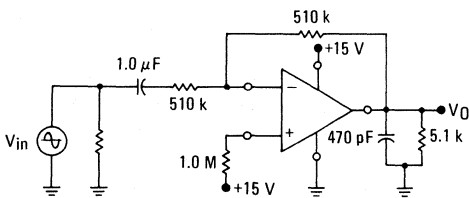


FIGURE 2 — SMALL-SIGNAL TRANSIENT RESPONSE



5.0 μs/DIVISION

FIGURE 3 — INVERTING AMPLIFIER

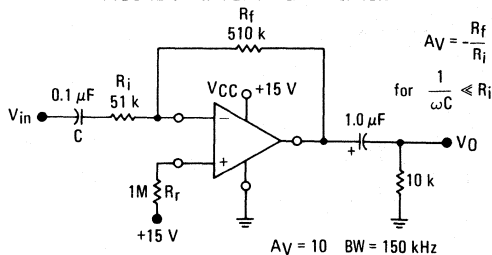
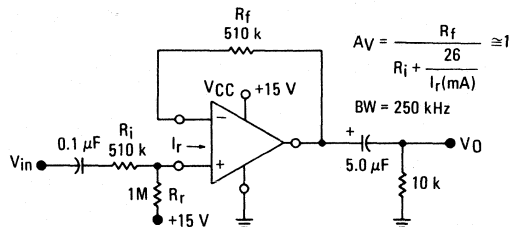


FIGURE 4 — NONINVERTING AMPLIFIER



MC3401P (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|-----------|-------------|----------------------------|
| Power Supply Voltage | V_{CC} | +18 | Vdc |
| Non-inverting Input Current | I_{in} | 5.0 | mA |
| Power Dissipation Derate above $T_A = +25^\circ\text{C}$ | P_D | 625 5.0 | mW mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | 0 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS [$V_{CC} = +15\text{ Vdc}$, $R_L = 5.0\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ (each amplifier) unless otherwise noted]

| Characteristic | Fig. No. | Note | Symbol | Min | Typ | Max | Unit |
|---|---------------|-------------|------------------------------------|-----------------|----------------------|---------------|---|
| Open-Loop Voltage Gain $T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$ | 5,9,10 | 1 | A_{vol} | 1000 800 | 2000 — | — — | V/V |
| Quiescent Power Supply Current (Total for four amplifiers) Noninverting inputs open Noninverting inputs grounded | 6,12 | 2 | I_{DO} I_{DG} | — — | 6.9 7.8 | 10 14 | mA _{dc} |
| Input Bias Current, $R_L = \infty$ $T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$ | 5 | 3 | I_{IB} | — — | 50 — | 300 500 | nA _{dc} |
| Output Current Source Capability Sink Capability | 5 13 14 | 4 | I_{source} I_{sink} | 5.0 0.5 | 10 1.0 | — — | mA _{dc} |
| Output Voltage High Voltage Low Voltage Undistorted Output Swing ($0^\circ\text{C} < T_A < +75^\circ\text{C}$) | 7 7 8 | 5 5 6 | V_{OH} V_{OL} $V_O(p-p)$ | 13.5 — 10 | 14.2 0.03 13.5 | — 0.1 — | V _{dc} V _(p-p) |
| Input Resistance | 5 | | R_{in} | 0.1 | 1.0 | — | MEG Ω |
| Slew Rate ($C_L = 100\text{ pF}$, $R_L = 5.0\text{ k}$) | | | SR | — | 0.6 | — | V/ μs |
| Unity Gain Bandwidth | | | BW | — | 5.0 | — | MHz |
| Phase Margin | | | ϕ_m | — | 70 | — | Degrees |
| Power Supply Rejection ($f = 100\text{ Hz}$) | | 7 | PSSR | — | 55 | — | dB |
| Channel Separation ($f = 1.0\text{ kHz}$) | | | e_{o1}/e_{o2} | — | 65 | — | dB |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

NOTES

- Open loop voltage gain is defined as the voltage gain from the inverting input to the output.
- The quiescent current will increase approximately 0.3 mA for each noninverting input which is grounded. Leaving the non-inverting input open causes the apparent input bias current to increase slightly (100 nA) at high temperatures.
- Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" — as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
- Sink current is specified for linear operation. When the device is used as a gate or a comparator (non-linear operation), the sink capability of the device is approximately 5.0 milliamperes.
- When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.
- Peak-to-peak restrictions are due to the variations of the quiescent dc output voltage in the standard configuration (Figure 8).
- Power supply rejection is specified at closed loop unity gain, and therefore indicates the supply rejection of both the biasing circuitry and the feedback amplifier.

SIMPLIFIED TEST CIRCUITS
 ($V_{CC} = +15\text{ Vdc}$, $R_L = 5.0\text{ k}\Omega$, $T_A = +25^\circ\text{C}$
 [each amplifier] unless otherwise noted)

FIGURE 5 – OPEN-LOOP GAIN AND INPUT RESISTANCE (INPUT BIAS CURRENT, OUTPUT CURRENT)

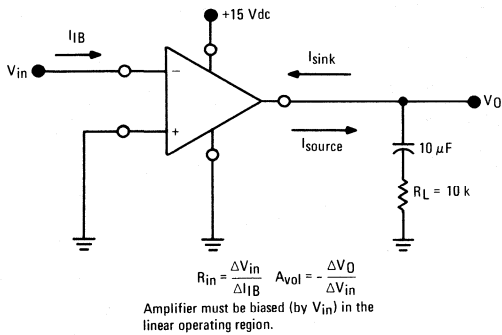


FIGURE 6 – QUIESCENT POWER SUPPLY CURRENT

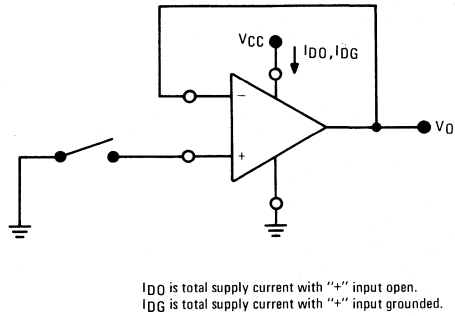


FIGURE 7 – OUTPUT VOLTAGE SWING

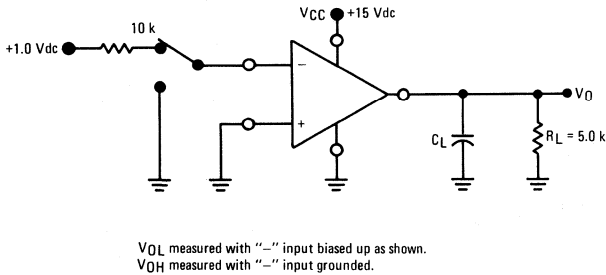
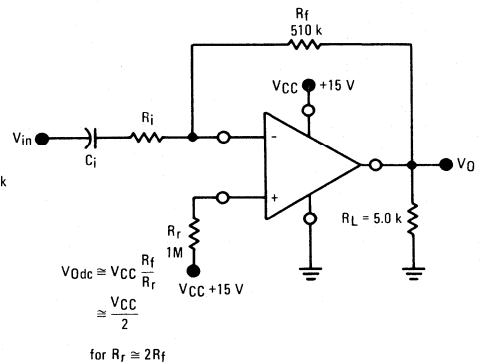


FIGURE 8 – PEAK-TO-PEAK OUTPUT VOLTAGE



TYPICAL CHARACTERISTICS
 ($V_{CC} = +15$ Vdc, $R_L = 5.0$ k Ω , $T_A = +25^\circ\text{C}$
 [each amplifier] unless otherwise noted.)

FIGURE 9 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

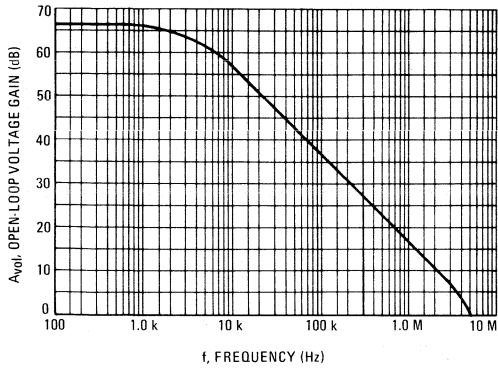


FIGURE 10 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

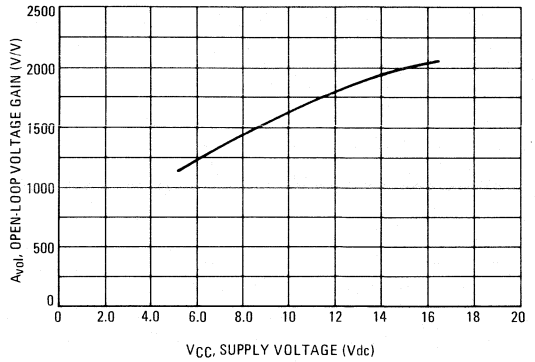


FIGURE 11 – OUTPUT RESISTANCE versus FREQUENCY

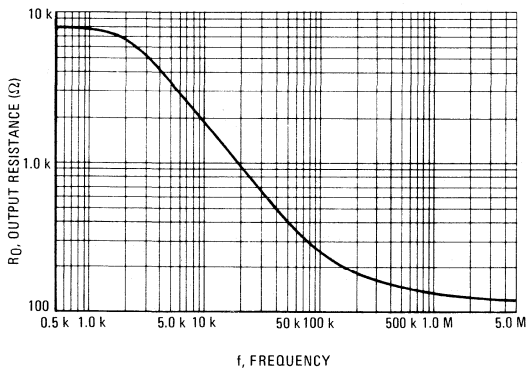


FIGURE 12 – SUPPLY CURRENT versus SUPPLY VOLTAGE

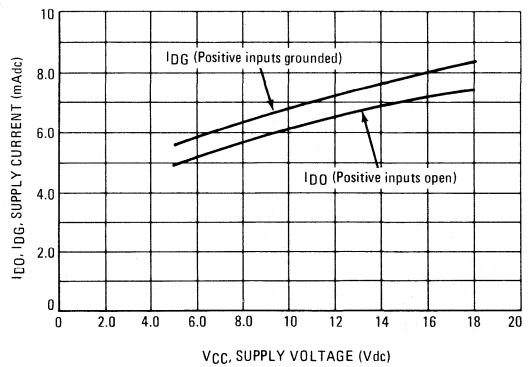


FIGURE 13 – LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

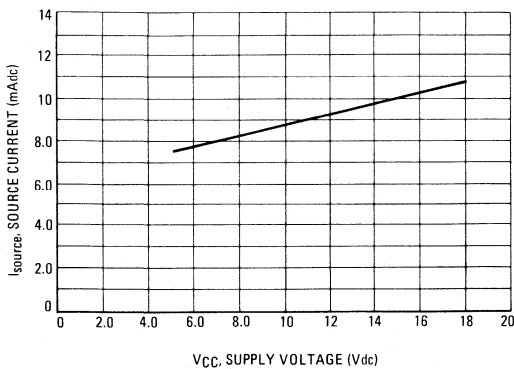
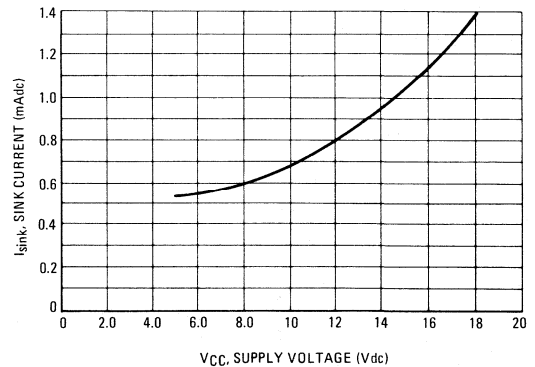


FIGURE 14 – LINEAR SINK CURRENT versus SUPPLY VOLTAGE



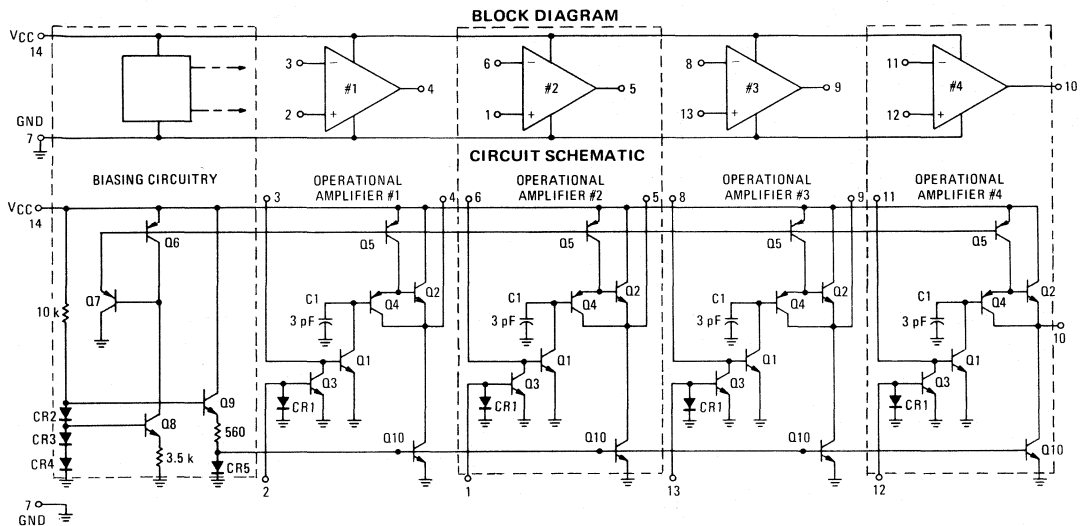
OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased class A by the current source I_2 . The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled

linear operation at the output. The sink current of the device can be forced to exceed the specified level with an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18. No external compensation is required.

FIGURE 15



A noninverting input is obtained by adding a current mirror as shown in Figure 17. Essentially all current which enters the non-inverting input, I_{in2} , flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_{in2} . Since the

alpha current gain of Q3 ≈ 1 , its collector current $\approx I_{in2}$ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 16 — A BASIC GAIN STAGE

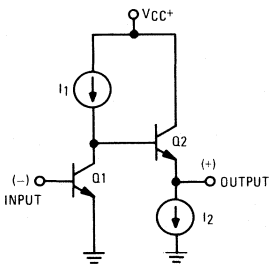
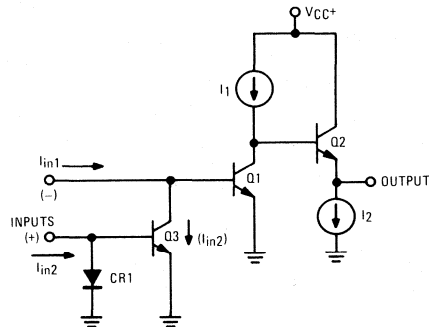


FIGURE 17 — OBTAINING A NONINVERTING INPUT



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor

Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage.

7

OPERATION AND APPLICATIONS (continued)

FIGURE 18 – A BASIC OPERATIONAL AMPLIFIER

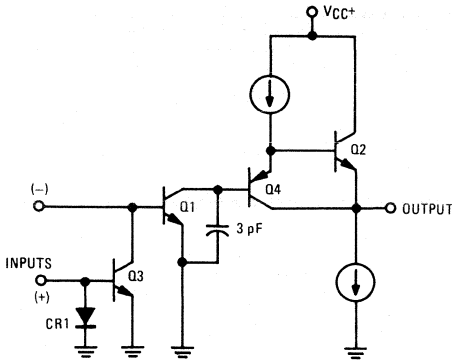
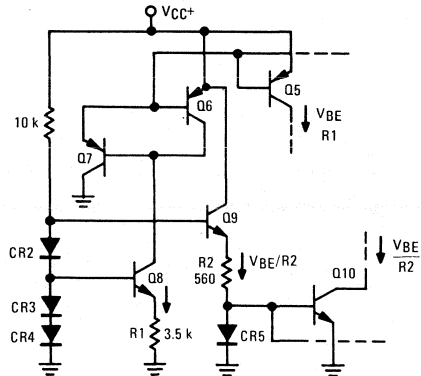


FIGURE 19 – BIASING CIRCUITRY



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing

A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4. The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 5 μ A to 100 μ A range.

B. V_{CC} Reference Voltage (see Figures 3 and 4)

The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r , allowing the input current, I_r , to be within the range of 5 μ A to 100 μ A. Choosing the feedback resistor, R_f , to be equal to $\frac{1}{2} R_r$ will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows for maximum dynamic range of the output voltage.

C. Reference Voltage other than V_{CC} (See Figure 20).

The biasing resistor R_r may be returned to a voltage (V_r)

other than V_{CC} . By setting $R_f = R_r$, (still keeping I_r between 5 μ A and 100 μ A) the output dc level will be equal to V_r . Neglecting error terms, the expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

where ϕ is the V_{BE} drop of the input transistors (approximately 0.7 Vdc @ +25°C).

The error terms not appearing in the above equation can cause the dc operating point to vary up to 20% from the expected value. Error terms are minimized by setting the input current within the range of 5 μ A to 100 μ A.

2. Gain Determination

A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

FIGURE 20 – INVERTING AMPLIFIER WITH ARBITRARY REFERENCE

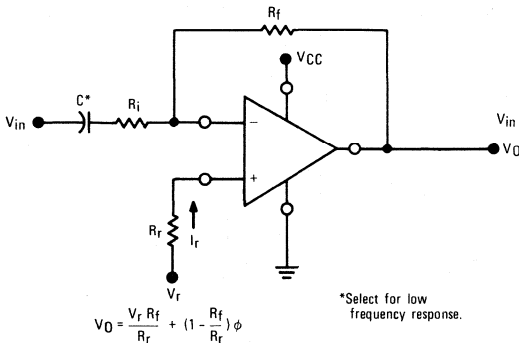
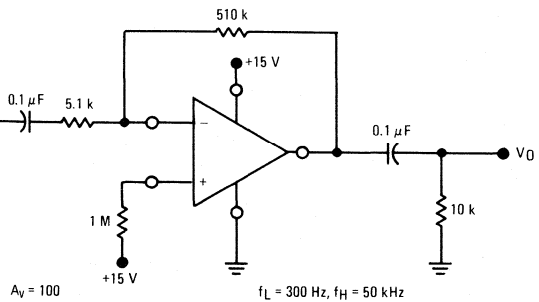


FIGURE 21 – INVERTING AMPLIFIER WITH $A_v = 100$ AND $V_r = V_{CC}$



NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i , in the same manner as for a conventional operational amplifier:

$$A_v = - \frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 5.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 500 kHz with 20 dB of closed loop gain or 50 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

B. Noninverting Amplifier

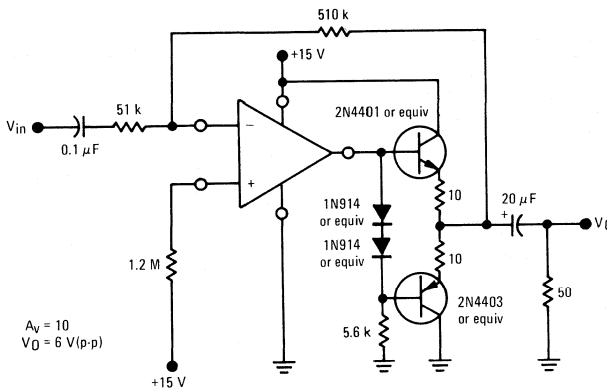
Although recommended as an inverting amplifier, the MC3401P may be used in the noninverting mode (see Figure 4). The amplifier gain in this configuration is subject to the same error terms that affect the output Q point biasing so the gain may deviate as much as $\pm 20\%$ from that expected. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes. The noninverting gain expression is given by:

$$A_v = \frac{R_f}{R_i + \frac{26}{I_r}} \pm 20\%$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For $R_f = 510 \text{ k}\Omega$ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

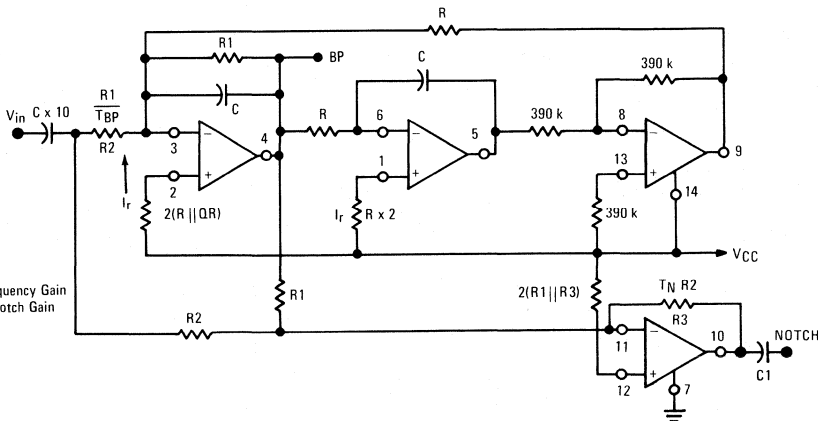
TYPICAL APPLICATIONS

FIGURE 22 – AMPLIFIER AND DRIVER FOR A 50-OHM LINE



$A_v = 10$
 $V_O = 6 \text{ V (p-p)}$

FIGURE 23 – BASIC BANDPASS AND NOTCH FILTER



T_{BP} = Center Frequency Gain
 T_N = Passband Notch Gain
 $\omega_0 = \frac{1}{RC}$
 $R1 = QR$
 $R2 = \frac{R1}{T_{BP}}$
 $R3 = T_N R2$

7

TYPICAL APPLICATIONS (continued)

FIGURE 24 – BANDPASS AND NOTCH FILTER

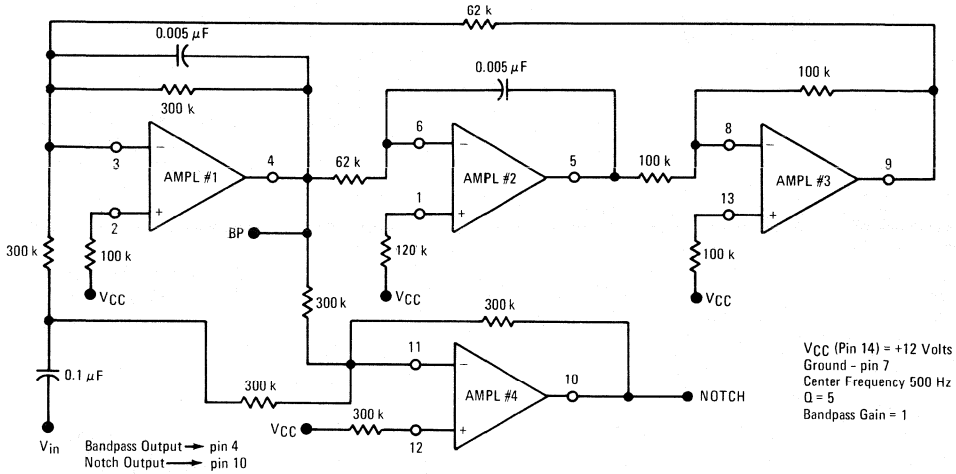
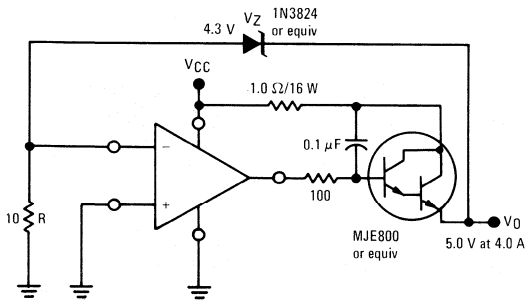
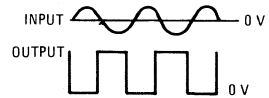
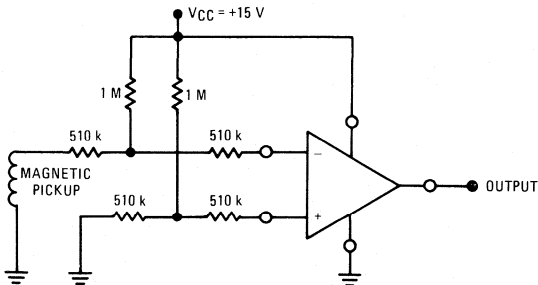


FIGURE 25 – VOLTAGE REGULATOR



$V_O = V_Z + 0.6 \text{ Vdc}$
 NOTE 1: R is used to bias the zener.
 NOTE 2: If the Zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier ($\approx 2.0 \text{ mV}/^\circ\text{C}$), the output is zero-TC. A 7.0-Volt Zener will give approximately zero-TC.

FIGURE 26 – ZERO CROSSING DETECTOR



MC5528, MC5529, MC7528, MC7529 (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Units |
|---|-------------------------------------|-------------|-------|
| Power Supply Voltage | V _{CC} | +7.0 | Vdc |
| | V _{EE} | -7.0 | Vdc |
| Differential Input Voltages | V _{in} or V _{ref} | ±5.0 | Vdc |
| Power Dissipation Derate above T _A = +25°C | P _D | 575 | mW |
| | | 3.85 | mW/°C |
| Operating Temperature Range MC5528, MC5529 MC7528, MC7529 | T _A | -55 to +125 | °C |
| | | 0 to +70 | |
| Storage Temperature Range | T _{stg} | -55 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = T_{low}# to T_{high}# unless otherwise noted.)

| Characteristic | Symbol | MC5528 ① # MC5529 | | | MC7528 # MC7529 | | | Unit |
|--|---------------------|----------------------|------|------|--------------------|------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential Input Threshold Voltage (V _{inS} = +5.0 V, V _{ID} = ±V _{th}) (V _{ref} = 15 mV, I _L = 16 mA, V _O < 0.4 V) | V _{th} | 10 | 15 | — | 11 | 15 | — | mV |
| | | 8.0 | — | — | 8.0 | — | — | |
| | | 35 | 40 | — | 36 | 40 | — | |
| | | 33 | — | — | 33 | — | — | |
| (V _{ref} = 40 mV, I _L = 16 mA, V _O < 0.4 V) | — | — | — | — | — | — | — | |
| (V _{ref} = 15 mV, I _L = -400 μA, V _O > 2.4 V) | — | 15 | 20 | — | 15 | 19 | — | |
| (V _{ref} = 40 mV, I _L = -400 μA, V _O > 2.4 V) | — | — | 22 | — | — | 22 | — | |
| (V _{ref} = 40 mV, I _L = -400 μA, V _O > 2.4 V) | — | 40 | 45 | — | 40 | 44 | — | |
| (V _{ref} = 40 mV, I _L = -400 μA, V _O > 2.4 V) | — | — | 47 | — | — | 47 | — | |
| Differential and Reference Input Bias Current (V _{ID} = V _{ref} = 0V, V _{inS} = +5.25 V, V _S = ±5.25 V) | I _{IB} | — | 30 | 100 | — | 30 | 75 | μA |
| Differential Input Offset Current (V _{ID} = V _{ref} = 0 V, V _{inS} = +5.25 V, V _S = ±5.25 V) | I _{IOD} | — | 0.5 | — | — | 0.5 | — | μA |
| Input Voltage, Logic "1" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = 2.0 V, I _L = 400 μA, V _S = ±4.75 V, V _O > 2.4 V) | V _{in} "1" | 2.0 | — | — | 2.0 | — | — | V |
| Input Voltage, Logic "0" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = 0.8 V, I _L = 16 mA, V _S = ±4.75 V, V _{OL} < 0.4 V) | V _{in} "0" | — | — | 0.8 | — | — | 0.8 | V |
| Input Current, Logic "1" (V _{ID} = 0 V, V _{ref} = 20 mV, V _{inS} = 2.4 V, V _S = ±5.25 V) | I _{in} "1" | — | 5.0 | 40 | — | — | — | μA |
| | | — | — | — | — | 0.02 | 1.0 | |
| Input Current, Logic "0" (V _{ID} = 0 V, V _{ref} = 20 mV, V _{inS} = +5.25 V, V _S = ±5.25 V) | I _{in} "0" | — | — | — | — | — | — | mA |
| | | — | -1.0 | -1.6 | — | -1.0 | -1.6 | |
| Output Voltage, Logic "1" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = 2.0 V, I _L = -400 μA, V _S = ±4.75 V) | V _O "1" | 2.4 | 3.9 | — | 2.4 | 3.9 | — | V |
| Output Voltage, Logic "0" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = 0.8 V, I _L = 16 mA, V _S = ±4.75 V) | V _O "0" | — | 0.25 | 0.40 | — | 0.25 | 0.40 | V |
| Short-Circuit Output Current (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = +5.25 V, V _S = ±5.25 V) | I _{OSC} | -2.1 | -2.8 | -3.5 | -2.1 | -2.8 | -3.5 | mA |
| V _{CC} Supply Current (V _{ID} = V _{inS} = 0 V, V _{ref} = 20 mV, V _S = ±5.25 V) | I _{CC} | — | 29 | 40 | — | 29 | 40 | mA |
| V _{EE} Supply Current (V _{ID} = V _{inS} = 0 V, V _{ref} = 20 mV, V _S = ±5.25 V) | I _{EE} | — | -13 | -18 | — | -13 | -18 | mA |

① For 0°C ≤ T_A ≤ 70°C operation, electrical characteristics for MC5528 and MC5529 are guaranteed the same as MC7528 and MC7529 respectively.

T_{low} = -55°C for MC5528, MC5529, 0°C for MC7528, MC7529
T_{high} = +125°C for MC5528, MC5529, +70°C for MC7528, MC7529

MC5528, MC5529, MC7528, MC7529 (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0\text{ V} \pm 5\%$, $V_{EE} = -5.0\text{ V} \pm 5\%$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Symbol | MC5528 MC5529 | | | MC7528 MC7529 | | | Unit |
|--|------------|------------------|------|-----|------------------|------|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| AC Common-Mode Input Firing Voltage ($V_{ref} = 20\text{ mV}$, $V_{inS} = 5.0\text{ V}$) | V_{CMF} | — | ±2.5 | — | — | ±2.5 | — | V |
| Propagation Delay Time, Differential Input to Logic "1" Output ($V_{ref} = 20\text{ mV}$) | t_{PLHD} | — | 20 | 40 | — | 20 | 40 | ns |
| Propagation Delay Time, Differential Input to Logic "0" Output ($V_{ref} = 20\text{ mV}$) | t_{PHLD} | — | 28 | — | — | 28 | — | ns |
| Propagation Delay Time, Strobe Input to Logic "1" Output ($V_{ref} = 20\text{ mV}$) | t_{PHLS} | — | 10 | 30 | — | 10 | 30 | ns |
| Propagation Delay Time, Strobe Input to Logic "0" Output ($V_{ref} = 20\text{ mV}$) | t_{PHLS} | — | 20 | — | — | 20 | — | ns |
| Overload Recovery Time, Differential Input | t_{RD} | — | 10 | — | — | 10 | — | ns |
| Overload Recovery Time, Common-Mode Input | t_{RCM} | — | 5.0 | — | — | 5.0 | — | ns |
| Minimum Cycle Time | $t(\min)$ | — | 200 | — | — | 200 | — | ns |

② Positive current is defined as current into the referenced pin.

③ Pin 1 to have $\geq 100\text{ pF}$ capacitor connected to ground.

④ Each test point to have $\leq 15\text{ pF}$ capacitive load to ground.

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

DUAL SENSE AMPLIFIERS

MC5534
MC5535
MC7534
MC7535

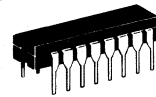
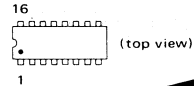
MONOLITHIC DUAL SENSE AMPLIFIERS WITH INVERTED OUTPUTS

This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits. These circuits are identical to the MC7524 except that an additional stage has been added to each output gate to provide an inverted output.

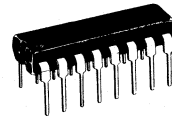
- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs
- Normally High Outputs Accomodate the Wired-OR of Several Sense Amplifiers

DUAL HIGH-SPEED SENSE AMPLIFIER WITH INVERTED OUTPUTS

MONOLITHIC SILICON
INTEGRATED CIRCUIT

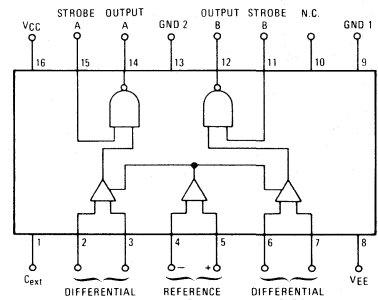
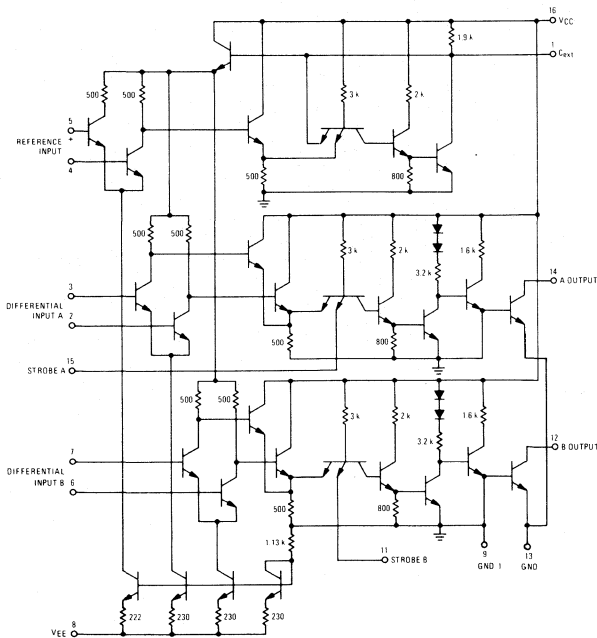


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC7528 and MC7529 only)

SCHEMATIC DIAGRAM



See Packaging Information Section for outline dimensions.

MC5534, MC5535, MC7534, MC7535 (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Units |
|---|-------------------------------------|-------------|-----------------|
| Power Supply Voltage | V _{CC} | +7.0 | V _{dc} |
| | V _{EE} | -7.0 | V _{dc} |
| Differential Input Voltages | V _{in} or V _{ref} | ±5.0 | V _{dc} |
| Power Dissipation Derate above T _A = +25°C | P _D | 575 | mW |
| | | 3.85 | mW/°C |
| Operating Temperature Range MC5534, MC5535 MC7534, MC7535 | T _A | -55 to +125 | °C |
| | | 0 to +70 | |
| Storage Temperature Range | T _{stg} | -55 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = T_{low}# to T_{high}# unless otherwise noted.)

| Characteristic | Symbol | MC5534 ① # MC5535 | | | MC7534# MC7535 | | | Unit |
|--|--------------------|----------------------|------|------|-------------------|------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential Input Threshold Voltage (V _{inS} = +5.0 V, V _{ID} = ±V _{th}) (V _{ref} = 15 mV, V _L = +5.25 V, I _L < 250 μA) MC5534, MC7534 MC5535, MC7535 (V _{ref} = 40 mV, V _L = +5.25 V, I _L < 250 μA) MC5534, MC7534 MC5535, MC7535 (V _{ref} = 15 mV, I _L = 20 mA, V _O = < 0.4 V) MC5534, MC7534 MC5535, MC7535 (V _{ref} = 40 mV, I _L = 200 mA, V _O = < 0.4 V) MC5534, MC7534 MC5535, MC7535 | V _{th} | 10 | 15 | — | 11 | 15 | — | mV |
| | | 8.0 | — | — | 8.0 | — | — | |
| | | 35 | 40 | — | 36 | 40 | — | |
| | | 33 | — | — | 33 | — | — | |
| | | — | 15 | 20 | — | 15 | 19 | |
| — | — | 22 | — | — | 22 | | | |
| — | — | 40 | 45 | — | 40 | 44 | | |
| — | — | — | 47 | — | — | 47 | | |
| Differential Reference Input Bias Current (V _{ID} = V _{ref} = 0 V, V _{inS} = +5.25 V, V _S = ±5.25 V) | I _{IB} | — | 30 | 100 | — | 30 | 75 | μA |
| Differential Input Offset Current (V _{ID} = V _{ref} = 0 V, V _{inS} = +5.25 V, V _S = ±5.25 V) | I _{IOD} | — | 0.5 | — | — | 0.5 | — | μA |
| Input Voltage, Logic "0" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = 0.8 V, V _L = +5.25 V, V _S = ±4.75 V, I _L = < 250 μA) | V _{in"0"} | — | — | 0.8 | — | — | 0.8 | V |
| Input Voltage, Logic "1" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = 2.0 V, I _L = 20 mA, V _S = ±4.75 V, V _O = < 0.4 V) | V _{in"1"} | 2.0 | — | — | 2.0 | — | — | V |
| Input Current, Logic "0" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = 0.4 V, V _S = ±5.25 V) | I _{in"0"} | — | -1.0 | -1.6 | — | -1.0 | -1.6 | mA |
| Input Current, Logic "1" (V _{ID} = 0 V, V _{ref} = 20 mV, V _{inS} = 2.4 V, V _S = ±5.25 V) | I _{in"1"} | — | 5.0 | 40 | — | — | — | μA |
| — | — | — | — | — | 0.02 | 1.0 | — | mA |
| Output Voltage, Logic "0" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = 2.0 V, I _L = 20 mA, V _S = ±4.75 V) | V _{O"0"} | — | 0.25 | 0.40 | — | 0.25 | 0.40 | V |
| Output Leakage Current (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = 0.8 V, V _L = 5.25 V, V _S = ±4.75 V) | I _{OL} | — | 0.01 | 250 | — | 0.01 | 250 | μA |
| V _{CC} Supply Current (V _{ID} = V _{inS} = 0 V, V _{ref} = 20 mV, V _S = ±5.25 V) | I _{CC} | — | 28 | 38 | — | 28 | 38 | mA |
| V _{EE} Supply Current (V _{ID} = V _{inS} = 0 V, V _{ref} = 20 mV, V _S = ±5.25 V) | I _{EE} | — | -13 | -18 | — | -13 | -18 | mA |

① For 0°C ≤ T_A ≤ 70°C operation, electrical characteristics for MC5534 and MC5535 are guaranteed the same as MC7534 and MC7535 respectively.

T_{low} = -55°C for MC5534, MC5535, 0°C for MC7534, MC7535
T_{high} = +125°C for MC5534, MC5535, +70°C for MC7534, MC7535

MC5534, MC5535, MC7534, MC7535 (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0\text{ V} \pm 5\%$, $V_{EE} = -5.0\text{ V} \pm 5\%$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Symbol | MC5534 MC5535 | | | MC7534 MC7535 | | | Unit |
|--|-----------------|------------------|-----------|-----|------------------|-----------|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| AC Common-Mode Input Firing Voltage ($V_{ref} = 20\text{ mV}$, $V_{inS} = 5.0\text{ V}$) | V_{CMF} | — | ± 2.5 | — | — | ± 2.5 | — | V |
| Propagation Delay Time, Differential Input to Logic "1" Output ($V_{ref} = 20\text{ mV}$) | t_{PLHD} | — | 24 | — | — | 24 | — | ns |
| Propagation Delay Time, Differential Input to Logic "0" Output ($V_{ref} = 20\text{ mV}$) | t_{PHLD} | — | 20 | 40 | — | 20 | 40 | ns |
| Propagation Delay Time, Strobe Input to Logic "1" Output ($V_{ref} = 20\text{ mV}$) | t_{PLHS} | — | 16 | — | — | 16 | — | ns |
| Propagation Delay Time, Strobe Input to Logic "0" Output ($V_{ref} = 20\text{ mV}$) | t_{PHLS} | — | 10 | 30 | — | 10 | 30 | ns |
| Overload Recovery Time, Differential Input | t_{RD} | — | 10 | — | — | 10 | — | ns |
| Overload Recovery Time, Common-Mode Input | t_{RCM} | — | 5.0 | — | — | 5.0 | — | ns |
| Minimum Cycle Time | $t(\text{min})$ | — | 200 | — | — | 200 | — | ns |

② Positive current is defined as current into the referenced pin.

③ Pin 1 to have $\geq 100\text{ pF}$ capacitor connected to ground.

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

DUAL SENSE AMPLIFIERS

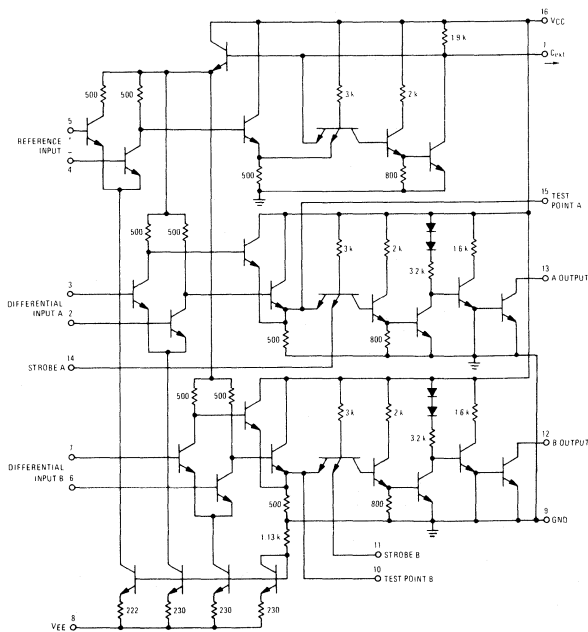
MC5538
MC5539
MC7538
MC7539

MONOLITHIC DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS AND INVERTED OUTPUTS

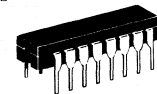
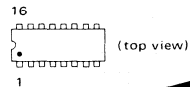
This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits. These devices are identical to MC5528/MC7528 with the exception of the inverted outputs.

- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs
- Test Points Available for Strobe Timing
- Inverted Outputs to Accomodate Wired-OR Outputs of Several Sense Amplifiers

SCHEMATIC DIAGRAM



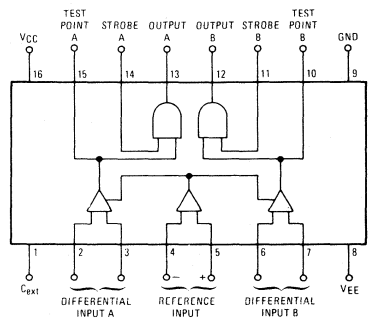
DUAL HIGH-SPEED SENSE AMPLIFIER WITH PREAMPLIFIER TEST POINTS AND INVERTED OUTPUTS MONOLITHIC SILICON INTEGRATED CIRCUIT



L SUFFIX
 CERAMIC PACKAGE
 CASE 620



P SUFFIX
 PLASTIC PACKAGE
 CASE 648
 (MC7538 and MC7539 only)



See Packaging Information Section for outline dimensions.

MC5538, MC5539, MC7538, MC7539 (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Units |
|---|-------------------------------------|-------------|-------|
| Power Supply Voltage | V _{CC} | +7.0 | Vdc |
| | V _{EE} | -7.0 | Vdc |
| Differential Input Voltages | V _{in} or V _{ref} | ±5.0 | Vdc |
| Power Dissipation Derate above T _A = +25°C | P _D | 575 | mW |
| | | 3.85 | mW/°C |
| Operating Temperature Range MC5538, MC5539 MC7538, MC7539 | T _A | -55 to +125 | °C |
| | | 0 to +70 | |
| Storage Temperature Range | T _{stg} | -55 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = T_{low}# to T_{high}# unless otherwise noted.)

| Characteristic | Symbol | MC5538 ① # MC5539 | | | MC7538 # MC7539 | | | Unit |
|--|---------------------|----------------------|------|------|--------------------|------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential Input Threshold Voltage (V _{inS} = +5.0 V, V _{ID} = ±V _{th}) (V _{ref} = 15 mV, V _L = +5.25 V, I _L < 250 μA) | V _{th} | 10 | 15 | — | 11 | 15 | — | mV |
| | | 8.0 | — | — | 8.0 | — | — | |
| | | 35 | 40 | — | 36 | 40 | — | |
| | | 33 | — | — | 33 | — | — | |
| (V _{ref} = 40 mV, V _L = +5.25 V, I _L < 250 μA) | V _{th} | — | 15 | 20 | — | 15 | 19 | mV |
| | | — | — | 22 | — | — | 22 | |
| (V _{ref} = 15 mV, I _L = 120 mA, V _L < 0.4 V) | V _{th} | — | — | 20 | — | — | 19 | mV |
| | | — | — | 22 | — | — | 22 | |
| (V _{ref} = 40 mV, I _L = +20 mA, V _L < 0.4 V) | V _{th} | — | 40 | 45 | — | 40 | 44 | mV |
| | | — | — | 47 | — | — | 47 | |
| Differential and Reference Input Bias Current (V _{ID} = V _{ref} = 0 V, V _{inS} = +5.25 V, V _S = ±5.25 V) | I _{IB} | — | 30 | 100 | — | 30 | 75 | μA |
| Differential Input Offset Current (V _{ID} = V _{ref} = 0 V, V _{inS} = +5.25 V, V _S = ±5.25 V) | I _{IOD} | — | 0.5 | — | — | 0.5 | — | μA |
| Input Voltage, Logic "1" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = +2.0 V, I _L = 20 mA, V _S = ±4.75 V, V _L < 0.4 V) | V _{in} "1" | 2.0 | — | — | 2.0 | — | — | V |
| Input Voltage, Logic "0" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = +0.8 V, V _L = +5.25 V, V _S = ±4.75 V, I _L < 250 μA) | V _{in} "0" | — | — | 0.8 | — | — | 0.8 | V |
| Input Current, Logic "1" (V _{ID} = 0 V, V _{ref} = 20 mV, V _{inS} = 2.4 V, V _S = ±5.25 V) | I _{in} "1" | — | 5.0 | 40 | — | — | — | μA |
| | | — | — | — | — | 0.02 | 1.0 | |
| Input Current, Logic "0" (V _{ID} = 0 V, V _{ref} = 20 mV, V _{inS} = +5.25 V, V _S = ±5.25 V) | I _{in} "0" | — | — | — | — | — | — | mA |
| | | — | — | — | — | — | — | |
| Input Current, Logic "0" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = 0.4 V, V _S = ±5.25 V) | I _{in} "0" | — | -1.0 | -1.6 | — | -1.0 | -1.6 | mA |
| Output Voltage, Logic "0" (V _{ID} = 40 mV, V _{ref} = 20 mV, V _{inS} = 2.0 V, I _L = 20 mA, V _S = ±4.75 V) | V _O "0" | — | 0.25 | 0.40 | — | 0.25 | 0.40 | V |
| V _{CC} Supply Current (V _{ID} = V _{inS} = 0 V, V _{ref} = 20 mV, V _S = ±5.25 V) | I _{CC} | — | 28 | 38 | — | 28 | 38 | mA |
| V _{EE} Supply Current (V _{ID} = V _{inS} = 0 V, V _S = ±5.25 V) | I _{EE} | — | -13 | -18 | — | -13 | -18 | mA |

① For 0°C ≤ T_A ≤ 70°C operation, electrical characteristics for MC5538 and MC5539 are guaranteed the same as MC7538 and MC7539 respectively.

T_{low} = -55°C for MC5538, MC5539; 0°C for MC7538, MC7539
T_{high} = +125°C for MC5538, MC5539; +70°C for MC7538, MC7539

MC5538, MC5539, MC7538, MC7539 (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0\text{ V} \pm 5\%$, $V_{EE} = -5.0\text{ V} \pm 5\%$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Symbol | MC5538 MC5539 | | | MC7538 MC7539 | | | Unit |
|--|-----------------|------------------|------|-----|------------------|------|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| AC Common-Mode Input Firing Voltage ($V_{ref} = 20\text{ mV}$, $V_{inS} = 5.0\text{ V}$) | V_{CMF} | — | ±2.5 | — | — | ±2.5 | — | V |
| Propagation Delay Time, Differential Input to Logic "1" Output ($V_{ref} = 20\text{ mV}$) | t_{PLHD} | — | 24 | — | — | 24 | — | ns |
| Propagation Delay Time, Differential Input to Logic "0" Output ($V_{ref} = 20\text{ mV}$) | t_{PHLD} | — | 20 | 40 | — | 20 | 40 | ns |
| Propagation Delay Time, Strobe Input to Logic "1" Output ($V_{ref} = 20\text{ mV}$) | t_{PHLS} | — | 16 | — | — | 16 | — | ns |
| Propagation Delay Time, Strobe Input to Logic "0" Output ($V_{ref} = 20\text{ mV}$) | t_{PHLS} | — | 10 | 30 | — | 10 | 30 | ns |
| Overload Recovery Time, Differential Input | t_{RD} | — | 10 | — | — | 10 | — | ns |
| Overload Recovery Time, Common-Mode Input | t_{RCM} | — | 5.0 | — | — | 5.0 | — | ns |
| Minimum Cycle Time | $t(\text{min})$ | — | 200 | — | — | 200 | — | ns |

② Positive current is defined as current into the referenced pin.

③ Pin 1 to have $\geq 100\text{ pF}$ capacitor connected to ground.

④ Each test point to have $\leq 15\text{ pF}$ capacitive load to ground.

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

DUAL SENSE AMPLIFIERS

MC7520L thru MC7523L

MONOLITHIC DUAL SENSE AMPLIFIERS

These dual sense amplifiers are designed for high-speed core memory systems. Low-level pulses originating in the memory are converted to logic levels compatible with MTTL and MDTL circuits. Each of the two basic device functions has two different threshold specifications. The dual-input preamplifiers are connected to a common output stage, with each preamplifier output strobed independently.

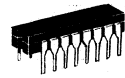
The output circuit of the MC7520L/MC7521L is comprised of two cascaded NAND gates, each having an external gate input. The external gate inputs may be used to connect the \bar{Q} output to the Gate Q input to achieve a flip-flop or register that responds to the sense and strobe input conditions. Output pulse stretching may be accomplished by resistive/capacitive coupling from the \bar{Q} output to the Gate Q input.

The output circuit of the MC7522L/MC7523L features an open-collector output, permitting the wired OR function. Load resistor R_L may be used as the output pullup resistor.

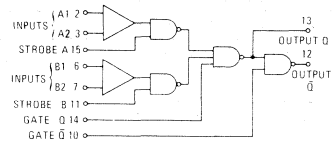
- Adjustable Threshold Voltage Levels
- High Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin – 1.0 Volt typical
- Good Fanout Capability

DUAL HIGH-SPEED SENSE AMPLIFIER INTEGRATED CIRCUITS MONOLITHIC SILICON EPITAXIAL PASSIVATED

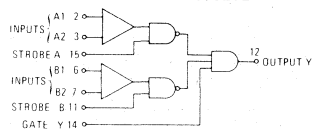
CERAMIC PACKAGE
CASE 620



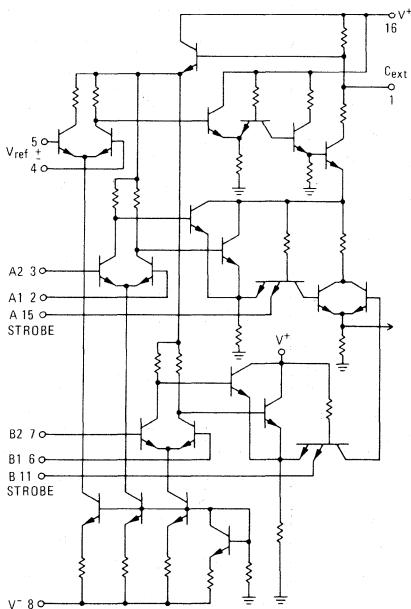
MC7520L and MC7521L



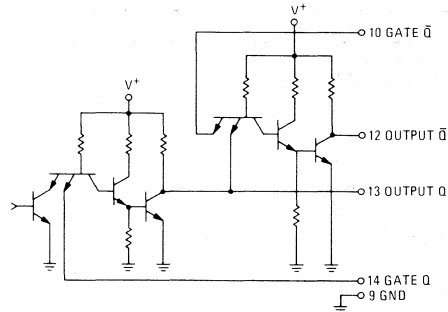
MC7522L and MC7523L



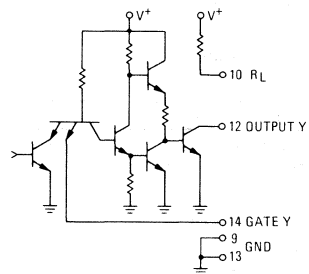
COMMON TO ALL DEVICES



MC7520L and MC7521L ONLY



MC7522L and MC7523L ONLY



See Packaging Information Section for outline dimensions.

MC7520L thru MC7523L (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = 5.0\text{ V}$, $V^- = -5.0\text{ V}$, $T_A = 0$ to $+70^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---------------|-------------------|------------|-------------------|---------------------|
| Input Threshold Voltage $V_{ref} = 15\text{ mV}$ MC7520L,MC7522L MC7521L,MC7523L | V_{th} | 11 8.0 | 15 15 | 19 22 | mV |
| $V_{ref} = 40\text{ mV}$ MC7520L,MC7522L MC7521L,MC7523L | | 36 33 | 40 40 | 44 47 | |
| Common-Mode Input Firing Voltage | V_{CMF} | — | ± 3.0 | — | Volts |
| Input Bias Current | I_{in} | — | 30 | 75 | μA |
| Input Offset Current | I_{io} | — | 0.5 | — | μA |
| Input Impedance ($f = 1.0\text{ kHz}$) | $Z_{(in)} D$ | — | 2.0 | — | k ohms |
| Input Voltage Logic "1" Level (Strobe Inputs) $V_{in} "0" = 0.8\text{ V}$ | $V_{in} "1"$ | 2.0 | — | — | Volts |
| Input Voltage Logic "0" Level (Strobe Inputs) $V_{in} "1" = 2.0\text{ V}$ | $V_{in} "0"$ | — | — | 0.8 | Volt |
| Input Current Logic "0" Level (Strobe Inputs) $V_{in} "0" = 0.4\text{ V}$ | $I_{in} "0"$ | — | — | -1.6 | mA |
| Input Current Logic "1" Level (Strobe Inputs) $V_{in} "1" = 2.4\text{ V}$ $V_{in} "1" = V^+$ | $I_{in} "1"$ | — | — | 40 1.0 | μA mA |
| Output Voltage Logic "1" Level $V_{in} "1" = 2.0\text{ V}$ | $V_{out} "1"$ | 2.4 | 3.9 | — | Volts |
| Output Voltage Logic "0" Level $V_{in} "0" = 0.8\text{ V}$ | $V_{out} "0"$ | — | 0.25 | 0.4 | Volt |
| Short-Circuit Output Current Q Output MC7520L,MC7521L \bar{Q} Output MC7520L,MC7521L Output MC7522L,MC7523L | I_{SC} | 3.3 2.1 2.1 | — | 5.0 3.5 3.5 | mA |
| V^+ Supply Current ($T_A = +25^\circ\text{C}$) MC7520L,MC7521L MC7522L,MC7523L | I^+ | — | 28 27 | — | mA |
| V^- Supply Current ($T_A = +25^\circ\text{C}$) MC7520L,MC7521L MC7522L,MC7523L | I^- | — | -14 -15 | — | mA |

SWITCHING CHARACTERISTICS ($V^+ = 5.0\text{ V}$, $V^- = -5.0\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-------------|-----|-----|-----|------|
| Differential-Mode Input Overload Recovery Time | $t_{OR DM}$ | — | 20 | — | ns |
| Common-Mode Input Overload Recovery Time | $t_{OR CM}$ | — | 20 | — | ns |
| Minimum Cycle Time | t_c (min) | — | 200 | — | ns |

MC7520L, MC7521L

| | | | | | |
|--|--|---|----------------|--------------|----|
| Propagation Delay Time (Differential Input to Q Output) | $t_{pd} "1" DQ$ | — | 20 | 40 | ns |
| (Differential Input to \bar{Q} Output) | $t_{pd} "0" DQ$ $t_{pd} "1" D\bar{Q}$ $t_{pd} "0" D\bar{Q}$ | — | 30 25 35 | — — 55 | |
| (Strobe Input to Q Output) | $t_{pd} "1" SQ$ $t_{pd} "0" SQ$ | — | 15 25 | 30 — | |
| (Strobe Input to \bar{Q} Output) | $t_{pd} "1" S\bar{Q}$ $t_{pd} "0" S\bar{Q}$ | — | 15 35 | — 55 | |
| (Gate Q Input to Q Output) | $t_{pd} "1" G_Q Q$ $t_{pd} "0" G_Q Q$ | — | 10 15 | 20 — | |
| (Gate Q Input to \bar{Q} Output) | $t_{pd} "1" G_Q \bar{Q}$ $t_{pd} "0" G_Q \bar{Q}$ | — | 15 20 | — 30 | |
| (Gate \bar{Q} Input to \bar{Q} Output) | $t_{pd} "1" G_{\bar{Q}} \bar{Q}$ $t_{pd} "0" G_{\bar{Q}} \bar{Q}$ | — | 15 10 | — 20 | |

MC7522L, MC7523L

| | | | | | |
|--|----------------------------------|---|----------|---------|----|
| Propagation Delay Time (Differential Input to Output) | $t_{pd} "1" D$ $t_{pd} "0" D$ | — | 20 30 | — 45 | ns |
| (Strobe Input to Output) | $t_{pd} "1" S$ $t_{pd} "0" S$ | — | 15 25 | — 40 | |
| (Gate Input to Output) | $t_{pd} "1" G$ $t_{pd} "0" G$ | — | 10 15 | — 25 | |

MC7520L thru MC7523L (continued)

MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Units |
|---|--------------------|-------------|-------|
| Power Supply Voltage | V ⁺ | +7.0 | Vdc |
| | V ⁻ | -7.0 | Vdc |
| Differential Input Signal Voltage | V _{in} | ±5.0 | Vdc |
| Strobe and Gate Input Voltage | V _{inS,G} | ±5.5 | Vdc |
| Power Dissipation Derate above $T_A = +25^{\circ}\text{C}$ | P _D | 575 | mW |
| | | 3.85 | mW/°C |
| Operating Temperature Range | T _A | 0 to +70 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

MC7524L MC7525L

DUAL SENSE AMPLIFIERS

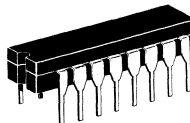
MONOLITHIC DUAL SENSE AMPLIFIERS

This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits.

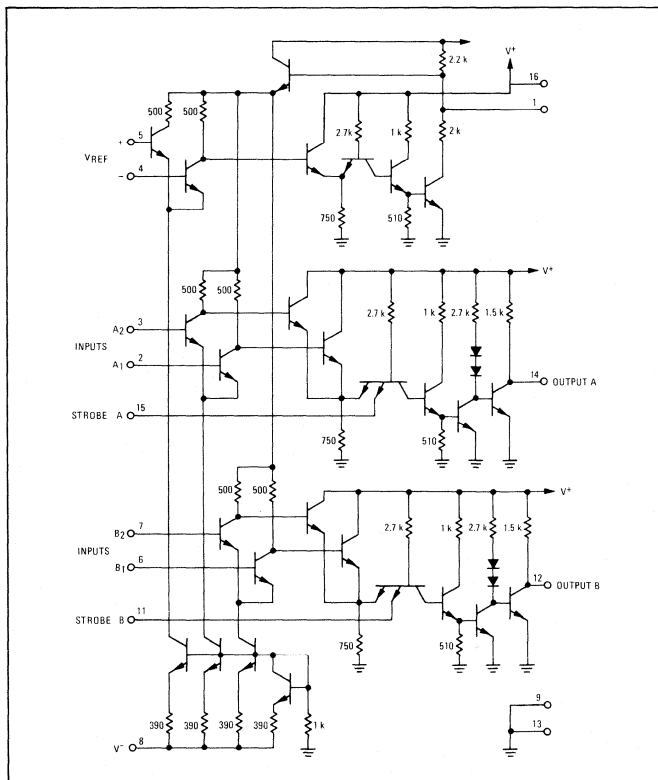
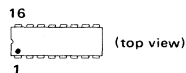
Features:

- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs

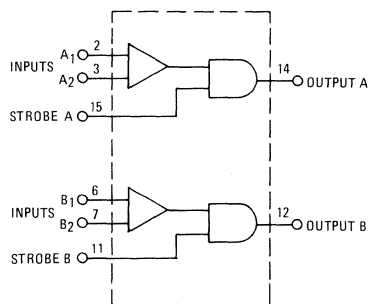
DUAL HIGH-SPEED SENSE AMPLIFIER INTEGRATED CIRCUIT MONOLITHIC SILICON EPITAXIAL PASSIVATED



CERAMIC PACKAGE
CASE 620



Equivalent Circuit



See Packaging Information Section for outline dimensions.

MC7524L, MC7525L (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Units |
|---|-----------------------|-------------|-------|
| Power Supply Voltage | V^+ | +7.0 | Vdc |
| | V^- | -7.0 | Vdc |
| Differential Input Voltages | V_{in} or V_{ref} | ± 5.0 | Vdc |
| Power Dissipation Derate above $T_A = +25^\circ\text{C}$ | P_D | 575 | mW |
| | | 3.85 | mW/°C |
| Operating Temperature Range | T_A | 0 to +70 | °C |
| Storage Temperature Range | T_{stg} | -55 to +150 | °C |

ELECTRICAL CHARACTERISTICS ($V^+ = 5.0\text{ V}$, $V^- = -5.0\text{ V}$, $T_A = 0$ to $+70^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|-----|-----------|------|---------------|
| Input Threshold Voltage $V_{ref} = 15\text{ mV}$ $V_{ref} = 40\text{ mV}$ | V_{th} | 11 | 15 | 19 | mV |
| | | 8.0 | 15 | 22 | |
| | | 36 | 40 | 44 | |
| | | 33 | 40 | 47 | |
| Common-Mode Input Firing Voltage | V_{CMF} | — | ± 3.0 | — | Volts |
| Input Bias Current | I_{in} | — | 30 | 75 | μA |
| Input Offset Current | I_{io} | — | 0.5 | — | μA |
| Input Impedance ($f = 1.0\text{ kHz}$) | $Z_{(in)} D$ | — | 2.0 | — | k ohms |
| Input Voltage Logic "1" Level (Strobe Inputs) | $V_{in(0)} = 0.8\text{ V}$ $V_{in(1)}$ | 2.0 | — | — | Volts |
| Input Voltage Logic "0" Level (Strobe Inputs) | $V_{in(1)} = 2.0\text{ V}$ $V_{in(0)}$ | — | — | 0.8 | Volt |
| Input Current Logic "0" Level (Strobe Inputs) | $V_{in(0)} = 0.4\text{ V}$ $I_{in(0)}$ | — | -1.0 | -1.6 | mA |
| Input Current Logic "1" Level (Strobe Inputs) | $V_{in(1)} = 2.4\text{ V}$ $V_{in(1)} = V^+$ $I_{in(1)}$ | — | — | 40 | μA |
| | | — | — | 1.0 | mA |
| Output Voltage Logic "1" Level | $V_{in(1)} = 2.0\text{ V}$, $V_{in(0)} = 0.8\text{ V}$ $V_{out(1)}$ | 2.4 | 3.9 | — | Volts |
| Output Voltage Logic "0" Level | $V_{in(0)} = 0.8\text{ V}$ $V_{out(0)}$ | — | 0.25 | 0.4 | Volt |
| Short-Circuit Output Current | $I_{sc(out)}$ | 2.1 | — | 3.5 | mA |
| V^+ Supply Current @ $T_A = +25^\circ\text{C}$ | I^+ | — | 25 | — | mA |
| V^- Supply Current @ $T_A = +25^\circ\text{C}$ | I^- | — | -15 | — | mA |

SWITCHING CHARACTERISTICS ($V^+ = 5.0\text{ V}$, $V^- = -5.0\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-------------------|-----|-----|-----|------|
| Propagation Delay Time (Differential Input to Output) | $t_{pd(1) D}$ | — | 15 | 40 | ns |
| | $t_{pd(0) D}$ | — | 40 | — | |
| Propagation Delay Time (Strobe Input to Output) | $t_{pd(1) S}$ | — | 15 | 30 | ns |
| | $t_{pd(0) S}$ | — | 35 | — | |
| Differential-Mode Input Overload Recovery Time | $t_{OR DM}$ | — | 20 | — | ns |
| Common-Mode Input Overload Recovery Time | $t_{OR CM}$ | — | 20 | — | ns |
| Minimum Cycle Time | $t_c(\text{min})$ | — | 200 | — | ns |

TWISTED-PAIR LINE RECEIVERS

MC55107
MC55108
MC75107
MC75108

MONOLITHIC DUAL LINE RECEIVERS

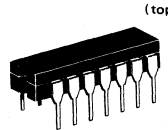
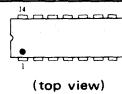
The MC55107/MC75107 and MC55108/MC75108 are MTTL compatible dual line receivers featuring independent channels with common voltage supply and ground terminals. The MC55107/MC75107 circuit features an active pull-up (totem-pole) output. The MC55108/MC75108 circuit features an open-collector output configuration that permits the Wired-OR logic connection with similar outputs (such as the MC5401/MC7401 MTTL gate or additional MC55108/MC75108 receivers). Thus a level of logic is implemented without extra delay. Both receivers feature double-protected input stages to guard against line loading under zero value supply conditions.

The MC55107/MC75107 and MC55108/MC75108 circuits are designed to detect input signals of greater than 25 millivolts amplitude and convert the polarity of the signal into appropriate MTTL compatible output logic levels.

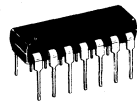
- High Common-Mode Rejection Ratio
- High Input-Impedance
- High Input Sensitivity
- Differential Input Common-Mode Voltage Range of ± 3.0 V
- Diode-Protected Input Stage
- Differential Input Common-Mode Voltage of More Than ± 15 V Using External Attenuator
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- MTTL or MDTL Drive Capability
- High DC Noise Margins

DUAL LINE RECEIVERS

MONOLITHIC SILICON INTEGRATED CIRCUITS



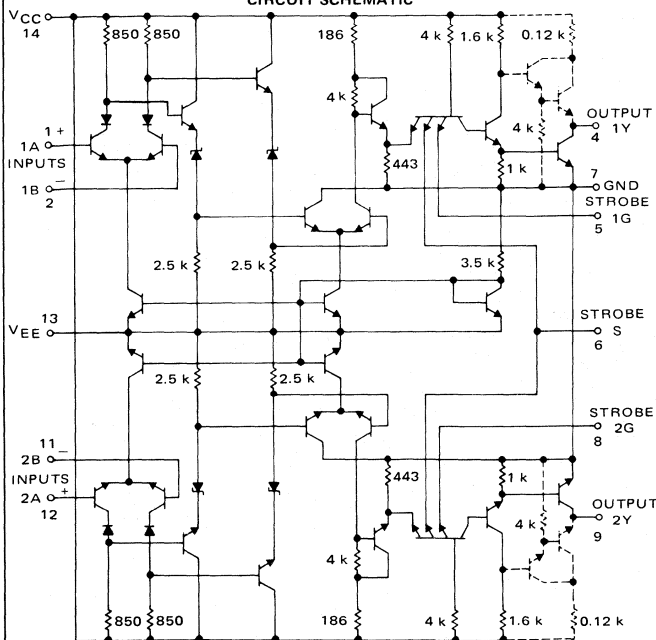
L SUFFIX
 CERAMIC PACKAGE
 CASE 632
 (TO-116)



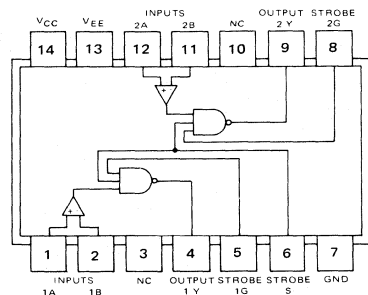
P SUFFIX
 PLASTIC PACKAGE
 CASE 646
 (TO-116)

(MC75107, MC75108 only)

CIRCUIT SCHEMATIC



Components shown with dashed lines are applicable to the MC55107 and MC75107 only.



TRUTH TABLE

| DIFFERENTIAL INPUTS A B | STROBES | | OUTPUT Y |
|-----------------------------|---------|--------|---------------|
| | G | S | |
| $V_{ID} \geq 25$ mV | L or H | L or H | H |
| | L or H | L | H |
| -25 mV $< V_{ID} < 25$ mV | L | L or H | H |
| | H | H | INDETERMINATE |
| $V_{ID} \leq -25$ mV | L or H | L | H |
| | L | L or H | H |
| | H | H | L |

See Packaging Information Section for outline dimensions.

MC55107, MC75107, MC55108, MC75108 (continued)

MAXIMUM RATINGS ($T_A = T_{Low}^*$ to T_{High}^* unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|------------|-------------|----------------------|
| Power Supply Voltages | V_{CC} | +7.0 | Vdc |
| | V_{EE} | -7.0 | Vdc |
| Differential-Mode Input Signal Voltage Range | V_{ID} | +6.0 | Vdc |
| Common-Mode Input Voltage Range | V_{ICR} | +5.0 | Vdc |
| Strobe Input Voltage | $V_{I(S)}$ | 5.5 | Vdc |
| Power Dissipation (Package Limitation) Plastic and Ceramic Dual-In-Line Packages Derate above $T_A = +25^\circ\text{C}$ | P_D | 575 | mW |
| | | 3.85 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range MC55107, MC55108 MC75107, MC75108 | T_A | -55 to +125 | $^\circ\text{C}$ |
| | | 0 to +70 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

RECOMMENDED OPERATING CONDITIONS

| Characteristic | Symbol | MC55107, MC55108 | | | MC75107, MC75108 | | | Unit |
|---|-----------|------------------|------|------|------------------|------|-------|------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Power Supply Voltages | V_{CC} | +4.5 | +5.0 | +5.5 | +4.75 | +5.0 | +5.25 | Vdc |
| | V_{EE} | -4.5 | -5.0 | -5.5 | -4.75 | -5.0 | -5.25 | |
| Output Sink Current | I_{OS} | — | — | -16 | — | — | -16 | mA |
| Differential-Mode Input Voltage Range | V_{IDR} | -5.0 | — | +5.0 | -5.0 | — | +5.0 | Vdc |
| Common-Mode Input Voltage Range | V_{ICR} | -3.0 | — | +3.0 | -3.0 | — | +3.0 | Vdc |
| Input Voltage Range, any differential input to ground | V_{IR} | -5.0 | — | +3.0 | -5.0 | — | +3.0 | Vdc |
| Operating Temperature Range | T_A | -55 | — | +125 | 0 | — | +70 | $^\circ\text{C}$ |

DEFINITIONS OF INPUT LOGIC LEVELS

| Characteristic | Symbol | Test Fig. | Min | Max | Unit |
|--|-------------|-----------|-------|--------|------|
| High-Level Input Voltage (between differential inputs) | V_{IDH} | 1 | 0.025 | 5.0 | Vdc |
| Low-Level Input Voltage (between differential inputs) | V_{IDL} | 1 | -5.0† | -0.025 | Vdc |
| High-Level Input Voltage (at strobe inputs) | $V_{IH(S)}$ | 3 | 2.0 | 5.5 | Vdc |
| Low-Level Input Voltage (at strobe inputs) | $V_{IL(S)}$ | 3 | 0 | 0.8 | Vdc |

†The algebraic convention, where the most positive limit is designated maximum, is used with Low-Level Input Voltage Level (V_{IDL}).

ELECTRICAL CHARACTERISTICS ($T_A = T_{Low}^*$ to T_{High}^* unless otherwise noted)

| Characteristic | Symbol | Test Fig. | MC55107, MC75107 | | | MC55108, MC75108 | | | Unit |
|---|------------|-----------|------------------|-------|------|------------------|-------|------|---------------------|
| | | | Min | Typ # | Max | Min | Typ # | Max | |
| High-Level Input Current to 1A or 2A Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{ID} = 0.5\text{ V}$, $V_{IC} = -3.0\text{ V}$ to $+3.0\text{ V}$) ‡ | I_{IH} | 2 | — | 30 | 75 | — | 30 | 75 | μA |
| Low-Level Input Current to 1A or 2A Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{ID} = -2.0\text{ V}$, $V_{IC} = -3.0\text{ V}$ to $+3.0\text{ V}$) ‡ | I_{IL} | 2 | — | — | -10 | — | — | -10 | μA |
| High-Level Input Current to 1G or 2G Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH(S)} = 2.4\text{ V}$) ‡ ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH(S)} = V_{CC}\text{ Max}$) ‡ | I_{IH} | 4 | — | — | 40 | — | — | 40 | μA mA |
| Low-Level Input Current to 1G or 2G Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL(S)} = 0.4\text{ V}$) ‡ | I_{IL} | 4 | — | — | -1.0 | — | — | -1.0 | mA |
| High-Level Input Current to S Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH(S)} = 2.4\text{ V}$) ‡ ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH(S)} = V_{CC}\text{ Max}$) ‡ | I_{IH} | 4 | — | — | 80 | — | — | 80 | μA mA |
| Low-Level Input Current to S Input ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL(S)} = 0.4\text{ V}$) ‡ | I_{IL} | 4 | — | — | -3.2 | — | — | -3.2 | mA |
| High-Level Output Voltage ($V_{CC} = \text{Min}$, $V_{EE} = \text{Min}$, $I_{load} = -400\text{ }\mu\text{A}$, $V_{IC} = -3.0\text{ V}$ to $+3.0\text{ V}$) ‡ | V_{OH} | 3 | 2.4 | — | — | — | — | — | V |
| Low-Level Output Voltage ($V_{CC} = \text{Min}$, $V_{EE} = \text{Min}$, $I_{sink} = 16\text{ mA}$, $V_{IC} = -3.0\text{ V}$ to $+3.0\text{ V}$) ‡ | V_{OL} | 3 | — | — | 0.4 | — | — | 0.4 | V |
| High-Level Leakage Current ($V_{CC} = \text{Min}$, $V_{EE} = \text{Min}$, $V_{OH} = V_{CC}\text{ Max}$) ‡ | I_{CEX} | 3 | — | — | — | — | — | 250 | μA |
| Short-Circuit Output Current # # ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$) ‡ | I_{OSC} | 5 | -18 | — | -70 | — | — | — | mA |
| High Logic Level Supply Current from V_{CC} ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{ID} = 25\text{ mV}$, $T_A = +25^\circ\text{C}$) ‡ | I_{CCH+} | 6 | — | 18 | 30 | — | 18 | 30 | mA |
| High Logic Level Supply Current from V_{EE} ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{ID} = 25\text{ mV}$, $T_A = +25^\circ\text{C}$) ‡ | I_{CCH-} | 6 | 0 | -8.4 | -15 | 0 | 8.4 | -15 | mA |

‡For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.

#All typical values are at $V_{CC} = +5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$, $T_A = +25^\circ\text{C}$.

#Not more than one output should be shorted at a time.

* $T_{Low} = -55^\circ\text{C}$ for MC55107 and MC55108, $T_{High} = +125^\circ\text{C}$ for MC55107 and MC55108
 $= 0$ for MC75107 and MC75108, $T_{High} = +70^\circ\text{C}$ for MC75107 and MC75108



MC55107, MC75107, MC55108, MC75108 (continued)

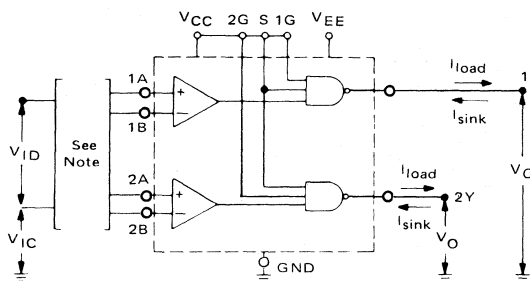
SWITCHING CHARACTERISTICS ($V_{CC} = +5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$, $T_A = +25^\circ\text{C}$)

| Characteristic | Symbol | Test Fig. | MC55107, MC75107 | | | MC55108, MC75108 | | | Unit |
|--|--------------|-----------|------------------|-----|-----|------------------|-----|-----|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Propagation Delay Time, low-to-high level from differential inputs A and B to output ($R_L = 390\ \Omega$, $C_L = 50\ \text{pF}$) ($R_L = 390\ \Omega$, $C_L = 15\ \text{pF}$) | $t_{PLH(D)}$ | 7 | — | 17 | 25 | — | 19 | 25 | ns |
| Propagation Delay Time, high-to-low level from differential inputs A and B to output ($R_L = 390\ \Omega$, $C_L = 50\ \text{pF}$) ($R_L = 390\ \Omega$, $C_L = 15\ \text{pF}$) | $t_{PHL(D)}$ | 7 | — | 17 | 25 | — | 19 | 25 | ns |
| Propagation Delay Time, low-to-high level, from strobe input to G or S output ($R_L = 390\ \Omega$, $C_L = 50\ \text{pF}$) ($R_L = 390\ \Omega$, $C_L = 15\ \text{pF}$) | $t_{PLH(S)}$ | 7 | — | 10 | 15 | — | 13 | 20 | ns |
| Propagation Delay Time, high-to-low level, from strobe input G or S to output ($R_L = 390\ \Omega$, $C_L = 50\ \text{pF}$) ($R_L = 390\ \Omega$, $C_L = 15\ \text{pF}$) | $t_{PHL(S)}$ | 7 | — | 8.0 | 15 | — | 13 | 20 | ns |

Symbols conform to JEDEC Bulletin No. 1 when applicable.

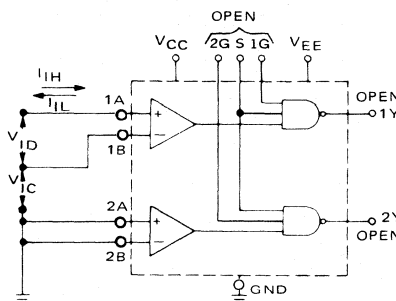
TEST CIRCUITS

FIGURE 1 – V_{IDH} and V_{IDL}



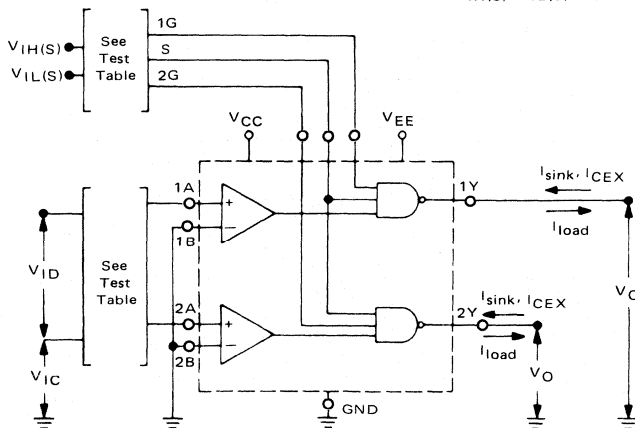
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 2 – I_{IH} and I_{IL}



NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded.

FIGURE 3 – $V_{IH(S)}$, $V_{IL(S)}$, V_{OH} , V_{OL} , and I_{OH}

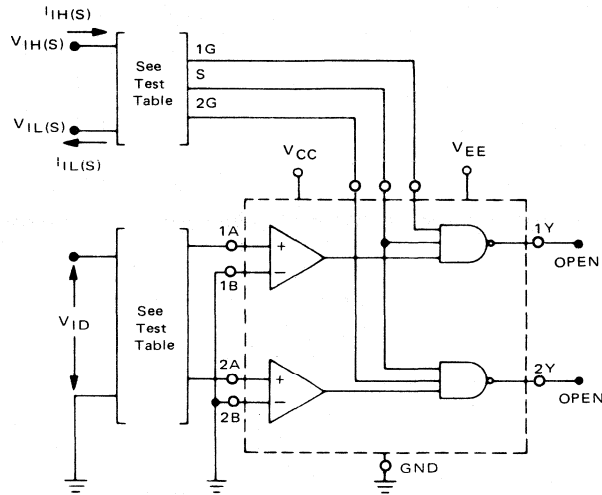


| MC55107 MC75107 | MC55108 MC75108 | V_{ID} | STROBE 1G or 2G | STROBE S |
|--------------------|--------------------|----------|-----------------|-------------|
| TEST | | APPLY | | |
| V_{OH} | I_{CEX} | +25 mV | $V_{IH(S)}$ | $V_{IH(S)}$ |
| V_{OH} | I_{CEX} | -25 mV | $V_{IL(S)}$ | $V_{IH(S)}$ |
| V_{OH} | I_{CEX} | -25 mV | $V_{IH(S)}$ | $V_{IL(S)}$ |
| V_{OL} | V_{OL} | -25 mV | $V_{IH(S)}$ | $V_{IH(S)}$ |

NOTES: 1. $V_{IC} = -3.0\text{ V to }+3.0\text{ V}$.
2. When testing one channel, the inputs of the other channel should be grounded.

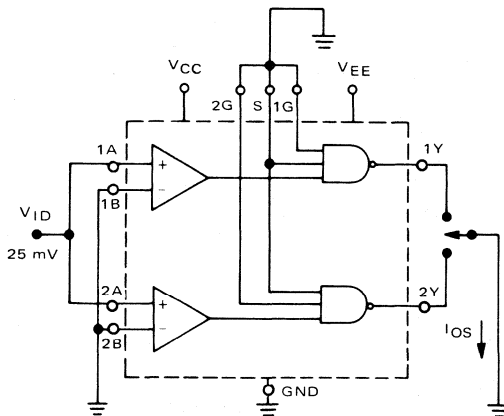
TEST CIRCUITS (continued)

FIGURE 4 - $I_{IH}(G)$, $I_{IL}(G)$, $I_{IH}(S)$, and $I_{IL}(S)$



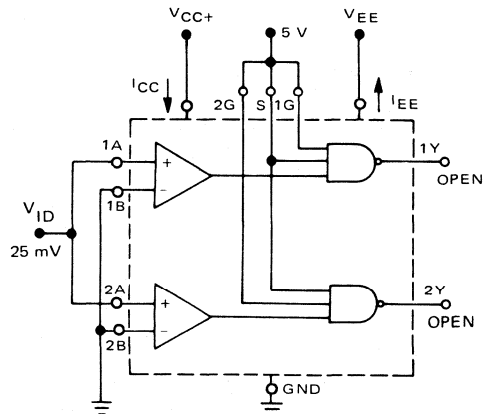
| TEST | INPUT 1A | INPUT 2A | STROBE 1G | STROBE S | STROBE 2G |
|-----------------------|----------|----------|-------------|-------------|-------------|
| I_{IH} at Strobe 1G | +25 mV | Gnd | $V_{IH}(S)$ | Gnd | Gnd |
| I_{IH} at Strobe 2G | Gnd | +25 mV | Gnd | Gnd | $V_{IH}(S)$ |
| I_{IH} at Strobe S | +25 mV | +25 mV | Gnd | $V_{IH}(S)$ | Gnd |
| I_{IL} at Strobe 1G | -25 mV | Gnd | $V_{IL}(S)$ | 4.5 V | Gnd |
| I_{IL} at Strobe 2G | Gnd | -25 mV | Gnd | 4.5 V | $V_{IL}(S)$ |
| I_{IL} at Strobe S | -25 mV | -25 mV | 4.5 V | $V_{IL}(S)$ | 4.5 V |

FIGURE 5 - I_{OS}



- NOTES: 1. Each channel is tested separately.
 2. Not more than one output should be tested at one time.

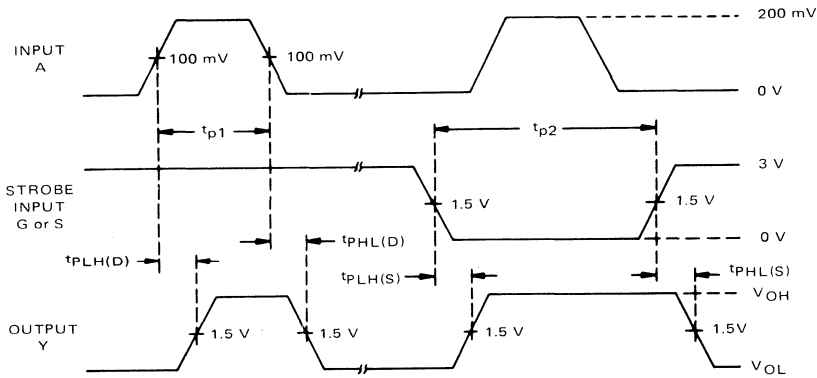
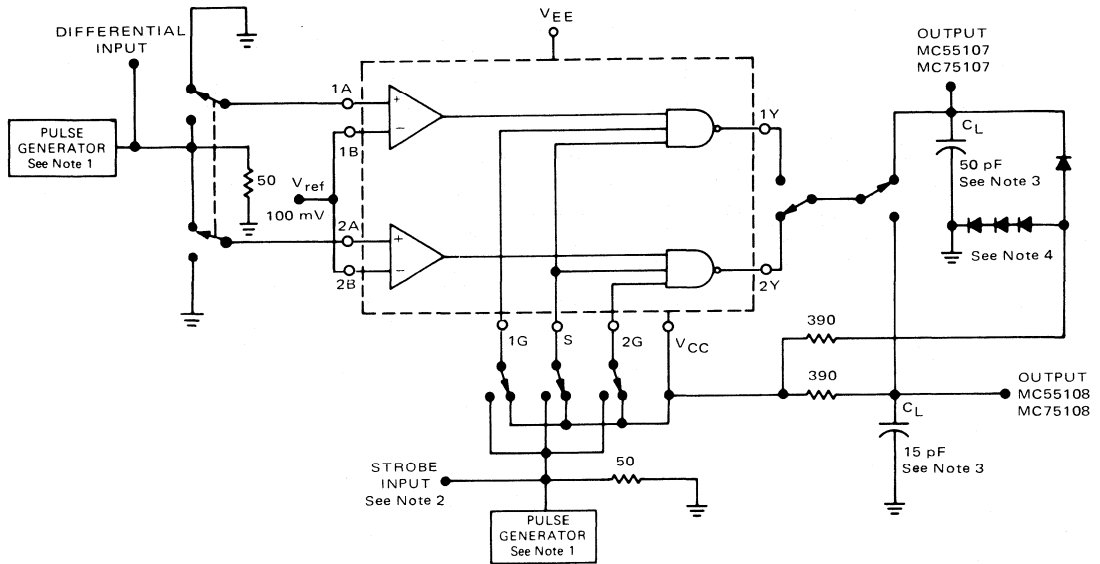
FIGURE 6 - I_{CC} and I_{EE}



MC55107, MC75107, MC55108, MC75108 (continued)

TEST CIRCUITS (continued)

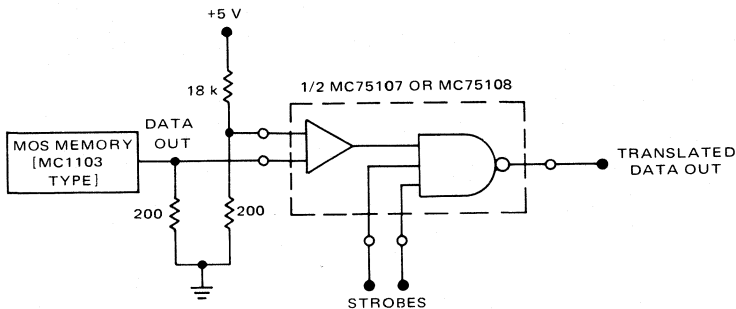
FIGURE 7 – PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



- NOTES: 1. The pulse generators have the following characteristics: $z_o = 50 \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz, $t_{p2} = 1$ ms, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe 1G when Inputs 1A-1B are being tested, to Strobe S when Inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916 or equivalent.

TYPICAL APPLICATION

FIGURE 8 – MOS-TO-TTL TRANSLATOR



MC55109
MC55110
MC75109
MC75110

MONOLITHIC DUAL LINE DRIVERS

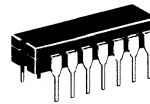
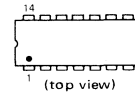
The MC55109/MC75109 and MC55110/75110 dual line drivers feature independent channels with common voltage supply and ground terminals. Each driver circuit provides a constant output current that switches to either of two output terminals subject to the appropriate logic levels at the input terminals. Output current can be switched "off" (inhibited) by appropriate logic levels at the inhibit inputs. Output current is nominally six milliamperes for the MC55109/MC75109 and twelve milliamperes for the MC55110/MC75110.

The inhibit feature permits use in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included to increase driver-logic versatility. With output current in the inhibited mode, $I_{O(off)}$ is specified so that minimum line loading occurs when the driver is used in a party-line system with other drivers. Output impedance of the driver in inhibited mode is very high (the output impedance of a transistor biased to cutoff).

All driver outputs have a common-mode voltage range of -3.0 volts to +10 volts, allowing common-mode voltage on the line without affecting driver performance.

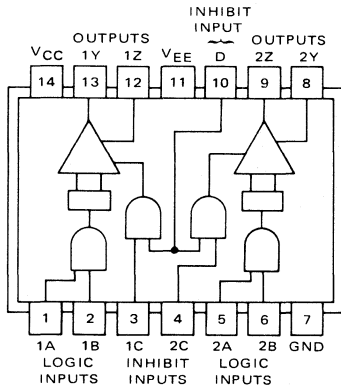
- Insensitive to Supply Variations Over the Entire Operating Range
- MTTL Input Compatibility
- Current-Mode Output (6.0 mA or 12 mA typical)
- High Output Impedance
- High Common-Mode Output Voltage Range (-3.0 V to +10 V)
- Inhibitor Available for Driver Selection

DUAL LINE DRIVERS
 MONOLITHIC SILICON
 INTEGRATED CIRCUIT



L SUFFIX
 CERAMIC PACKAGE
 CASE 632
 (TO-116)

P SUFFIX
 PLASTIC PACKAGE
 CASE 646
 (TO-116)
 (MC75109, MC75110 only)



TRUTH TABLE

| LOGIC INPUTS | | INHIBITOR INPUTS | | OUTPUTS | |
|--------------|--------|------------------|--------|---------|---|
| A | B | C | D | Y | Z |
| L or H | L or H | L | L or H | H | H |
| L or H | L or H | L or H | L | H | H |
| L | L or H | H | H | L | H |
| L or H | L | H | H | L | H |
| H | H | H | H | H | L |

Low output represents the "on" state.
 High output represents the "off" state.

MC55109, MC75109, MC55110, MC75110 (continued)

MAXIMUM RATINGS ($T_A = T_{low}^*$ to T_{high}^* unless otherwise noted)

| Ratings | Symbol | Value | Unit |
|--|----------------------|----------------------------|-----------------------|
| Power Supply Voltages (See Note 1) | V_{CC} V_{EE} | +7.0 -7.0 | Volts |
| Logic and Inhibitor Input Voltages (See Note 1) | V_{in} | 5.5 | Volts |
| Common-Mode Output Voltage Range (See Note 1) | V_{OCR} | -5.0 to +12 | Volts |
| Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above $T_A = +25^{\circ}C$ | P_D | 675 3.85 | mW mW/ $^{\circ}C$ |
| Operating Temperature Range MC55109, MC55110 MC75109, MC75110 | T_A | -55 to +125 0 to +70 | $^{\circ}C$ |
| Storage Temperature Range Ceramic Dual In-Line Package Plastic Dual In-Line Package | T_{stg} | -65 to +150 -55 to +150 | $^{\circ}C$ |

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2)

| Characteristic | Symbol | MC55109/MC55110 | | | MC75109/MC75110 | | | Unit |
|----------------------------------|----------------------|-----------------|--------------|--------------|-----------------|--------------|----------------|-------|
| | | Min | Nom | Max | Min | Nom | Max | |
| Power Supply Voltages | V_{CC} V_{EE} | +4.5 -4.5 | +5.0 -5.0 | +5.5 -5.5 | +4.75 -4.75 | +5.0 -5.0 | +5.25 -5.25 | Volts |
| Common-Mode Output Voltage Range | V_{OCR} | | | | | | | Volts |
| Positive | | 0 | — | +10 | 0 | — | +10 | |
| Negative | | 0 | — | -3.0 | 0 | — | -3.0 | |

Note 1. These voltage values are in respect to the ground terminal.

Note 2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

DEFINITIONS OF INPUT LOGIC LEVELS**

| Characteristic | Symbol | Test Fig. | Min | Max | Unit |
|---|----------|-----------|-----|-----|-------|
| High-Level Input Voltage (at any input) | V_{IH} | 1,2 | 2.0 | 5.5 | Volts |
| Low-Level Input Voltage (at any input) | V_{IL} | 1,2 | 0 | 0.8 | Volts |

**The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

7

MC55109, MC75109, MC55110, MC75110 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = T_{low}^*$ to T_{high}^* unless otherwise noted.)

| Characteristic # | Symbol | Test Fig. | MC55109/MC75109 | | | MC55110/MC75110 | | | Unit |
|--|----------------------|-----------|-----------------|-------|------------|-----------------|-------|-----------|---------------------|
| | | | Min | Typ # | Max | Min | Typ # | Max | |
| High-Level Input Current to 1A, 1B, 2A or 2B ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_L} = 2.4 \text{ V}$)# ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_L} = V_{CC} \text{ Max}$) | I_{IH_L} | 1 | - | - | 40 1.0 | - | - | 40 1.0 | μA mA |
| Low-Level Input Current to 1A, 1B, 2A or 2B ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL_L} = 0.4 \text{ V}$) | I_{IL_L} | 1 | - | - | -3.0 | - | - | -3.0 | mA |
| High-Level Input Current into 1C or 2C ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_I} = 2.4 \text{ V}$) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_I} = V_{CC} \text{ Max}$) | I_{IH_I} | 2 | - | - | 40 1.0 | - | - | 40 1.0 | μA mA |
| Low-Level Input Current into 1C or 2C ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL_I} = 0.4 \text{ V}$) | I_{IL_I} | 2 | - | - | -3.0 | - | - | -3.0 | mA |
| High-Level Input Current into D ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_I} = 2.4 \text{ V}$) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IH_I} = V_{CC} \text{ Max}$) | I_{IH_I} | 2 | - | - | 80 2.0 | - | - | 80 2.0 | μA mA |
| Low-Level Input Current into D ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$, $V_{IL_I} = 0.4 \text{ V}$) | I_{IL_I} | 2 | - | - | -6.0 | - | - | -6.0 | mA |
| Output Current ("on" state) ($V_{CC} = \text{Max}$, $V_{EE} = \text{Max}$) ($V_{CC} = \text{Min}$, $V_{EE} = \text{Max}$) | $I_{O(\text{on})}$ | 3 | - | - | 7.0 3.5 | - | - | 15 - | mA |
| Output Current ("off" state) ($V_{CC} = \text{Min}$, $V_{EE} = \text{Min}$) | $I_{O(\text{off})}$ | 3 | - | - | 100 | - | - | 100 | μA |
| Supply Current from V_{CC} (with driver enabled) ($V_{IL_L} = 0.4 \text{ V}$, $V_{IH_I} = 2.0 \text{ V}$) | $I_{CC(\text{on})}$ | 4 | - | 25 | 30 | - | 28 | 35 | mA |
| Supply Current from V_{EE} (with driver enabled) ($V_{IL_L} = 0.4 \text{ V}$, $V_{IH_I} = 2.0 \text{ V}$) | $I_{EE(\text{on})}$ | 4 | - | -23 | -30 | - | -41 | -50 | mA |
| Supply Current from V_{CC} (with driver inhibited) ($V_{IL_L} = 0.4 \text{ V}$, $V_{IL_I} = 0.4 \text{ V}$) | $I_{CC(\text{off})}$ | 4 | - | 18 | - | - | 21 | - | mA |
| Supply Current from V_{EE} (with driver inhibited) ($V_{IL_L} = 0.4 \text{ V}$, $V_{IL_I} = 0.4 \text{ V}$) | $I_{EE(\text{off})}$ | 4 | - | -10 | - | - | -17 | - | mA |

* $T_{low} = -55^{\circ}\text{C}$ for MC55109 and MC55110 $T_{high} = +125^{\circ}\text{C}$ for MC55109 and MC55110
= 0 for MC75109 and MC75110 = $+70^{\circ}\text{C}$ for MC75109 and MC75110

#All typical values are at $V_{CC} = +5.0 \text{ V}$, $V_{EE} = -5.0 \text{ V}$.

#For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.

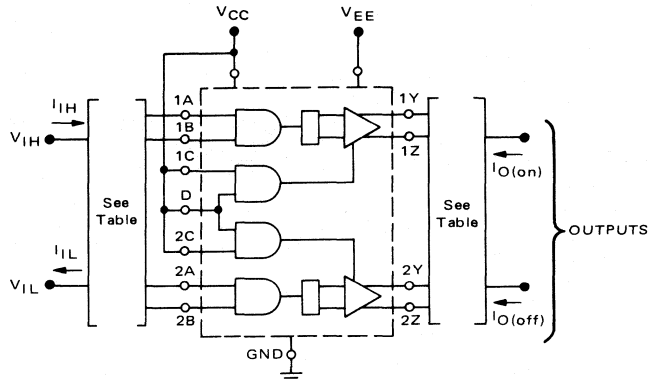
SWITCHING CHARACTERISTICS ($V_{CC} = +5.0 \text{ V}$, $V_{EE} = -5.0 \text{ V}$, $T_A = +25^{\circ}\text{C}$)

| Characteristic | Symbol | Test Fig. | Min | Typ | Max | Unit |
|---|-------------|-----------|-----|-----|-----|------|
| Propagation Delay Time from Logic Input A or B to Output Y or Z ($R_L = 50 \text{ ohms}$, $C_L = 40 \text{ pF}$) | t_{PLH_L} | 5 | - | 9.0 | 15 | ns |
| | t_{PHL_L} | | - | 9.0 | 15 | |
| Propagation Delay Time from Inhibitor Input C or D to Output Y or Z ($R_L = 50 \text{ ohms}$, $C_L = 40 \text{ pF}$) | t_{PLH_I} | 5 | - | 16 | 25 | ns |
| | t_{PHL_I} | | - | 13 | 25 | |

Symbols conform to JEDEC Bulletin No. 1 when applicable.

TEST CIRCUITS

FIGURE 1 - V_{IH} , V_{IL} , I_{IH} , and I_{IL}

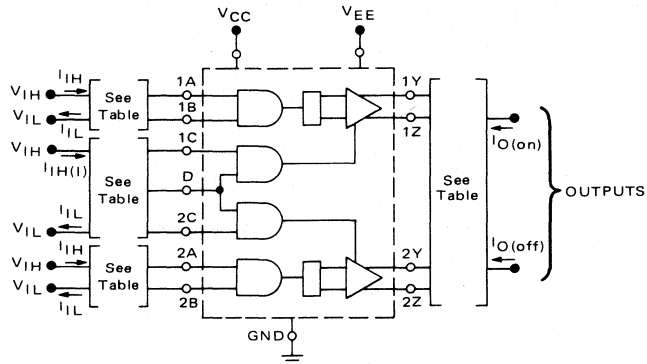


TEST TABLE

| TEST AT ANY LOGIC INPUT | LOGIC INPUTS NOT UNDER TEST | ALL INHIBITOR INPUTS | OUTPUT 1Y or 2Y | OUTPUT 1Z or 2Z |
|-------------------------|-----------------------------|----------------------|-----------------|-----------------|
| V_{IHL} | Open | V_{IH_I} | H (See Note 1) | L (See Note 1) |
| V_{ILL} | V_{CC} | V_{IH_I} | L (See Note 1) | H (See Note 1) |
| I_{IHL} | 4.5 V | V_{IH_I} | Gnd | Gnd |
| I_{ILL} | Gnd | V_{IH_I} | Gnd | Gnd |

- NOTES:
1. Low output represents the "on" state, high output represents the "off" state.
 2. Each input is tested separately.
 3. Arrows indicate actual direction of current flow.

FIGURE 2 - V_{IH} , V_{IL} , I_{IH} , I_{IL}

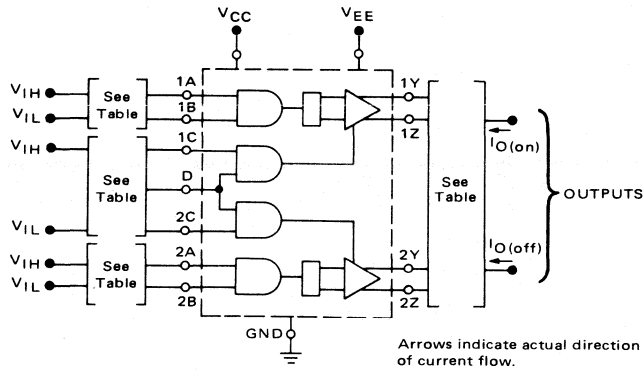


TEST TABLE

| TEST AT ANY INHIBITOR INPUT | ALL LOGIC INPUTS | INHIBITOR INPUTS NOT UNDER TEST | OUTPUT 1Y or 2Y | OUTPUT 1Z or 2Z |
|-----------------------------|------------------|---------------------------------|-----------------|-----------------|
| V_{IH_I} | V_{IHL} | Open | H(See Note 1) | L(See Note 1) |
| | V_{ILL} | Open | L(See Note 1) | H(See Note 1) |
| V_{IL_I} | V_{IHL} | V_{CC} | H(See Note 1) | H(See Note 1) |
| | V_{ILL} | V_{CC} | H(See Note 1) | H(See Note 1) |
| I_{IH_I} | Gnd | 4.5 V | Gnd | Gnd |
| I_{IL_I} | Gnd | Gnd | Gnd | Gnd |

TEST CIRCUITS (continued)

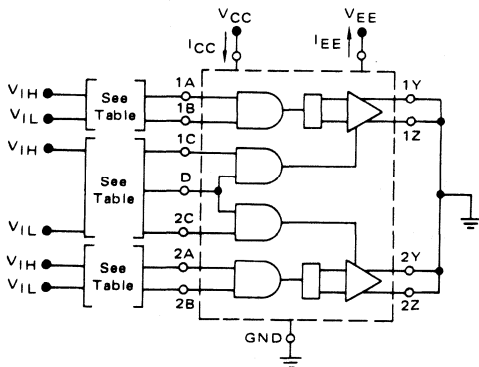
FIGURE 3— $I_{O(on)}$ and $I_{O(off)}$



TEST TABLE

| TEST | | LOGIC INPUTS | | INHIBITOR INPUTS | |
|--------------|-----------------------------|--------------|--------------|------------------|----------|
| | | 1A or 2A | 1B or 2B | 1C or 2C | D |
| $I_{O(on)}$ | at output 1Y or 2Y | V_{IL} | V_{IL} | V_{IH} | V_{IH} |
| | | V_{IL} | V_{IH} | | |
| | | V_{IH} | V_{IL} | | |
| $I_{O(on)}$ | at output 1Z or 2Z | V_{IH} | V_{IH} | V_{IH} | V_{IH} |
| $I_{O(off)}$ | at output 1Y or 2Y | V_{IH} | V_{IH} | V_{IH} | V_{IH} |
| $I_{O(off)}$ | at output 1Z or 2Z | V_{IL} | V_{IL} | V_{IH} | V_{IH} |
| | | V_{IL} | V_{IH} | | |
| | | V_{IH} | V_{IL} | | |
| $I_{O(off)}$ | at output 1Y, 2Y, 1Z, or 2Z | Either state | Either state | V_{IL} | V_{IL} |
| | | | | V_{IL} | V_{IH} |
| | | | | V_{IH} | V_{IL} |

FIGURE 4— I_{CC} and I_{EE}

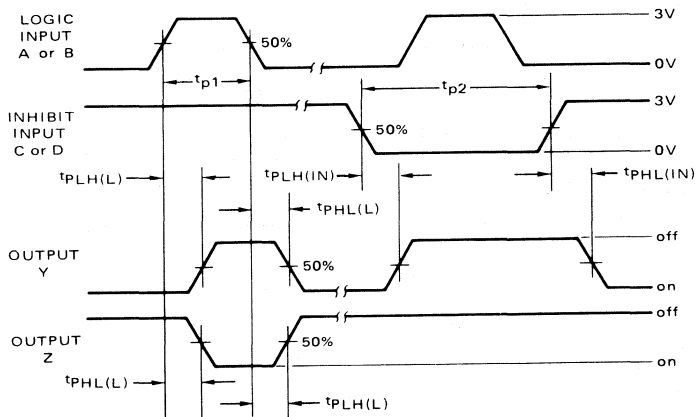
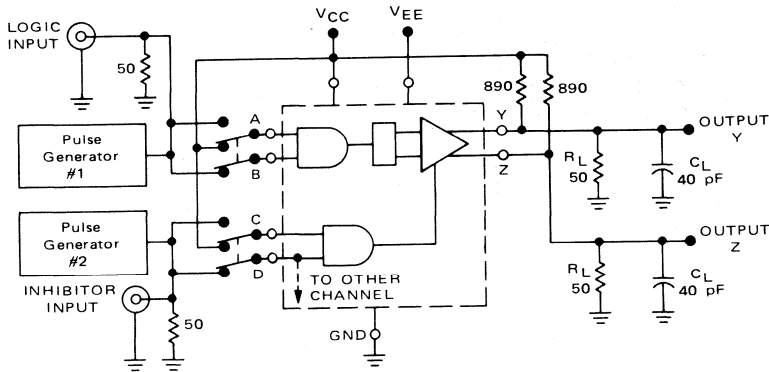


TEST TABLE

| TEST | | ALL LOGIC INPUTS | ALL INHIBITOR INPUTS |
|---------------|------------------|------------------|----------------------|
| $I_{CC(on)}$ | Driver enabled | V_{IL} | V_{IH} |
| $I_{EE(on)}$ | Driver enabled | V_{IL} | V_{IH} |
| $I_{CC(off)}$ | Driver inhibited | V_{IL} | V_{IL} |
| $I_{EE(off)}$ | Driver inhibited | V_{IL} | V_{IL} |

TEST CIRCUITS (continued)

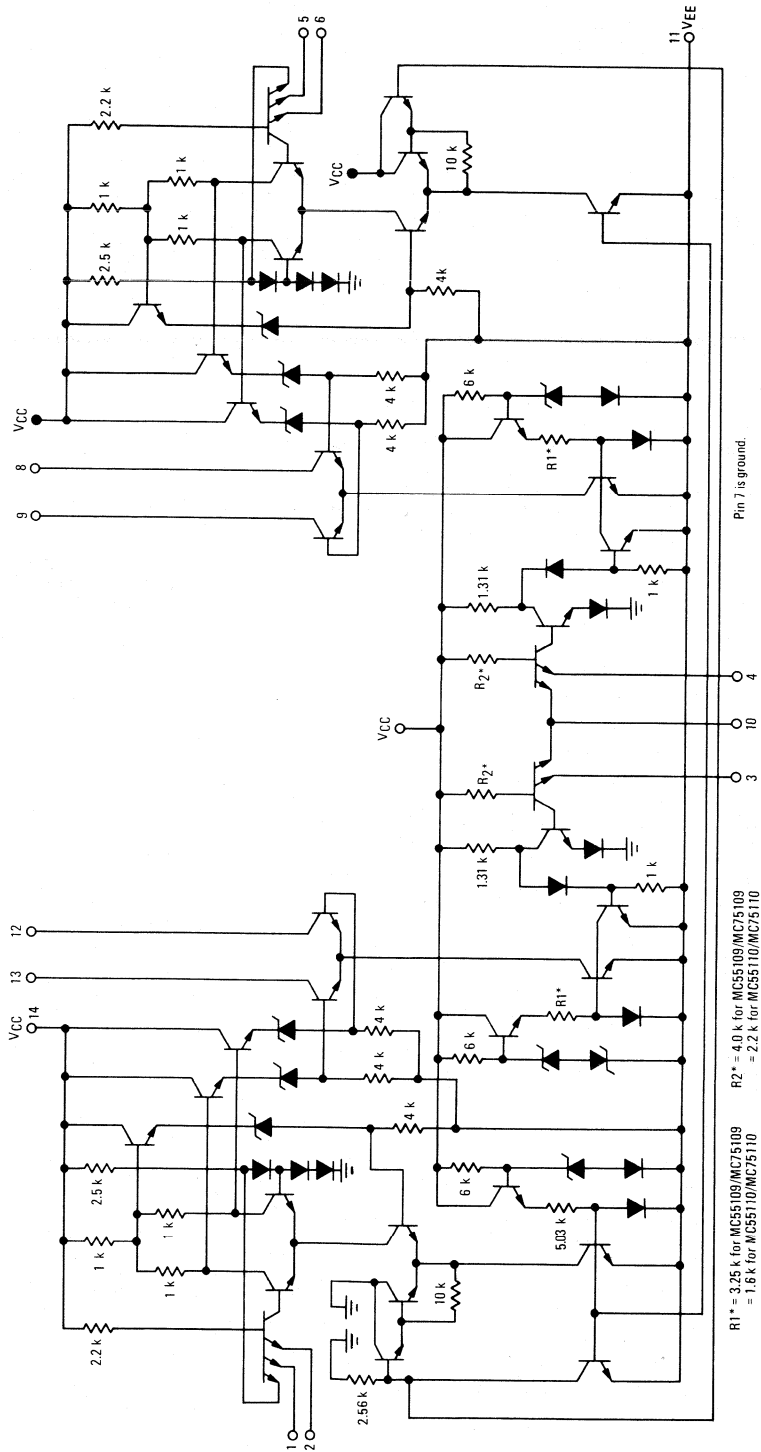
FIGURE 5 – PROPAGATION DELAY TIMES TEST CIRCUIT AND WAVEFORMS



- NOTES: 1. The pulse generators have the following characteristics: $z_o = 50 \Omega$, $t_r = t_f = 10 \pm 5 \text{ ns}$, $t_{p1} = 500 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$, $t_{p2} = 1 \text{ ms}$, $\text{PRR} = 500 \text{ kHz}$.
 2. C_L includes probe and jig capacitance.
 3. For simplicity, only one channel and the inhibitor connections are shown.

MC55109, MC75109, MC55110, MC75110 (continued)

CIRCUIT DIAGRAM



DUAL MEMORY DRIVER

MC55325

MC75325

Advance Information

DUAL MEMORY DRIVER

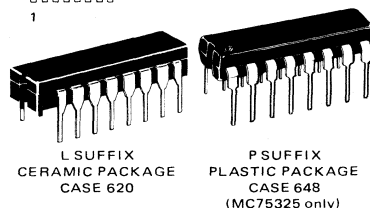
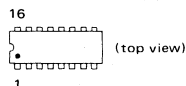
The MC55325/75325 is a monolithic integrated circuit memory driver with logic inputs, and is designed for use with magnetic memories.

The device contains two 600-mA source-switch pairs and two 600-mA sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. With this arrangement selection of one of the four switches provides turn-on with minimum time skew of the output current rise.

- 600-mA Output Capability
- Output Short-Circuit Protection
- Input Clamp Diodes
- Dual Sink and Dual Source Outputs
- MDTL and M TTL Compatibility
- 24-Volt Output Capability

DUAL MEMORY DRIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT



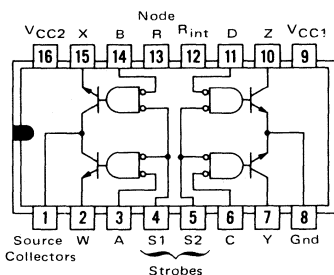
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC75325 only)

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|-----------|-------------|----------------------|
| Supply Voltage (Note 1) | V_{CC1} | 7.0 | Vdc |
| | V_{CC2} | 25 | Vdc |
| Input Voltage | V_{in} | 5.5 | Vdc |
| Power Dissipation (Package Limitation) Ceramic and Plastic Dual In-Line Pkg. Derate above $T_A = +25^\circ\text{C}$ | P_D | 1.0 | W |
| | | 6.6 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| | | 0 to +70 | |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

Note 1. Voltage values are with respect to the network ground terminal.



SWITCHING CHARACTERISTICS ($V_{CC1} = 5.0\text{ V}$, $C_L = 25\text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | ns | |
|---|--------------------------|-----------|-----|
| | | Typ | Max |
| Propagation Delay Time to Source Collectors ($V_{CC2} = 15\text{ V}$, $R_L = 24\text{ ohms}$) | Low-to-High-Level Output | t_{PLH} | 25 |
| | High-to-Low-Level Output | t_{PHL} | 50 |
| Transition Time to Source Outputs ($V_{CC2} = 20\text{ V}$, $R_L = 1\text{ k ohms}$) | Low-to-High-Level Output | t_{TLH} | 55 |
| | High-to-Low-Level Output | t_{THL} | 7.0 |
| Propagation Delay Time to Sink Outputs ($V_{CC2} = 15\text{ V}$, $R_L = 24\text{ ohms}$) | Low-to-High-Level Output | t_{PLH} | 20 |
| | High-to-Low-Level Output | t_{PHL} | 45 |
| Transition Time to Sink Outputs ($V_{CC2} = 15\text{ V}$, $R_L = 24\text{ ohms}$) | Low-to-High-Level Output | t_{TLH} | 7.0 |
| | High-to-Low-Level Output | t_{THL} | 9.0 |
| Storage Time to Sink Outputs ($V_{CC2} = 15\text{ V}$, $R_L = 24\text{ ohms}$) | t_s | 15 | 30 |

TRUTH TABLE

| ADDRESS INPUTS | | | | STROBE INPUTS | | OUTPUTS | | | |
|----------------|---|-----------|---|---------------|------------|-------------|-----|-----------|-----|
| SOURCE A | B | SINK C | D | SOURCE S1 | SINK S2 | SOURCE W | X | SINK Y | Z |
| L | H | X | X | L | H | On | Off | Off | Off |
| H | L | X | X | L | H | Off | On | Off | Off |
| X | X | L | H | H | L | Off | Off | On | Off |
| X | X | H | L | H | L | Off | Off | Off | On |
| X | X | X | X | H | H | Off | Off | Off | Off |
| H | H | H | H | X | X | Off | Off | Off | Off |

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at any one time.

This is advance information on a new introduction and specifications are subject to change without notice.

See Packaging Information Section for outline dimensions.

MC55325, MC75325 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = T_{low\#}$ to $T_{high\#}$ unless otherwise noted.

| Characteristic | Symbol | MC55325 | | | MC75325 | | | Unit |
|---|---------------|---------|------|------|---------|------|------|---------------|
| | | Min | Typ* | Max | Min | Typ* | Max | |
| High-Level Input Voltage | V_{IH} | 2.0 | — | — | 2.0 | — | — | V |
| Low-Level Input Voltage | V_{IL} | — | — | 0.8 | — | — | 0.8 | V |
| Input Clamp Voltage ($V_{CC1} = 4.5$ V, $V_{CC2} = 24$ V, $I_I = -10$ mA, $T_A = 25^\circ\text{C}$) | V_I | — | -1.3 | -1.7 | — | -1.3 | -1.7 | V |
| Off-State Current, Source-Collectors Terminal ($V_{CC1} = 4.5$ V, $V_{CC2} = 24$ V) $T_A = T_{low}$ to T_{high} $T_A = 25^\circ\text{C}$ | I_{off} | — | — | 500 | — | — | 200 | μA |
| High-Level Sink Output Voltage ($V_{CC1} = 4.5$ V, $V_{CC2} = 24$ V, $I_O = 0$) | V_{OH} | 19 | 23 | — | 19 | 23 | — | V |
| Saturation Voltage** Source Outputs ($V_{CC1} = 4.5$ V, $V_{CC2} = 15$ V, $I_{source} \approx -600$ mA, $R_L = 24$ ohms, Note 2) $T_A = T_{low}$ to T_{high} $T_A = 25^\circ\text{C}$ Sink Outputs ($V_{CC1} = 4.5$ V, $V_{CC2} = 15$ V, $I_{sink} \approx 600$ mA, $R_L = 24$ ohms, Note 2) $T_A = T_{low}$ to T_{high} $T_A = 25^\circ\text{C}$ | V_{sat} | — | — | 0.9 | — | — | 0.9 | V |
| Input Current at Maximum Input Voltage ($V_{CC1} = 5.5$ V, $V_{CC2} = 24$ V, $V_I = 5.5$ V) Address Inputs Strobe Inputs | I_I | — | — | 1.0 | — | — | 1.0 | mA |
| High-Level Input Current ($V_{CC1} = 5.5$ V, $V_{CC2} = 24$ V, $V_I = 2.4$ V) Address Inputs Strobe Inputs | I_{IH} | — | 3.0 | 40 | — | 3.0 | 40 | μA |
| Low-Level Input Current ($V_{CC1} = 5.5$ V, $V_{CC2} = 24$ V, $V_I = 0.4$ V) Address Inputs Strobe Inputs | I_{IL} | — | -1.0 | -1.6 | — | -1.0 | -1.6 | mA |
| Supply Current, All Sources and Sinks "Off" ($V_{CC1} = 5.5$ V, $V_{CC2} = 24$ V, $T_A = 25^\circ\text{C}$) From V_{CC1} From V_{CC2} | $I_{CC(off)}$ | — | 14 | 22 | — | 14 | 22 | mA |
| Supply Current from V_{CC1} , Either Sink "On" ($V_{CC1} = 5.5$ V, $V_{CC2} = 24$ V, $I_{sink} = 50$ mA, $T_A = 25^\circ\text{C}$) | I_{CC1} | — | 55 | 70 | — | 55 | 70 | mA |
| Supply Current from V_{CC2} , Either Source "On" ($V_{CC1} = 5.5$ V, $V_{CC2} = 24$ V, $I_{source} = -50$ mA, $T_A = 25^\circ\text{C}$) | I_{CC2} | — | 32 | 50 | — | 32 | 50 | mA |

*All typical values are at $T_A = 25^\circ\text{C}$.

$T_{low} = -55^\circ\text{C}$ for MC55325, 0°C for MC75325

**Not more than one output is to be "on" at any one time.

$T_{high} = +125^\circ\text{C}$ for MC55325, $+70^\circ\text{C}$ for MC75325

NOTE 2. Saturation voltage must be measured using pulse techniques: pulse width = 200 μs , duty cycle $\leq 2\%$.

MC75113L

TWISTED-PAIR LINE DRIVER

Advance Information

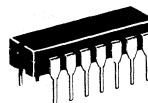
TWISTED-PAIR LINE DRIVER

... designed for use in high-speed data transmission systems which use balanced terminated transmission lines. The MC75113's push-pull output eliminates ground loop and cross-talk problems. When all the inputs are at logic "0", no current flows through either output, making it ideal for party-line operation.

- Push-Pull Drive Capability, ± 20 mA
- Current Gated "Off" for Party-Line Operation
- MTTL and MDTL Compatible Inputs
- Wide Common-Mode Output Voltage Range:
 ± 3.0 Volts typical

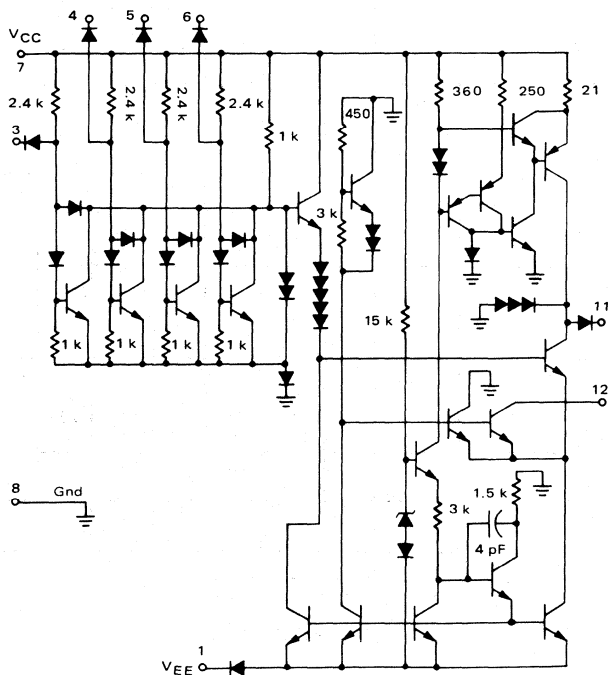
DIFFERENTIAL PARTY-LINE DRIVER

MONOLITHIC SILICON
INTEGRATED CIRCUIT

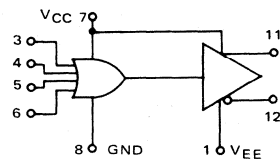


CERAMIC PACKAGE
CASE 632
TO-116

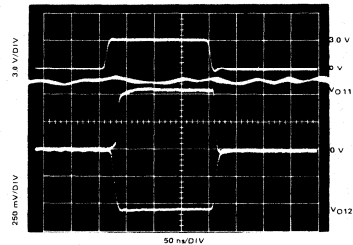
CIRCUIT DIAGRAM



BLOCK DIAGRAM



TYPICAL OPERATION



This is advance information and specifications are subject to change without notice. See Packaging Information Section for outline dimensions.

MC75113L (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|-------------------------------------|-------------|-------------|
| Positive Power Supply Voltage (Pin 7) | V _{CC} | +8.0 | Volts |
| Negative Power Supply Voltage (Pin 1) | V _{EE} | -8.0 | Volts |
| Positive Input Voltage (Pins 3,4,5,6) | V _{in} | +8.0 | Volts |
| Negative Input Voltage (Pins 3,4,5,6) | V _{in} | -4.0 | Volts |
| Output Voltage (Pins 11,12) | V _O | +8.0/-3.0 | Volts |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |
| Operating Temperature Range | T _A | 0 to +75 | °C |
| Power Dissipation (Package Limitation) Derate Above T _A = +25°C | P _D 1/θ _{JA} | 1000 6.7 | mW mW/°C |

ELECTRICAL CHARACTERISTICS (T_A = 0 to +75°C unless otherwise noted.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|--------|------------------|------|------|------|------|
| Positive Power Supply Current | 1 | I _{CC} | — | +46 | +61 | mA |
| Negative Power Supply Current | 1 | I _{EE} | — | -32 | -44 | mA |
| Positive Output Current (short circuit) | 2 | I _{O11} | +18 | +20 | +26 | mA |
| Negative Output Current (short circuit) | 2 | I _{O12} | -18 | -20 | -26 | mA |
| Differential Output Current | 3 | ΔI _O | — | ±2.0 | — | mA |
| Positive Output "ON" Common-Mode Range | 4 | V _{O1} | +2.7 | — | — | V |
| Negative Output "ON" Common-Mode Range | 4 | V _{O2} | -2.7 | — | — | V |
| Positive Output "OFF" Common-Mode Range | 5 | V _{O3} | +3.0 | — | — | V |
| Negative Output "OFF" Common-Mode Range | 5 | V _{O4} | -2.5 | — | — | V |
| Positive Output "OFF" Common-Mode Range | 6 | V _{O5} | -2.4 | — | — | V |
| Negative Output "OFF" Common-Mode Range | 6 | V _{O6} | +3.0 | — | — | V |
| Power Off Positive Output Common-Mode Range | 7 | V _{O7} | -2.0 | — | — | V |
| Power Off Negative Output Common-Mode Range | 7 | V _{O8} | -2.0 | — | — | V |
| Forward Input Current | 8 | I _{IF} | — | — | -2.6 | mA |
| Reverse Input Current | 8 | I _{IR} | — | — | +50 | μA |

SWITCHING CHARACTERISTICS (T_A = +25°C unless otherwise noted, see Figure 9)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---------------------|-----|-----|-----|------|
| "ON" Propagation Delay (Positive Output) | t _{on 11} | — | 25 | 30 | ns |
| Rise Time (Positive Output) | t _{r 11} | — | 10 | 15 | ns |
| "OFF" Propagation Delay (Positive Output) | t _{off 11} | — | 15 | 20 | ns |
| Fall Time (Positive Output) | t _{f 11} | — | 10 | 15 | ns |
| "ON" Propagation Delay (Negative Output) | t _{on 12} | — | 25 | 30 | ns |
| Rise Time (Negative Output) | t _{r 12} | — | 10 | 15 | ns |
| "OFF" Propagation Delay (Negative Output) | t _{off 12} | — | 15 | 20 | ns |
| Fall Time (Negative Output) | t _{f 12} | — | 10 | 15 | ns |

*Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

MC75113L (continued)

TEST CIRCUITS

TABLE I – INPUT LOGIC VOLTAGE FOR TEST CIRCUITS

| Temperature (°C) | V _{inL} (VOLTS) | V _{inH} (VOLTS) |
|------------------|--------------------------|--------------------------|
| 0° | 1.16 | 1.85 |
| +25° | 1.08 | 1.78 |
| +75° | 0.94 | 1.64 |

FIGURE 1 – POWER SUPPLY CURRENTS

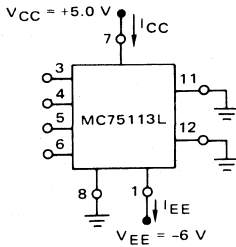


FIGURE 2 – POSITIVE and NEGATIVE OUTPUT CURRENTS (Short Circuit)

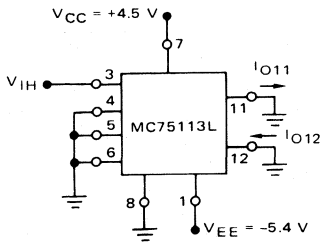


FIGURE 3 – DIFFERENTIAL OUTPUT CURRENT

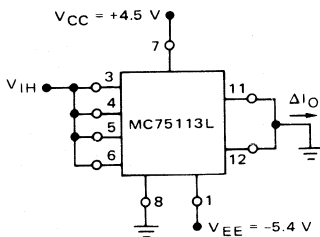


FIGURE 4 – OUTPUT "ON" POSITIVE and NEGATIVE OUTPUT COMMON-MODE RANGE

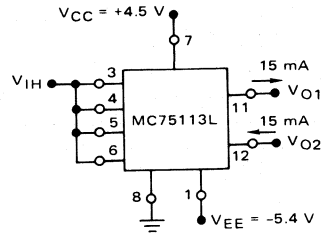


FIGURE 5 – OUTPUT "OFF" POSITIVE and NEGATIVE OUTPUT COMMON-MODE RANGE

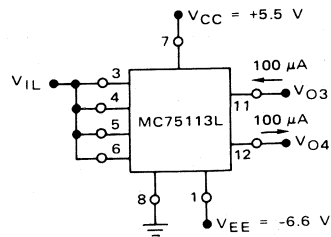


FIGURE 6 – OUTPUT "OFF" POSITIVE and NEGATIVE OUTPUT COMMON-MODE RANGE

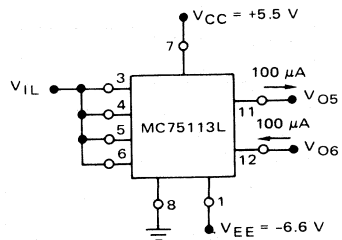
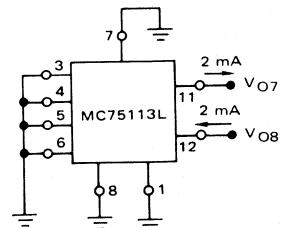


FIGURE 7 – POWER "OFF" POSITIVE and NEGATIVE OUTPUT COMMON-MODE RANGE



TEST CIRCUITS (continued)

FIGURE 8 – INPUT CURRENT TESTS

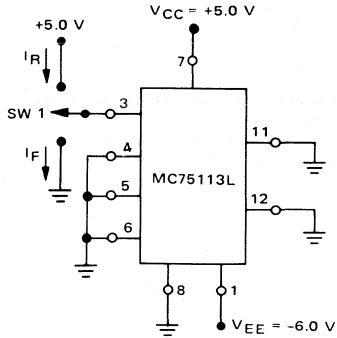
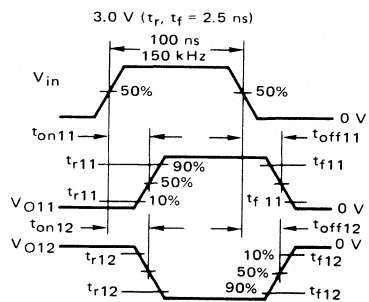
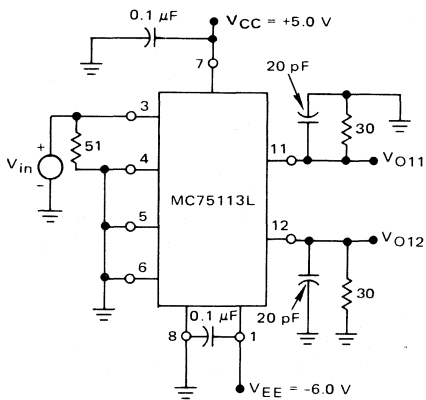


FIGURE 9 – AC TEST CIRCUIT and WAVEFORMS



MC75450

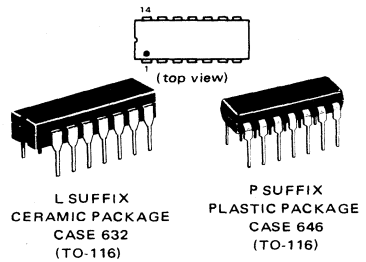
PERIPHERAL DRIVER

DUAL PERIPHERAL POSITIVE "AND" DRIVER

The MC75450 is a versatile device designed for use as a general-purpose dual interface circuit in MDTL and MTTL type systems. This device features two standard MTTL gates and two noncommitted, high-current, high-voltage NPN transistors. Typical applications include relay and lamp drivers, power drivers, MOS and memory drivers.

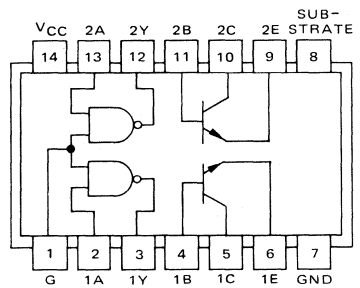
- MDTL and MTTL Compatibility
- 300 mA Output Current Drive Capability (each transistor)
- Separate Gate and Output Transistor for Maximum Design Flexibility
- High Output Breakdown Voltage:
V_{CER} = 30 Volts minimum

DUAL PERIPHERAL POSITIVE "AND" DRIVER MONOLITHIC SILICON INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

P SUFFIX
PLASTIC PACKAGE
CASE 646
(TO-116)



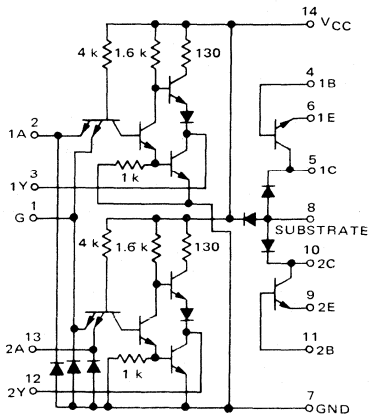
Positive Logic: Y = $\overline{A\overline{B}}$ (gate only)
C = AG (gate and transistor)

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|------------------|-------------|-------------|
| Power Supply Voltage (See Note 1) | V _{CC} | +7.0 | Vdc |
| Input Voltage (See Note 1) | V _{in} | 5.5 | Vdc |
| V _{CC} -to-Substrate Voltage | | 35 | Vdc |
| Collector-to-Substrate Voltage | | 35 | Vdc |
| Collector-Base Voltage | V _{CB} | 35 | Vdc |
| Collector-Emitter Voltage (See Note 2) | V _{CE} | 30 | Vdc |
| Emitter-Base Voltage | V _{EB} | 5.0 | Vdc |
| Collector Current (continuous) (See Note 3) | | 300 | mA |
| Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T _A = +25°C | P _D | 830 6.6 | mW mW/°C |
| Operating Temperature Range | T _A | 0 to +70 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 ohms.
3. Both halves of these dual circuits may conduct the rated current simultaneously.

CIRCUIT SCHEMATIC



MC75450 (continued)

RECOMMENDED OPERATING CONDITIONS (See Note 4)

| Characteristic | Symbol | Min | Nom | Max | Unit |
|----------------|-----------------|------|-----|------|------|
| Supply Voltage | V _{CC} | 4.75 | 5.0 | 5.25 | Vdc |

Note 4. The substrate, pin 8, must always be at the most negative device voltage for proper operation.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

| Characteristic | Symbol | Test Fig. | Min | Typ* | Max | Unit |
|---|--------------------------------------|-----------|-----|------|------|------|
| MTTL GATES | | | | | | |
| High-Level Input Voltage | V _{IH} | 1 | 2.0 | — | — | Vdc |
| Low-Level Input Voltage | V _{IL} | 2 | — | — | 0.8 | Vdc |
| High-Level Output Voltage (V _{CC} = 4.5 V, V _{IL} = 0.8 V, I _{OH} = -400 μA) | V _{OH} | 2 | 2.4 | 3.3 | — | Vdc |
| Low-Level Output Voltage (V _{CC} = 4.75 V, V _{IH} = 2.0 V, I _{OL} = 16 mA) | V _{OL} | 1 | — | 0.22 | 0.4 | Vdc |
| High-Level Input Current (V _{CC} = 5.25 V, V _{in} = 2.4 V) | I _{IH} | 3 | — | — | 40 | μA |
| Input A | | | — | — | 80 | μA |
| Input G (V _{CC} = 5.25 V, V _{in} = 5.5 V) | | | — | — | 1.0 | mA |
| Input A | | | — | — | 2.0 | mA |
| Low-Level Input Current (V _{CC} = 5.25 V, V _{in} = 0.4 V) | I _{IL} | 4 | — | — | -1.6 | mA |
| Input G | | | — | — | -3.2 | mA |
| Short-Circuit Output Current** (V _{CC} = 5.25 V) | I _{OS} | 5 | -18 | — | -55 | mA |
| Supply Current | I _{CCH} I _{CCL} | 6 | — | 2.0 | 4.0 | mA |
| High-Level Output (V _{CC} = 5.25 V, V _{in} = 0) Low-Level Output (V _{CC} = 5.25 V, V _{in} = 5.0 V) | | | — | 6.0 | 11 | |
| Input Clamp Voltage (V _{CC} = 4.75 V, I _{in} = -12 mA) | V _{in} | 4 | — | — | -1.5 | V |

OUTPUT TRANSISTORS

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|----------------------|----------------------|------------------|------------------|------|
| Collector-Base Breakdown Voltage (I _C = 100 μA, I _E = 0) | V _{CB0} | 35 | — | — | Vdc |
| Collector-Emitter Breakdown Voltage (I _C = 100 μA, R _{BE} = 500 ohms) | V _{CER} | 30 | — | — | Vdc |
| Emitter-Base Breakdown Voltage (I _E = 100 μA, I _C = 0) | V _{EBO} | 5.0 | — | — | Vdc |
| Static Forward Transfer Ratio (See Note 5) (V _{CE} = 3.0 V, I _C = 100 mA, T _A = +25°C) (V _{CE} = 3.0 V, I _C = 300 mA, T _A = +25°C) (V _{CE} = 3.0 V, I _C = 100 mA, T _A = 0°C) (V _{CE} = 3.0 V, I _C = 300 mA, T _A = 0°C) | h _{FE} | 25 30 20 25 | — — — — | — — — — | |
| Base-Emitter Voltage (See Note 5) (I _B = 10 mA, I _C = 100 mA) (I _B = 30 mA, I _C = 300 mA) | V _{BE} | — — | 0.85 1.05 | 1.0 1.2 | Vdc |
| Collector-Emitter Saturation Voltage (See Note 5) (I _B = 10 mA, I _C = 100 mA) (I _B = 30 mA, I _C = 300 mA) | V _{CE(sat)} | — — | 0.25 0.5 | 0.4 0.7 | Vdc |

Note 5. These parameters must be measured using pulse techniques; t_w = 300 μs, duty cycle ≤ 2%.

*All typical values at V_{CC} = 5.0 V, T_A = +25°C.

**Not more than one output should be shorted at a time.

MC75450 (continued)

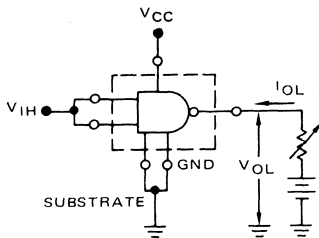
SWITCHING CHARACTERISTICS ($V_{CC} = 5.0 \text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Symbol | Test Fig. | Min | Typ | Max | Unit |
|--|-----------|-----------|-----|-----|-----|------|
| MTTL GATES | | | | | | |
| Propagation Delay Time ($C_L = 15 \text{ pF}$, $R_L = 400 \text{ ohms}$) | | 7 | | | | ns |
| Low-to-High-Level Output | t_{PLH} | | — | 14 | — | |
| High-to-Low-Level Output | t_{PHL} | | — | 6.0 | — | |
| OUTPUT TRANSISTORS # | | | | | | |
| Switching Times ($I_C = 200 \text{ mA}$, $I_{B(1)} = 20 \text{ mA}$, $I_{B(2)} = -40 \text{ mA}$, $V_{BE(\text{off})} = -1.0 \text{ V}$, $C_L = 15 \text{ pF}$, $R_L = 50 \text{ ohms}$) | | 8 | | | | ns |
| Delay Time | t_d | | — | 9.0 | — | |
| Rise Time | t_r | | — | 11 | — | |
| Storage Time | t_s | | — | 14 | — | |
| Fall Time | t_f | | — | 8.0 | — | |
| GATES AND TRANSISTORS COMBINED # | | | | | | |
| Propagation Delay Time ($I_C = 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \text{ ohms}$) | | 9 | | | | ns |
| Low-to-High-Level Output | t_{PLH} | | — | 21 | — | |
| High-to-Low Level Output | t_{PHL} | | — | 16 | — | |
| Transition Time # ($I_C = 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \text{ ohms}$) | | 9 | | | | ns |
| Low-to-High-Level Output | t_{TLH} | | — | 7.0 | — | |
| High-to-Low-Level Output | t_{THL} | | — | 8.0 | — | |

#Voltage and current values are nominal; exact values vary slightly with transistors parameters.
Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

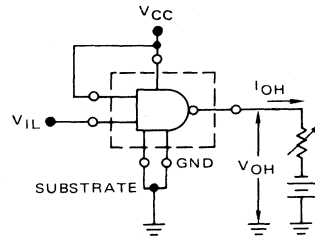
DC TEST CIRCUITS FOR MTTT GATES

FIGURE 1 – V_{IH} , V_{OL}



Both inputs are tested simultaneously.

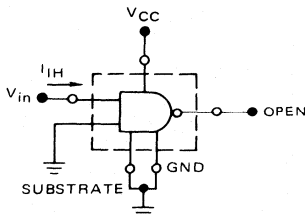
FIGURE 2 – V_{IL} , V_{OH}



Each input is tested separately.

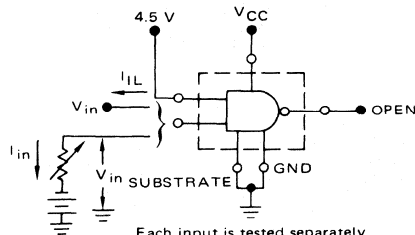
(Arrows indicate actual direction of current flow. Current into a terminal is a positive value.)

FIGURE 3 – I_{IH}



Each input is tested separately.

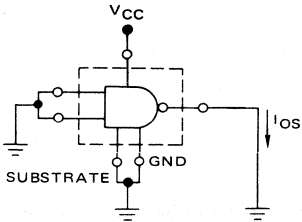
FIGURE 4 – I_{IL} , V_{in}



Each input is tested separately.

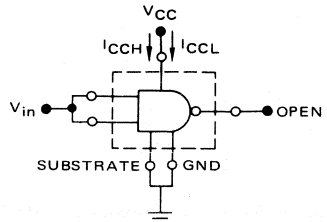
DC TEST CIRCUITS FOR M TTL GATES (continued)

FIGURE 5 - I_{OS}



Each gate is tested separately

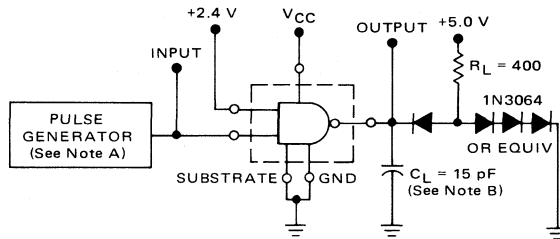
FIGURE 6 - I_{CCH} , I_{CCL}



Both gates are tested simultaneously.

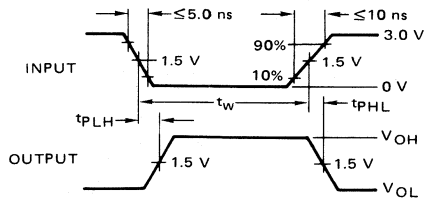
(Arrows indicate actual direction of current flow. Current into a terminal is a positive value.)

FIGURE 7 - PROPAGATION DELAY TIMES, EACH GATE



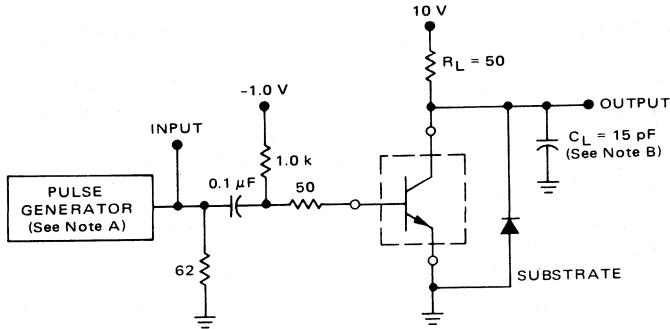
NOTES: A. The pulse generator has the following characteristics: $t_w = 0.5 \mu s$, PRR = 1.0 MHz, $z_o \approx 50 \Omega$.
 B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS



TEST CIRCUITS (continued)

FIGURE 8 – SWITCHING TIMES, EACH TRANSISTOR



NOTES: A. The pulse generator has the following characteristics: $t_w = 0.3 \mu s$, duty cycle $\leq 1\%$, $z_o \approx 50 \Omega$.
 B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS

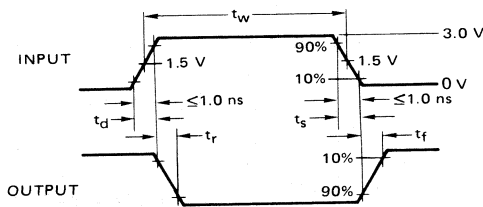
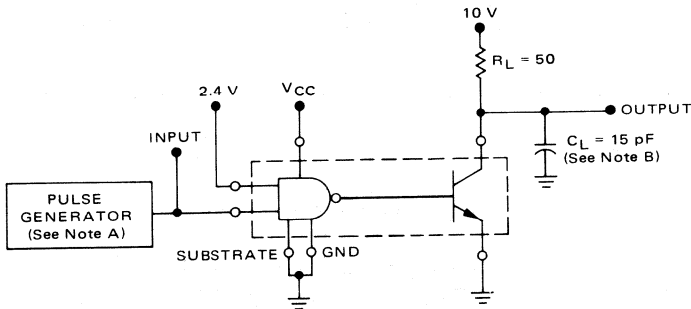
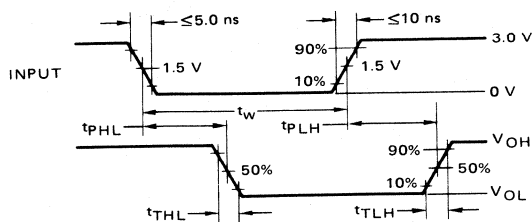


FIGURE 9 – SWITCHING TIMES, GATE AND TRANSISTOR



NOTES: A. The pulse generator has the following characteristics: $t_w = 0.5 \mu s$, PRR = 1.0 MHz, $z_o \approx 50 \Omega$.
 B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS



MC75451P

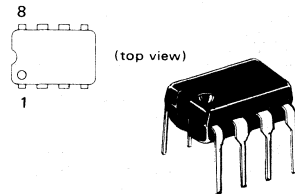
PERIPHERAL DRIVER

DUAL PERIPHERAL POSITIVE "AND" DRIVER

... designed for use as a general-purpose interface circuit in MDTL and MTTL type systems. The MC75451P is a dual peripheral positive AND driver consisting of logic gate outputs internally connected to the bases of two high-current, high-voltage NPN transistors. Typical applications include relay and lamp drivers, power drivers, MOS and memory drivers.

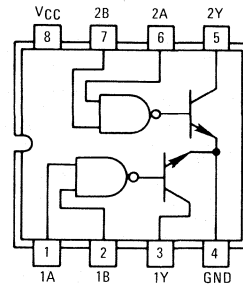
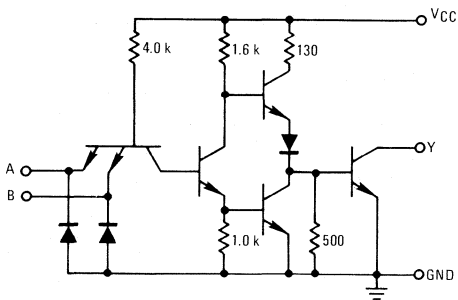
- MDTL and MTTL Compatibility
- 300 mA Output Current Drive Capability (each transistor)
- High Output Breakdown Voltage;
V_{CER} = 30 Volts minimum

DUAL PERIPHERAL POSITIVE "AND" DRIVER MONOLITHIC SILICON INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 626

CIRCUIT SCHEMATIC (1/2 circuit shown)



Positive Logic: Y = AB

MAXIMUM RATINGS (T_A = +25°C)

| Rating | Symbol | Value | Unit |
|---|------------------|-------------|-------------|
| Power Supply Voltage (See Note 1) | V _{CC} | +7.0 | Vdc |
| Input Voltage (See Notes 1 and 2) | V _{in} | 5.5 | Vdc |
| Output Voltage (See Notes 1 and 3) | V _O | 30 | Vdc |
| Output Current (continuous) | I _O | 300 | mA |
| Power Dissipation (Package Limitation) Plastic Dual In-Line Package Derate above T _A = +25°C | P _D | 830 6.6 | mW mW/°C |
| Operating Temperature Range | T _A | 0 to +70 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

NOTE 1. Voltage values are with respect to network ground terminal.

NOTE 2. Input voltage should be zero or positive with respect to device ground terminal.

NOTE 3. This is the maximum voltage which should be applied to any output when it is in the "off" state.

TRUTH TABLE

| A | B | Y |
|---|---|-----------------|
| L | L | L ("on" state) |
| L | H | L ("on" state) |
| H | L | L ("on" state) |
| H | H | H ("off" state) |

H = high level, L = low level

MC75451P (continued)

RECOMMENDED OPERATING CONDITIONS

| Characteristic | Symbol | Min | Nom | Max | Unit |
|----------------|----------|------|-----|------|------|
| Supply Voltage | V_{CC} | 4.75 | 5.0 | 5.25 | Vdc |

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to $+70^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Test Fig. | Min | Typ* | Max | Unit |
|--|------------------------|-----------|--------|-------------|------------|---------------------------------------|
| High-Level Input Voltage | V_{IH} | 1 | 2.0 | — | — | Vdc |
| Low-Level Input Voltage | V_{IL} | 2 | — | — | 0.8 | Vdc |
| Input Clamp Voltage ($V_{CC} = 4.75\text{ V}$, $I_{in} = -12\text{ mA}$) | V_{in} | 4 | — | — | -1.5 | Vdc |
| High-Level Output Current ($V_{CC} = 4.75\text{ V}$, $V_{IH} = 2.0\text{ V}$, $V_{OH} = 30\text{ V}$) | I_{OH} | 1 | — | — | 100 | μA |
| Low-Level Output Voltage ($V_{CC} = 4.75\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OL} = 100\text{ mA}$) ($V_{CC} = 4.75\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OL} = 300\text{ mA}$) | V_{OL} | 2 | — — | 0.25 0.5 | 0.4 0.7 | Vdc |
| High-Level Input Current ($V_{CC} = 5.25\text{ V}$, $V_{in} = 2.4\text{ V}$) ($V_{CC} = 5.25\text{ V}$, $V_{in} = 5.5\text{ V}$) | I_{IH} | 3 | — — | — — | 40 1.0 | μA mA |
| Low-Level Input Current ($V_{CC} = 5.25\text{ V}$, $V_{in} = 0.4\text{ V}$) | I_{IL} | 4 | — | -1.0 | -1.6 | mA |
| Supply Current ($V_{CC} = 5.25\text{ V}$, $V_{in} = 5.0\text{ V}$) ($V_{CC} = 5.25\text{ V}$, $V_{in} = 0$) | I_{CCH} I_{CCL} | 5 | — — | 7.0 52 | 11 65 | mA |
| | | | | | | High-Level Output Low-Level Output |

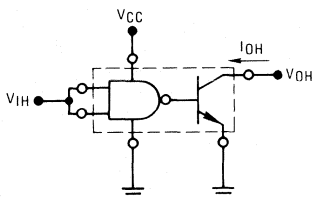
*Typical values are at $V_{CC} = 5.0\text{ V}$, $T_A = +25^\circ\text{C}$.

SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Symbol | Test Fig. | Min | Typ | Max | Unit |
|---|------------------------|-----------|--------|-----------|--------|------|
| Propagation Delay Time ($I_O \approx 200\text{ mA}$, $C_L = 15\text{ pF}$, $R_L = 50\text{ ohms}$) Low-to-High-Level Output High-to-Low-Level Output | t_{PLH} t_{PHL} | 6 | — — | 17 18 | — — | ns |
| Transition Time ($I_O \approx 200\text{ mA}$, $C_L = 15\text{ pF}$, $R_L = 50\text{ ohms}$) Low-to-High-Level Output High-to-Low-Level Output | t_{TLH} t_{THL} | 6 | — — | 6.0 11 | — — | ns |

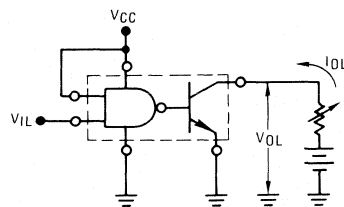
Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

FIGURE 1 – V_{IH} , I_{OH}



TEST CIRCUITS

FIGURE 2 – V_{IL} , V_{OL}



Each input is tested separately.

TEST CIRCUITS (continued)

FIGURE 3 – I_{IH}

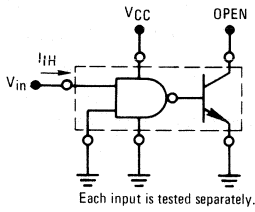


FIGURE 4 – I_{IL} , V_{in}

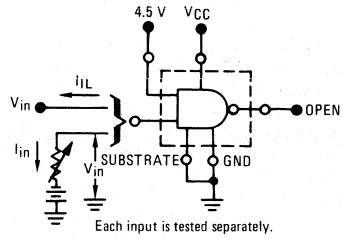


FIGURE 5 – I_{CCH} , I_{CCL}

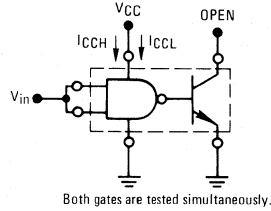
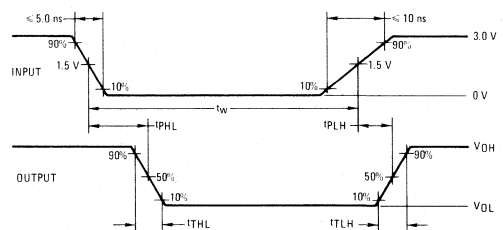
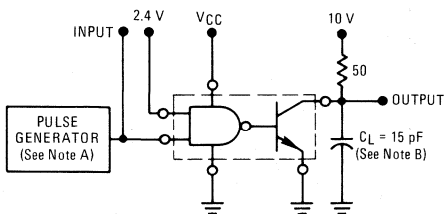


FIGURE 6 – SWITCHING TIMES AND WAVEFORMS



MCBC1709 MCB1709F

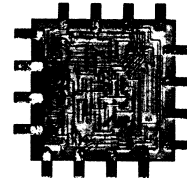
MONOLITHIC OPERATIONAL AMPLIFIER

Beam-lead sealed-junction technology and fabrication make the MCBC1709 and MCB1709F devices excellent choices for military, aerospace, and commercial applications; usages requiring a high degree of reliability under environmental conditions of severe temperature extremes, mechanical shock, and high humidity. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metallized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

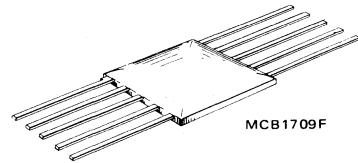
- High-Performance Open Loop Gain Characteristics
 $A_{VOL} = 45,000$ typical
- Low Temperature Drift $-\pm 3.0 \mu V/^{\circ}C$
- Large Output Voltage Swing $-\pm 14 V$ typical @ $\pm 15 V$ Supply
- Low Output Impedance $-Z_{out} = 150$ ohms typical

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON



BEAM-LEAD CHIP
MCBC1709

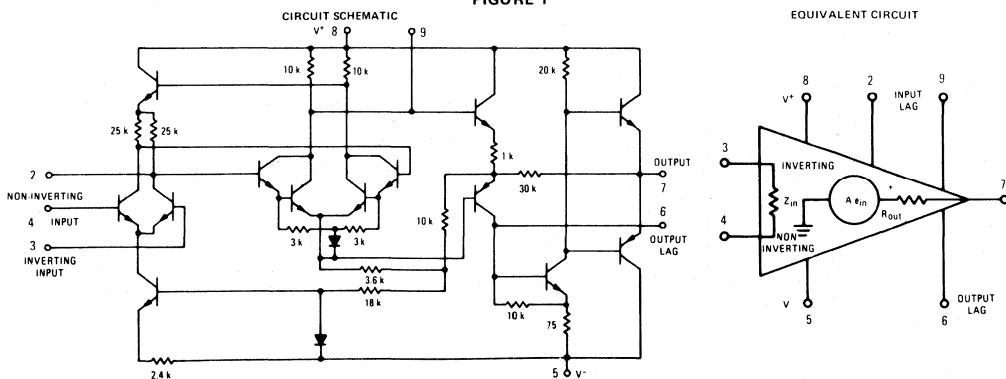


CASE 665
CERAMIC PACKAGE

MAXIMUM RATINGS ($T_A = +25^{\circ}C$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|----------------|-------------|-----------------------|
| Power Supply Voltage | V^+ V^- | +18 -18 | Vdc |
| Differential Input Signal | V_{in} | ± 5.0 | Volts |
| Common Mode Input Swing | CMV_{in} | $\pm V^+$ | Volts |
| Load Current | I_L | 10 | mA |
| Output Short Circuit Duration | t_S | 5.0 | s |
| Power Dissipation Derate above $T_A = +25^{\circ}C$ | P_D | 500 3.3 | mW mW/ $^{\circ}C$ |
| Operating Temperature Range | T_A | -55 to +125 | $^{\circ}C$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^{\circ}C$ |

FIGURE 1



Pin numbers shown are for Case 665, refer to Figure 10 for chip bonding diagram.

See Packaging Information Section for outline dimensions.

MCBC1709, MCB1709F (continued)

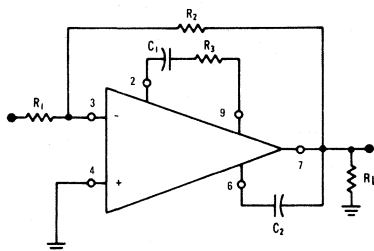
ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MCBC1709 and MCB1709F | | | Unit |
|--|--------------------------------------|-----------------------|----------------------|-------------------|--|
| | | Min | Typ | Max | |
| Open Loop Voltage Gain ($V_O = \pm 10$ V, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$) | A_{VOL} | 25,000 | 45,000 | 70,000 | — |
| Output Impedance ($f = 20$ Hz) | Z_{out} | — | 150 | — | Ω |
| Input Impedance ($f = 20$ Hz) | Z_{in} | 150 | 400 | — | $k\Omega$ |
| Output Voltage Swing ($R_L = 10$ $k\Omega$) ($R_L = 2.0$ $k\Omega$) | V_o | ± 12 ± 10 | ± 14 ± 13 | — — | V_{peak} |
| Input Common-Mode Voltage Swing | CMV_{in} | ± 8.0 | ± 10 | — | V_{peak} |
| Common-Mode Rejection Ratio ($f = 20$ Hz) | CM_{rej} | 70 | 90 | — | dB |
| Input Bias Current ($T_A = +25^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) | I_b | — — | 0.2 0.5 | 0.5 1.5 | μA |
| Input Offset Current ($T_A = +25^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) ($T_A = +125^\circ\text{C}$) | $ I_{io} $ | — — — | 0.05 — — | 0.2 0.5 0.2 | μA |
| Input Offset Voltage ($T_A = +25^\circ\text{C}$) ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$) | $ V_{io} $ | — — | 1.0 — | 5.0 6.0 | mV |
| Step Response { Gain = 100, 5.0% overshoot, $R_1 = 1.0$ $k\Omega$, $R_2 = 100$ $k\Omega$, $R_3 = 1.5$ $k\Omega$, $C_1 = 100$ μF , $C_2 =$ 3.0 μF } | t_f t_{pd} dV_{out}/dt ① | — — — | 0.8 0.38 12 | — — — | μs μs $\text{V}/\mu\text{s}$ |
| { Gain = 10, 10% overshoot, $R_1 = 1.0$ $k\Omega$, $R_2 = 10$ $k\Omega$, $R_3 = 1.5$ $k\Omega$, $C_1 = 500$ μF , $C_2 = 20$ μF } | t_f t_{pd} dV_{out}/dt ① | — — — | 0.6 0.34 1.7 | — — — | μs μs $\text{V}/\mu\text{s}$ |
| { Gain = 1, 5.0% overshoot, $R_1 = 10$ $k\Omega$, $R_2 = 10$ $k\Omega$, $R_3 =$ 1.5 $k\Omega$, $C_1 = 5000$ μF , $C_2 = 200$ μF } | t_f t_{pd} dV_{out}/dt ① | — — — | 2.2 1.3 0.25 | — — — | μs μs $\text{V}/\mu\text{s}$ |
| Average Temperature Coefficient of Input Offset Voltage ($R_S = 50$ Ω , $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$) ($R_S \leq 10$ $k\Omega$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$) | $ TCV_{io} $ | — — | 3.0 6.0 | — — | $\mu\text{V}/^\circ\text{C}$ |
| DC Power Dissipation (Power Supply = ± 15 V, $V_o = 0$) | P_D | — | 80 | 165 | mW |
| Positive Supply Sensitivity (V^- constant) | S^+ | — | 25 | 150 | $\mu\text{V}/\text{V}$ |
| Negative Supply Sensitivity (V^+ constant) | S^- | — | 25 | 150 | $\mu\text{V}/\text{V}$ |

① $dV_{out}/dt =$ Slew Rate

TYPICAL CHARACTERISTICS

FIGURE 2 – TEST CIRCUIT
 $V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$



| Fig. No. | Curve No. | Test Conditions | | | | |
|----------|-----------|--------------------|--------------------|--------------------|-------------------------|-------------------------|
| | | R_1 (Ω) | R_2 (Ω) | R_3 (Ω) | C_1 (μF) | C_2 (μF) |
| 3 | 1 | 10 k | 10 k | 1.5 k | 5.0 k | 200 |
| | 2 | 10 k | 100 k | 1.5 k | 500 | 20 |
| | 3 | 10 k | 1.0 M | 1.5 k | 100 | 3.0 |
| | 4 | 1.0 k | 1.0 M | 0 | 10 | 3.0 |
| 4 | 1 | 1.0 M | 1.0 M | 0 | 10 | 3.0 |
| | 2 | 10 k | 1.0 M | 1.5 k | 100 | 3.0 |
| | 3 | 10 k | 100 k | 1.5 k | 500 | 20 |
| | 4 | 10 k | 10 k | 1.5 k | 5.0 k | 200 |
| 5 | 1 | 0 | ∞ | 1.5 k | 5.0 k | 200 |
| | 2 | 0 | ∞ | 1.5 k | 500 | 20 |
| | 3 | 0 | ∞ | 1.5 k | 100 | 3.0 |
| | 4 | 0 | ∞ | 0 | 10 | 3.0 |

TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 3 – LARGE SIGNAL SWING
versus FREQUENCY

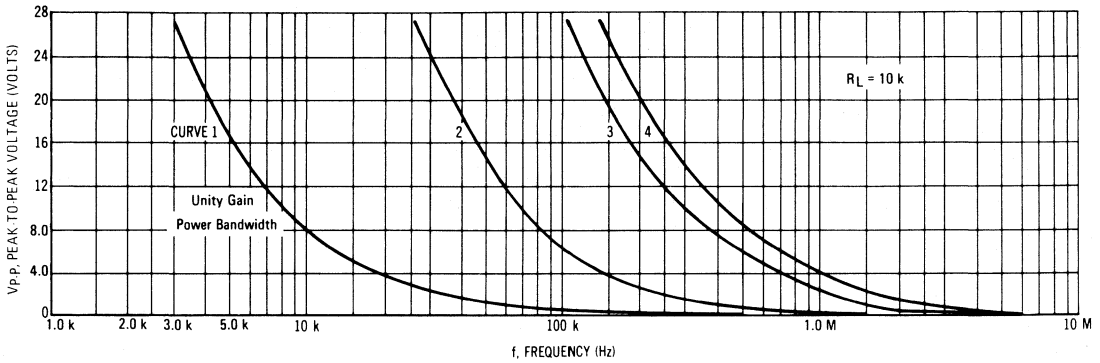


FIGURE 4 – VOLTAGE GAIN
versus FREQUENCY

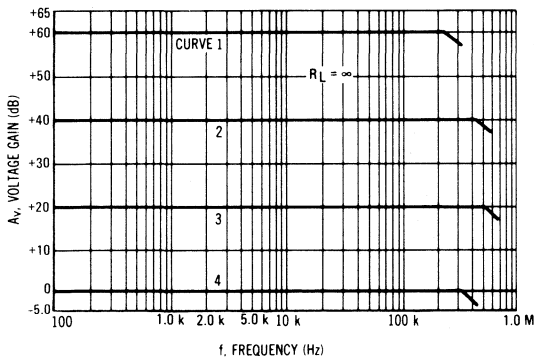


FIGURE 5 – OPEN LOOP
VOLTAGE GAIN versus FREQUENCY

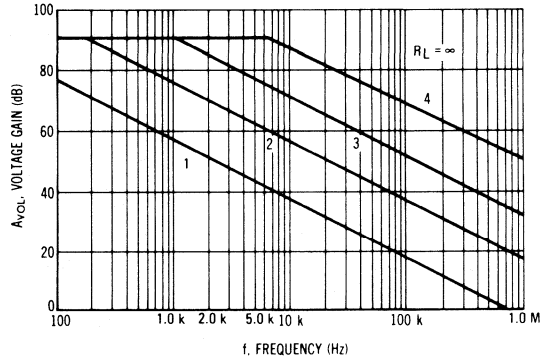


FIGURE 6 – VOLTAGE GAIN
versus POWER SUPPLY VOLTAGE

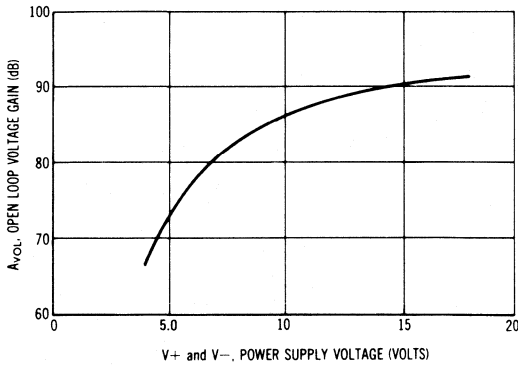
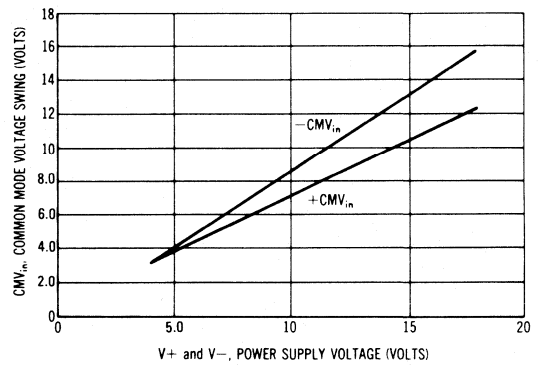


FIGURE 7 – COMMON SWING
versus POWER SUPPLY VOLTAGE



7

MCBC1709, MCB1709F (continued)

TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

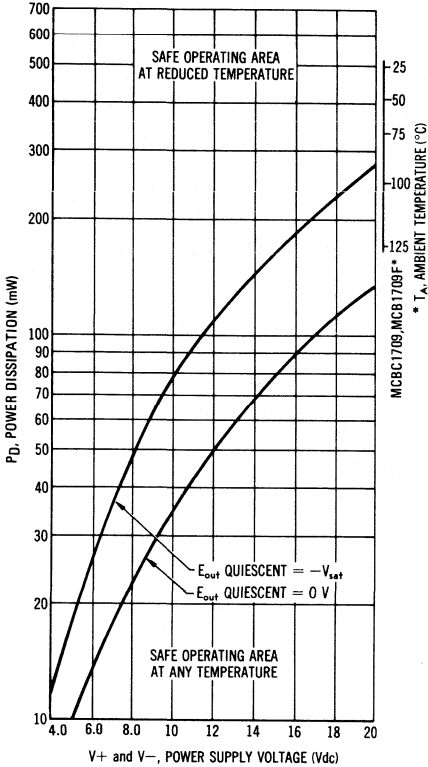


FIGURE 9 – INPUT NOISE VOLTAGE versus SOURCE RESISTANCE

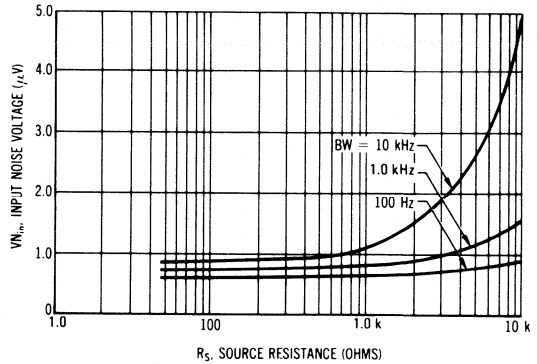
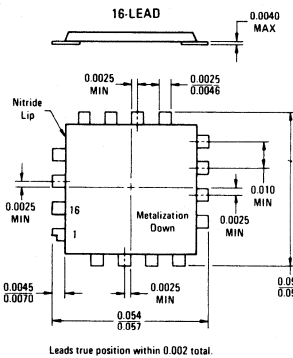
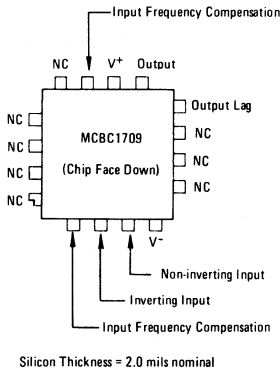


FIGURE 10 – BONDING DIAGRAM



PACKAGING AND HANDLING

The MCBC1709 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

DIFFERENTIAL COMPARATOR

MCBC1710 MCB1710F

Advance Information

MONOLITHIC DIFFERENTIAL VOLTAGE COMPARATOR

Beam-lead sealed-junction technology and fabrication make the MCBC1710 and MCB1710F devices excellent choices for military, aerospace, and commercial applications. These devices are designed for use in level detection, low-level sensing, and memory applications.

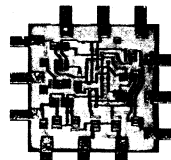
- Differential Input Characteristics –
Input Offset Voltage = 1.0 mV
Offset Voltage Drift = $3.0 \mu\text{V}/^\circ\text{C}$
- Fast Response Time – 40 ns
- Output Compatible With All Saturating Logic Forms –
 $V_O = +3.2 \text{ V}$ to -0.5 V Typical
- Low Output Impedance – 200 ohms

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol* | Value | Unit |
|---|-----------|-------------|----------------------|
| Power Supply Voltage | V_{CC} | +14 | Vdc |
| | V_{EE} | -7.0 | Vdc |
| Differential Input Signal | V_{ID} | ± 5.0 | Volts |
| Common Mode Input Swing | V_{ICR} | ± 7.0 | Volts |
| Peak Load Current | I_L | 10 | mA |
| Power Dissipation (package limitations) | P_D | 500 | mW |
| Flat Package | | 3.3 | mW/ $^\circ\text{C}$ |
| Derate above $T_A = +25^\circ\text{C}$ | | | |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

*Symbols conform to JEDEC Engineering Bulletin No. 1 where applicable.

DIFFERENTIAL COMPARATOR INTEGRATED CIRCUIT MONOLITHIC SILICON



BEAM-LEAD CHIP

MCBC1710

F SUFFIX
CERAMIC PACKAGE
CASE 606
(TO-91)

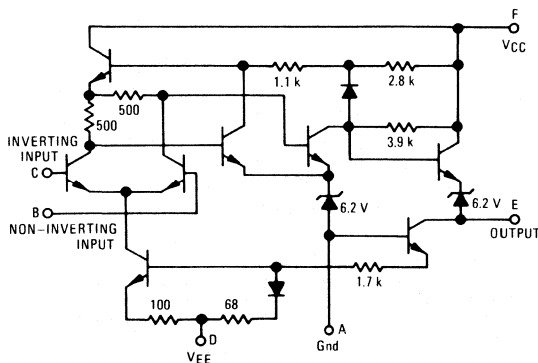


MCB1710F

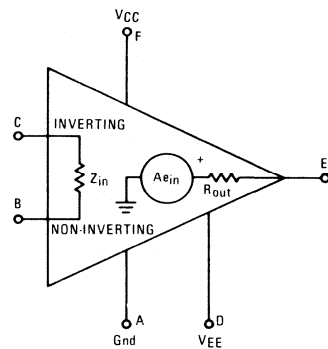
SCHEMATIC PIN CONNECTIONS

| Chip | A | B | C | D | E | F |
|-------------|---|---|---|---|---|---|
| "F" Package | 1 | 2 | 3 | 5 | 6 | 8 |

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



This is advance information on a new introduction and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

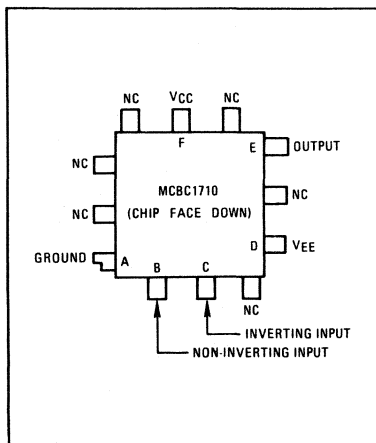
MCBC1710, MCB1710F (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = +12$ Vdc, $V_{EE} = -6.0$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted)

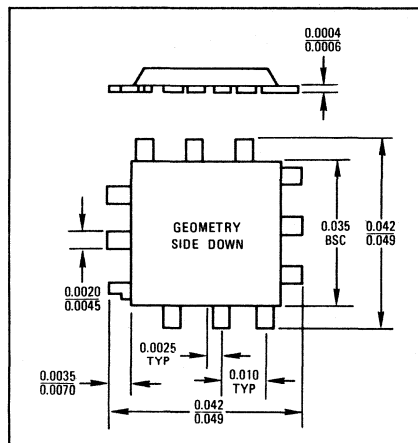
| Characteristic | Symbol | MCBC1710/MCB1710F | | | Unit |
|--|----------------------|-------------------|------------|------------|-----------------|
| | | Min | Typ | Max | |
| Input Offset Voltage ($V_O = 1.4$ Vdc) | V_{IO} | — | 1.0 | 2.0 | mVdc |
| Input Bias Current ($V_O = 1.4$ Vdc) | I_{IB} | — | 12 | 20 | μAdc |
| Output Resistance | r_o | — | 200 | — | Ohms |
| Positive Output Voltage ($V_{in} \geq 5.0$ mV, $0 \leq I_O \leq 5.0$ mA) | V_{OH} | 2.5 | 3.2 | 4.0 | Vdc |
| Negative Output Voltage ($V_{in} \geq -5.0$ mV) | V_{OL} | -1.0 | -0.5 | 0 | Vdc |
| Output Sink Current ($V_{in} \geq -5.0$ mV, $V_{out} \geq 0$) | I_s | 2.0 | 2.5 | — | mAdc |
| Common Mode Rejection Ratio ($V_O = -7.0$ Vdc, $R_S \leq 200 \Omega$) | CMRR | — | 100 | — | dB |
| Propagation Delay Time For Positive and Negative Going Input Pulse | t_{pd} | — | 40 | — | ns |
| Power Supply Current ($V_O \leq 0$ Vdc) | I_{D+} I_{D-} | — | 6.4 5.5 | 9.0 7.0 | mAdc |
| DC Quiescent Power Dissipation | P_D | — | 115 | 150 | mW |

*Symbols conform to JEDEC Engineering Bulletin No. 1 where applicable.
See current MC1710/1710C data sheet for additional information.

BONDING DIAGRAM



12 - BEAM CHIP



PACKAGING AND HANDLING

The MCBC1710 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of

polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

MCBC1723 MCB1723F

Advance Information

MONOLITHIC VOLTAGE REGULATOR

The MCBC1723/MCB1723F is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metalized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

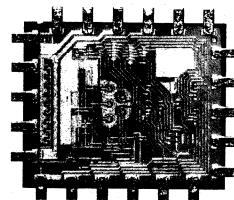
- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line Regulation
- Adjustable Short-Circuit Protection

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol * | Value | Unit |
|---|---------------------------------|-------------|-------------------|
| Pulse Voltage from V _{CC} to V _{EE} (50 ms) | V _{in(p)} | 50 | V _{peak} |
| Continuous Voltage from V _{CC} to V _{EE} | V _{in} | 40 | Vdc |
| Input-Output Voltage Differential | V _{in} -V _O | 40 | Vdc |
| Maximum Output Current | I _L | 150 | mAdc |
| Current from V _{ref} | I _{ref} | 15 | mAdc |
| Operating Temperature Range | T _A | -55 to +125 | °C |
| Junction Temperature Range | T _J | -65 to +150 | °C |

*Symbols conform to JEDEC Engineering Bulletin No. 1 where applicable.

VOLTAGE REGULATOR INTEGRATED CIRCUIT



BEAM-LEAD CHIP

MCBC1723

F SUFFIX CERAMIC PACKAGE CASE 607 (TO-86)



SCHEMATIC PIN CONNECTIONS

| Chip | A | B | C | D | E | F | G | H | J | K | L |
|-------------|---|---|---|---|---|---|---|----|----|----|----|
| "F" Package | 2 | 3 | 4 | 5 | 6 | 7 | 9 | 10 | 11 | 12 | 13 |

FIGURE 1 - TYPICAL CIRCUIT CONNECTION

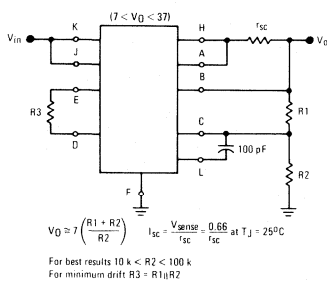
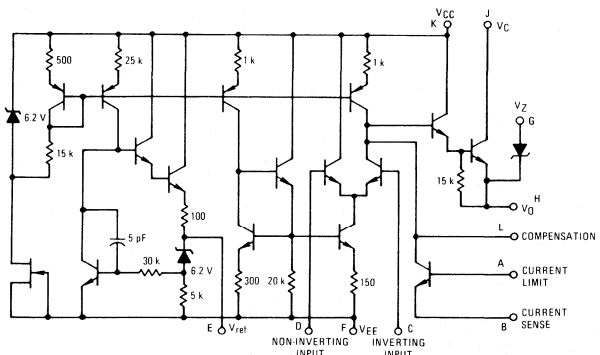


FIGURE 2 - CIRCUIT SCHEMATIC



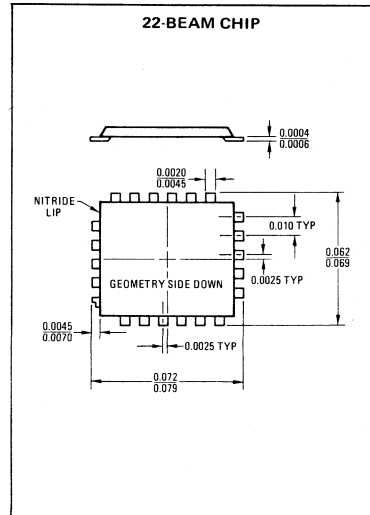
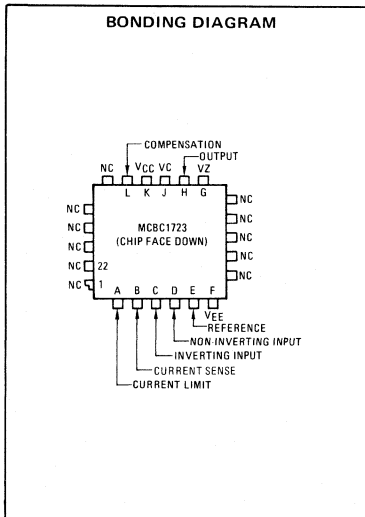
This is advance information on a new introduction and specifications are subject to change without notice.
See Packaging Information Section for outline dimensions.

MCBC1723, MCB1723F (continued)

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: $T_A = +25^\circ\text{C}$, $V_{in} = 12\text{ Vdc}$, $V_O = 5\text{ Vdc}$, $I_L = 1\text{ mA}$, $r_{sc} = 0$, $C_1 = 100\text{ pF}$, $C_{ref} = 0$ and divider impedance as seen by the error amplifier $\leq 10\text{ k}\Omega$ connected as shown in Figure 1)

| Characteristic | Symbol* | MCBC1723/MCB1723F | | | Unit |
|--|----------------|-------------------|------|------|--------------------|
| | | Min | Typ | Max | |
| Input Voltage Range | V_{in} | 9.5 | — | 40 | Vdc |
| Output Voltage Range | V_O | 2.0 | — | 37 | Vdc |
| Input-Output Voltage Differential | $V_{in} - V_O$ | 3.0 | — | 38 | Vdc |
| Reference Voltage | V_{ref} | 6.95 | 7.15 | 7.35 | Vdc |
| Standby Current Drain ($I_L = 0$, $V_{in} = 30\text{ V}$) | I_{IB} | — | 2.3 | 3.5 | mAdc |
| Output Noise Voltage ($f = 100\text{ Hz}$ to 10 kHz) $C_{ref} = 0$ $C_{ref} = 5.0\text{ }\mu\text{F}$ | V_n | — | 20 | — | $\mu\text{V(rms)}$ |
| Line Regulation ($12\text{ V} < V_{in} < 15\text{ V}$) ($12\text{ V} < V_{in} < 40\text{ V}$) | Reg_{in} | — | 0.01 | 0.1 | % V_O |
| Load Regulation ($1.0\text{ mA} < I_L < 50\text{ mA}$) | Reg_{load} | — | 0.03 | 0.15 | % V_O |
| Ripple Rejection ($f = 50\text{ Hz}$ to 10 kHz) $C_{ref} = 0$ $C_{ref} = 5.0\text{ }\mu\text{F}$ | Rej_R | — | 74 | — | dB |
| Short Circuit Current Limit ($r_{sc} = 10\text{ }\Omega$, $V_O = 0$) | I_{sc} | — | 65 | — | mAdc |

*Symbols conform to JEDEC Engineering Bulletin No. 1 where applicable.



PACKAGING AND HANDLING

The MCBC1723 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of

polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

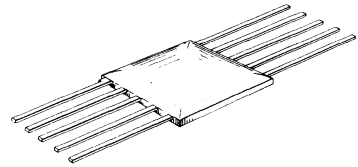
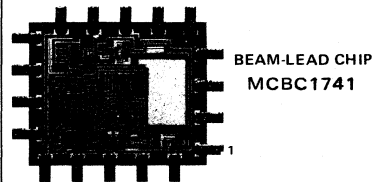
MCBC1741
MCB1741F

MONOLITHIC OPERATIONAL AMPLIFIER

Beam-lead sealed-junction technology and fabrication make the MCBC1741 and MCB1741F devices excellent choices for military, aerospace, and commercial applications; usages requiring a high degree of reliability under environmental conditions of severe temperature extremes, mechanical shock, and high humidity. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metallized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

**OPERATIONAL AMPLIFIER
INTEGRATED CIRCUIT
MONOLITHIC SILICON**



MCB1741F
CASE 665
CERAMIC PACKAGE

SCHEMATIC PIN CONNECTIONS

| | | | | | | | |
|-------------|---|---|---|---|---|---|---|
| Chip | A | B | C | D | E | F | G |
| "F" Package | 2 | 3 | 4 | 5 | 6 | 7 | 8 |

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|------------|-------------|----------------------|
| Power Supply Voltage | V^+ | +22 | Vdc |
| | V^- | -22 | |
| Differential Input Signal | V_{in} | ± 30 | Volts |
| Common Mode Input Swing (Note 1) | CMV_{in} | ± 15 | Volts |
| Output Short Circuit Duration (Note 2) | t_S | Continuous | |
| Power Dissipation | P_D | 500 | mW |
| | | 3.3 | mW/ $^\circ\text{C}$ |
| Derate above $T_A = +25^\circ\text{C}$ (Flat Package) | | | |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

FIGURE 1 – CIRCUIT SCHEMATIC

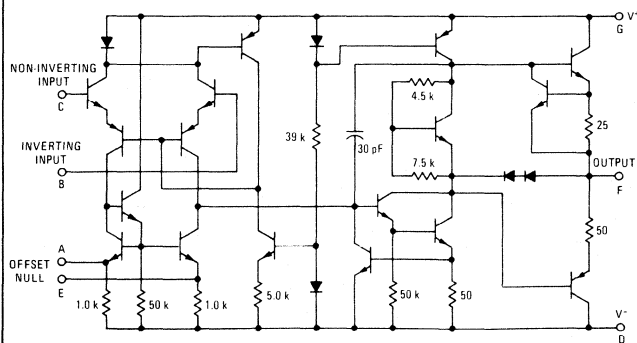
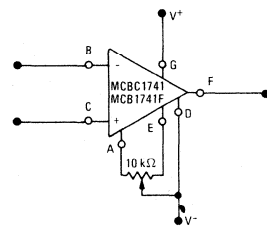


FIGURE 2 – OFFSET ADJUST CIRCUIT



See Packaging Information Section for outline dimensions.

MCBC1741, MCB1741F (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MCBC1741, MCB1741F | | | Unit |
|--|--------------------------------------|----------------------------------|---------------------------|-------------|--|
| | | Min | Typ | Max | |
| Open Loop Voltage Gain ($R_L = 2.0$ k Ω) ($V_O = \pm 10$ V, $T_A = +25^\circ\text{C}$) ($V_O = \pm 10$ V, $T_A = -55$ to $+125^\circ\text{C}$) | A_{VOL} | 50,000 25,000 | 200,000 — | — — | — |
| Output Impedance ($f = 20$ Hz) | Z_O | — | 75 | — | Ω |
| Input Impedance ($f = 20$ Hz) | Z_{in} | 0.3 | 1.0 | — | Meg Ω |
| Output Voltage Swing ($R_L = 10$ k Ω) ($R_L = 2.0$ k Ω) ($R_L = 2.0$ k Ω , $T_A = -55$ to $+125^\circ\text{C}$) | V_O | ± 12 ± 10 ± 10 | ± 14 ± 13 — | — — — | V_{peak} |
| Input Common-Mode Voltage Swing | CMV_{in} | ± 12 | ± 13 | — | V_{peak} |
| Common-Mode Rejection Ratio ($f = 20$ Hz) | CM_{rej} | 70 | 90 | — | dB |
| Input Bias Current ($T_A = +25^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) | I_b | — — | 0.2 0.5 | 0.5 1.5 | μA |
| Input Offset Current ($T_A = +25^\circ\text{C}$) ($T_A = -55$ to $+125^\circ\text{C}$) | $ I_{io} $ | — — | 0.03 — | 0.2 0.5 | μA |
| Input Offset Voltage ($T_A = +25^\circ\text{C}$) ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$) | $ V_{io} $ | — — | 1.0 — | 5.0 6.0 | mV |
| Step Response Gain = 100, $R_1 = 1.0$ k Ω , $R_2 = 100$ k Ω , $R_3 = 1.0$ k Ω | t_f t_{pd} dV_{out}/dt ① | — — — | 29 8.5 1.0 | — — — | μs μs V/ μs |
| Gain = 10, $R_1 = 1.0$ k Ω , $R_2 = 10$ k Ω , $R_3 = 1.0$ k Ω | t_f t_{pd} dV_{out}/dt ① | — — — | 3.0 1.0 1.0 | — — — | μs μs V/ μs |
| Gain = 1, $R_1 = 10$ k Ω , $R_2 = 10$ k Ω , $R_3 = 5.0$ k Ω | t_f t_{pd} dV_{out}/dt ① | — — — | 0.6 0.38 0.8 | — — — | μs μs V/ μs |
| Average Temperature Coefficient of Input Offset Voltage ($R_S = 50$ Ω , $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$) ($R_S = 10$ k Ω , $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$) | $ TC_{V_{io}} $ | — — | 3.0 6.0 | — — | $\mu\text{V}/^\circ\text{C}$ |
| Average Temperature Coefficient of Input Offset Current ($T_A = -55$ to $+125^\circ\text{C}$) | $ TC_{V_{io}} $ | — | 50 | — | $\text{pA}/^\circ\text{C}$ |
| DC Power Dissipation (Power Supply = ± 15 V, $V_O = 0$) | P_D | — | 50 | 85 | mW |
| Positive Supply Sensitivity (V^- constant) | S^+ | — | 30 | 150 | $\mu\text{V}/\text{V}$ |
| Negative Supply Sensitivity (V^+ constant) | S^- | — | 30 | 150 | $\mu\text{V}/\text{V}$ |
| Power Bandwidth ($A_V = 1$, $R_L = 2.0$ k Ω , THD = 5%, $V_O = 20$ V $_{p-p}$) | PBW | — | 10 | — | kHz |

① dV_{out}/dt = Slew Rate

MCBC1741, MCB1741F (continued)

TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)

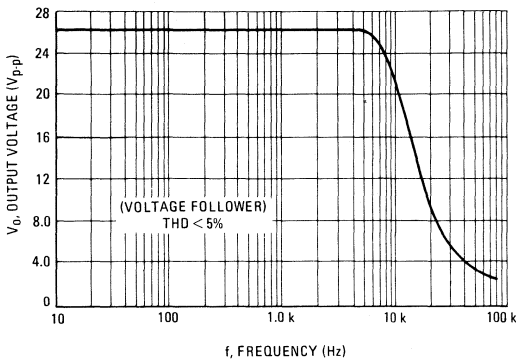


FIGURE 4 – OPEN LOOP FREQUENCY RESPONSE

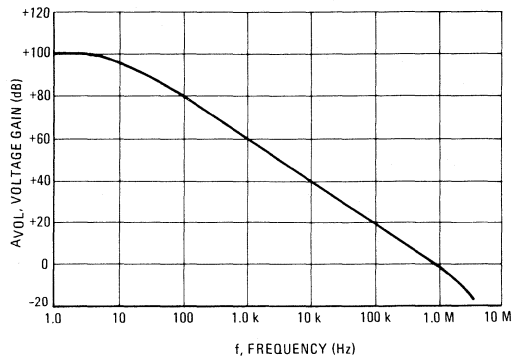


FIGURE 5 – OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

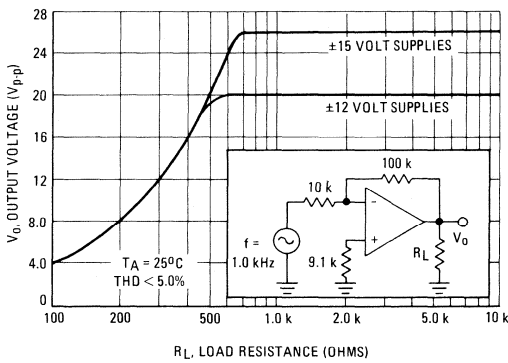


FIGURE 6 – COMMON-MODE REJECTION
RATIO versus FREQUENCY

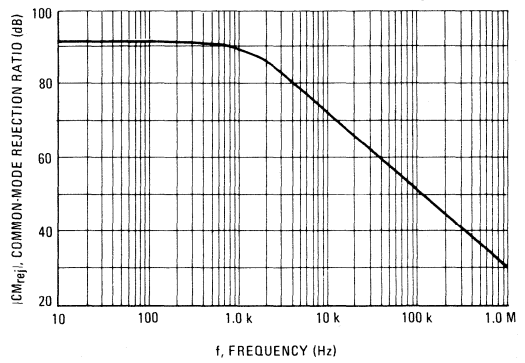


FIGURE 7 – INPUT OFFSET CURRENT
versus TEMPERATURE

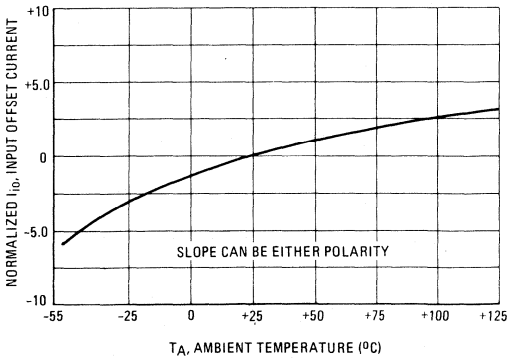
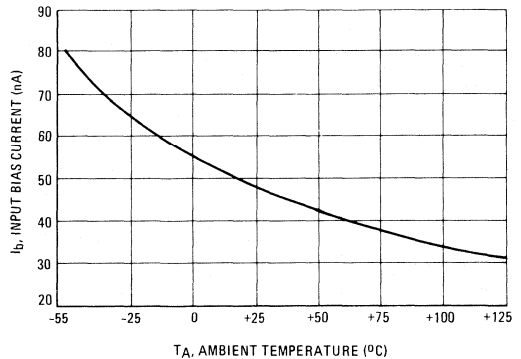


FIGURE 8 – INPUT BIAS CURRENT
versus TEMPERATURE



7

MCBC1741, MCB1741F (continued)

TYPICAL CHARACTERISTICS (continued)

($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 9 — POWER DISSIPATION versus POWER SUPPLY VOLTAGE

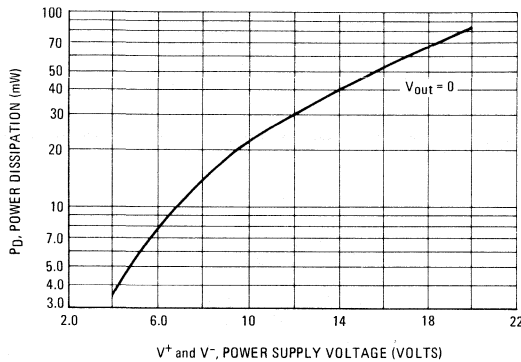


FIGURE 10 — OUTPUT NOISE versus SOURCE RESISTANCE

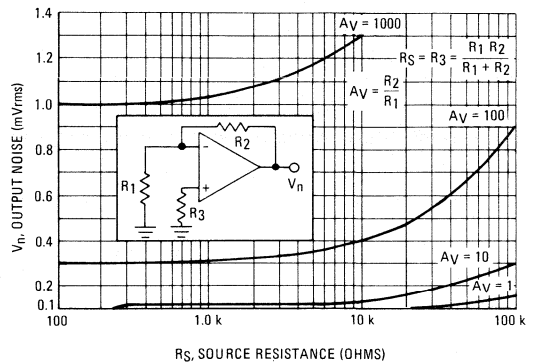
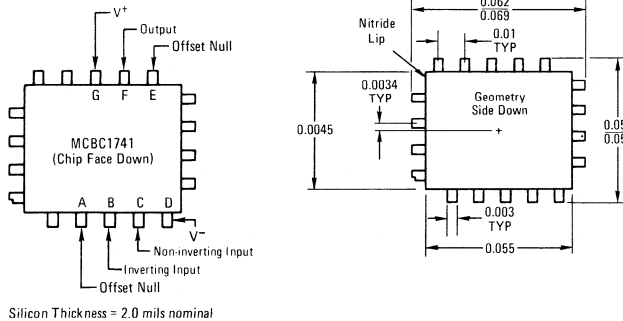


FIGURE 11 — BONDING DIAGRAM



PACKAGING AND HANDLING

The MCBC1741 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

MCBC1748 MCB1748F

Advance Information

HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

Beam-lead sealed-junction technology and fabrication make the MCBC1748 and MCB1748F devices excellent choices for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. Beam-lead products employ a silicon-nitride dielectric that hermetically seals the chip, eliminating the need for a hermetic package. The beam leads are gold cantilevered structures extending from the chip. These beams bond readily to a gold metallized substrate providing one of the most reliable interconnection systems known for semiconductor devices.

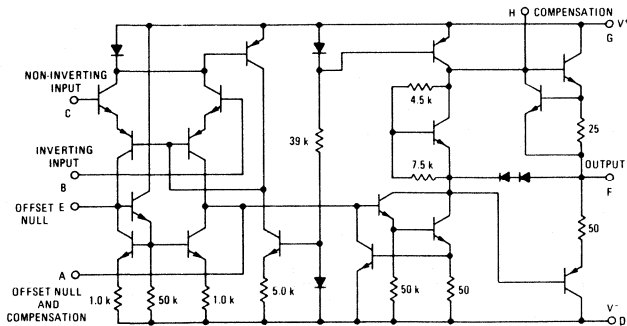
- Noncompensated MCBC1741
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

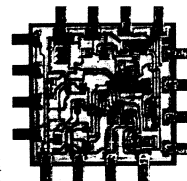
| Rating | Symbol | Value | Unit |
|---|----------------|-------------|----------------------|
| Power Supply Voltage | V^+ V^- | +18 -18 | Vdc |
| Differential Input Signal | V_{in} | ± 5.0 | Volts |
| Common Mode Input Swing ① | CMV_{in} | $\pm V^+$ | Volts |
| Load Current | I_L | 10 | mA |
| Output Short Circuit Duration | t_S | 5.0 | s |
| Power Dissipation | P_D | 500 | mW |
| Derate above $T_A = +25^\circ\text{C}$ (Flat Package) | | 3.3 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

① For supply voltages less than ± 15 V, the Maximum Input Voltage is equal to the Supply Voltage.

FIGURE 1 - CIRCUIT SCHEMATIC



OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT



MCBC1748

BEAM-LEAD CHIP

F SUFFIX
CERAMIC PACKAGE
CASE 606
(TO-91)

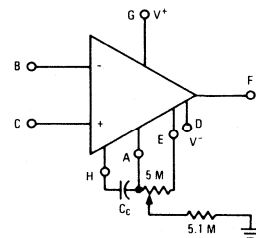


MCB1748F

SCHEMATIC PIN CONNECTIONS

| Chip | A | B | C | D | E | F | G | H |
|-------------|---|---|---|---|---|---|---|---|
| "F" Package | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

FIGURE 2 - OFFSET ADJUST AND FREQUENCY COMPENSATION



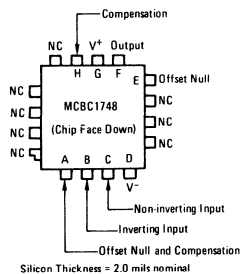
This is advance information on a new introduction and specifications are subject to change without notice. See Packaging Information Section for outline dimensions.

MCBC1748, MCB1748F (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---------------|----------------------|----------------------|------|------------------------|
| Open-Loop Voltage Gain, ($V_O = +10$ V, $R_L = 2.0$ k ohms) | A_{VOL} | 50,000 | 200,000 | — | — |
| Output Impedance ($f = 20$ Hz) | Z_O | — | 75 | — | ohms |
| Common Mode Input Impedance ($f = 20$ Hz) | Z_{in} | — | 200 | — | Megohms |
| Output Voltage Swing ($R_L = 10$ k ohms) $R_L = 2$ k ohms ($T_A = -55$ to $+125^\circ\text{C}$) | V_O | ± 12 ± 10 | ± 14 ± 13 | — | Vpk |
| Common-Mode Input Voltage Swing | CMV_{in} | — | ± 13 | — | Vpk |
| Common-Mode Rejection Ratio ($f = 100$ Hz) | CM_{rej} | — | 90 | — | dB |
| Input Bias Current | I_b | — | 0.08 | 0.5 | μA_{dc} |
| Input Offset Current | I_{io} | — | 0.02 | 0.2 | μA_{dc} |
| Input Offset Voltage ($R_S \leq 10$ k Ω) | V_{io} | — | 1.0 | 5.0 | mVdc |
| Step Response ($V_{in} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ k Ω , $C_L = 100$ pF) | | | | | |
| Rise Time | t_r | — | 0.3 | — | μs |
| Overshoot Percentage | | — | 5.0 | — | % |
| Slew Rate | dV_{out}/dt | — | 0.8 | — | V/ μs |
| Short-Circuit Output Current | I_{SC} | — | 25 | — | mAdc |
| Differential Input Impedance (Open-Loop, $f = 20$ Hz) | | | | | |
| Parallel Input Resistance | R_p | — | 2.0 | — | Megohms |
| Parallel Input Capacitance | C_p | — | 1.4 | — | pF |
| Power Supply Sensitivity | | | | | |
| $V^- = \text{constant}$, $R_S \leq 10$ k ohms | S+ | — | 30 | 150 | $\mu\text{V}/\text{V}$ |
| $V^+ = \text{constant}$, $R_S \leq 10$ k ohms | S- | — | 30 | 150 | |
| Power Supply Current | | | | | |
| I_{D^+} | | — | 1.67 | 2.83 | mAdc |
| I_{D^-} | | — | 1.67 | 2.83 | mAdc |
| DC Quiescent Power Dissipation ($V_O = 0$) | P_D | — | 50 | 85 | mW |

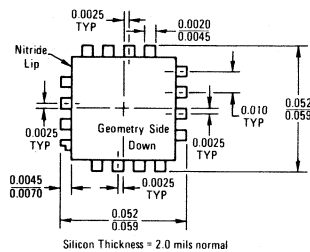
BONDING DIAGRAM



PACKAGING AND HANDLING

The MCBC1748 beam-lead sealed-junction linear integrated circuit is available in chip form (non-encapsulated) as shown in the outline dimensional drawing. The shipping carrier for chips is a 2" square glass plate on which the chips are placed. A thin layer of

16-BEAM CHIP



polymer film covers the plate and retains the chips in place. The chips do not adhere to the film when it is lifted to remove them from the carrier. Care must be exercised when removing the chips from the carrier to ensure that the beams are not bent. A vacuum pickup is useful for this purpose.

MCC1536
MCC1436

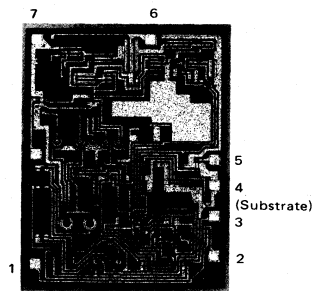
**HIGH VOLTAGE, INTERNALLY COMPENSATED
MONOLITHIC OPERATIONAL AMPLIFIER**

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1536 and MCC1436 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Maximum Supply Voltage – ± 40 Vdc
- Output Voltage Swing –
 $\pm 30 V_{pk(min)}$ ($V^+ = +36 V, V^- = -36 V$)
 $\pm 22 V_{pk(min)}$ ($V^+ = +28 V, V^- = -28 V$)
- Input Bias Current – 20 nA max
- Input Offset Current – 3.0 nA max
- Input Offset Voltage Null Capability
- Fast Slew Rate – 2.0 V/ μ s typ
- Input Over-Voltage Protection
- Internally Compensated
- $AV_{OL} - 500,000$ typ
- Characteristics Independent of Power Supply Voltages –
 $(\pm 5.0$ Vdc to ± 36 Vdc)

**OPERATIONAL AMPLIFIER
MONOLITHIC SILICON
INTEGRATED CIRCUIT
EPITAXIAL PASSIVATED**



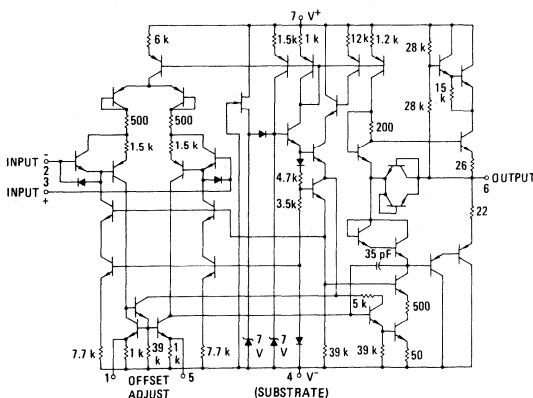
MCC1536/MCC1436

MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise noted)

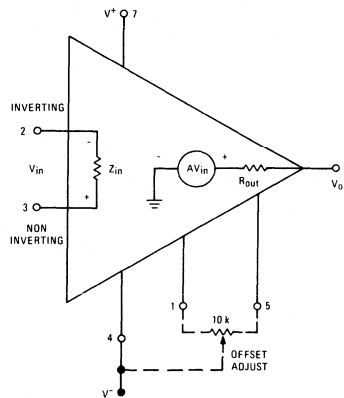
| Rating | Symbol | MCC1536 | MCC1436 | Unit |
|---|----------------|-------------------------|------------|------------|
| Power Supply Voltage | V^+ V^- | +40 -40 | +34 -34 | Vdc |
| Differential Input Signal (1) | V_{in} | $\pm(V^+ + V^- - 3)$ | | Volts |
| Common-Mode Input Swing | CMV_{in} | $+V^+, -(V^- - 3)$ | | Volts |
| Output Short Circuit Duration ($V^+ = V^- = 28$ Vdc, $V_O = 0$) | T_{SC} | 5.0 | | s |
| Operating Temperature Range | T_A | -55 to +125 0 to +75 | | $^\circ C$ |
| Junction Temperature Range | T_{stg} | -65 to +150 | | $^\circ C$ |

(1) The absolute voltage applied to either input terminal must not exceed $+V^+, -(|V^-| - 3)$.

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



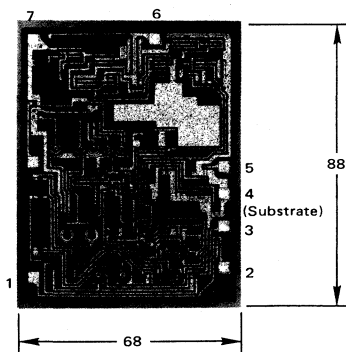
MCC1536, MCC1436 (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +28\text{ Vdc}$, $V^- = -28\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristics | Symbol | MCC1536 | | | MCC1436 | | | Unit |
|---|------------------------|----------------------|----------------------|------------|----------|-------------------|------------|-----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | I_b | — | 8.0 | 20 | — | 15 | 40 | nAdc |
| Input Offset Current | $ I_{io} $ | — | 1.0 | 3.0 | — | 5.0 | 10 | nAdc |
| Input Offset Voltage | $ V_{io} $ | — | 2.0 | 5.0 | — | 5.0 | 10 | mVdc |
| Differential Input Impedance (Open-Loop, $f \leq 5.0\text{ Hz}$) | R_p | — | 10 | — | — | 10 | — | Meg ohms |
| Parallel Input Resistance | C_p | — | 2.0 | — | — | 2.0 | — | pF |
| Parallel Input Capacitance | | | | | | | | |
| Common-Mode Input Impedance ($f \leq 5.0\text{ Hz}$) | $Z_{(in)}$ | — | 250 | — | — | 250 | — | Meg ohms |
| Common-Mode Input Voltage Swing | CMV_{in} | — | ± 25 | — | — | ± 25 | — | V_{pk} |
| Common-Mode Rejection Ratio (dc) | CM_{rej} | — | 110 | — | — | 110 | — | dB |
| Large Signal dc Open Loop Voltage Gain ($V_o = \pm 10\text{ V}$, $R_L = 100\text{ k ohms}$) ($V_o = \pm 10\text{ V}$, $R_L = 10\text{ k ohms}$) | A_{VOL} | — | 100,000 500,000 | — | — | 70,000 500,000 | — | V/V |
| Power Bandwidth (Voltage Follower) ($A_V = 1$, $R_L = 5.0\text{ k ohms}$, $THD \leq 5\%$, $V_o = 40\text{ Vp-p}$) | P_{BW} | — | 23 | — | — | 23 | — | kHz |
| Unity Gain Crossover Frequency (open-loop) | | — | 1.0 | — | — | 1.0 | — | MHz |
| Phase Margin (open-loop, unity gain) | | — | 50 | — | — | 50 | — | degrees |
| Gain Margin | | — | 18 | — | — | 18 | — | dB |
| Slew Rate (Unity Gain) | dV_{out}/dt | — | 2.0 | — | — | 2.0 | — | $V/\mu s$ |
| Output Impedance ($f \leq 5.0\text{ Hz}$) | Z_{out} | — | 1.0 | — | — | 1.0 | — | k ohms |
| Short-Circuit Output Current | I_{SC} | — | ± 17 | — | — | ± 17 | — | mAdc |
| Output Voltage Swing ($R_L = 5.0\text{ k ohms}$) $V^+ = +28\text{ Vdc}$, $V^- = -28\text{ Vdc}$ $V^+ = +36\text{ Vdc}$, $V^- = -36\text{ Vdc}$ | V_o | ± 22 ± 30 | ± 23 ± 32 | — | ± 20 | ± 22 | — | V_{pk} |
| Power Supply Sensitivity (dc) $V^- = \text{constant}$, $R_s \leq 10\text{ k ohms}$ $V^+ = \text{constant}$, $R_s \leq 10\text{ k ohms}$ | S^+ S^- | — — | 15 15 | 100 100 | — — | 35 35 | 200 200 | $\mu V/V$ |
| Power Supply Current | I_{D^+} I_{D^-} | — — | 2.2 2.2 | 4.0 4.0 | — — | 2.6 2.6 | 5.0 5.0 | mAdc |
| DC Quiescent Power Dissipation ($V_o = 0$) | P_D | — | 124 | 224 | — | 146 | 280 | mW |

See current MC1536/1436 data sheet for additional information.

MCC1536/MCC1436 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).

Die Dimensions

Thickness = 8.0

Bonding Pads = 4.0×4.0

PACKAGING AND HANDLING

The MCC1536/MCC1436 operational amplifier is now available in die (chip) form. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1539
MCC1439

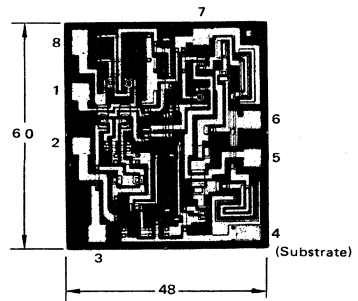
MONOLITHIC OPERATIONAL AMPLIFIER CHIP

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information see Motorola Application Note AN-439.

The MCC1539 and MCC1439 employ phosphosilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Low Input Offset Voltage – 3.0 mV max
- Low Input Offset Current – 60 nA max
- Large Power-Bandwidth – 20 V_{p-p} Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- Slew Rate – 34 V/ μ s typ

**OPERATIONAL AMPLIFIER CHIP
INTEGRATED CIRCUIT
MONOLITHIC SILICON**



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|-------------------------------|-------------------|------------------------------------|-----------------|
| Power Supply Voltage | V ⁺ | +18 | V _{dc} |
| | V ⁻ | -18 | V _{dc} |
| Differential Input Signal | V _{in} | $\pm[V^+ + V^-]$ | V _{dc} |
| Common Mode Input Swing | CMV _{in} | +V ⁺ , - V ⁻ | V _{dc} |
| Load Current | I _L | 15 | mA |
| Output Short Circuit Duration | t _S | Continuous | |
| Operating Temperature Range | T _A | MCC1539 | -55 to +125 |
| | | MCC1439 | 0 to +75 |
| Junction Temperature Range | T _J | -65 to +150 | °C |

FIGURE 1 – CIRCUIT SCHEMATIC

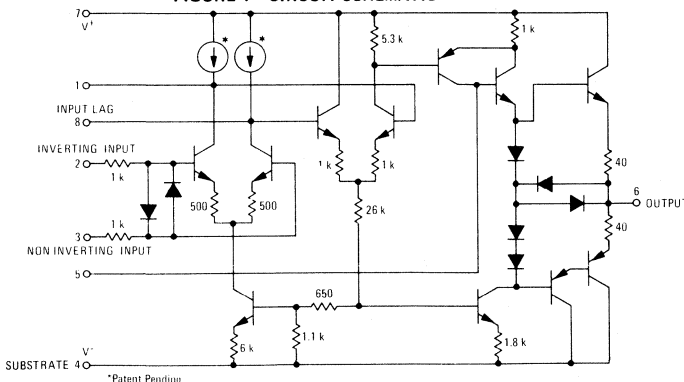
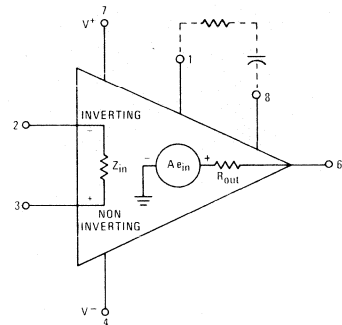


FIGURE 2 – EQUIVALENT CIRCUIT



MCC1539, MCC1439 (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MCC1539 | | | MCC1439 | | | Unit |
|--|------------------------|---------|------------|------------|----------|------------|------------|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | I_b | — | 0.20 | 0.50 | — | 0.20 | 1.0 | μA |
| Input Offset Current | $ I_{io} $ | — | 20 | 60 | — | 20 | 100 | nA |
| Input Offset Voltage | $ V_{io} $ | — | 1.0 | 3.0 | — | 2.0 | 7.5 | mV |
| Average Temperature Coefficient of Input Offset Voltage ($R_S = 50 \Omega$) | $ TC_{V_{io}} $ | — | 3.0 | — | — | 3.0 | — | $\mu\text{V}/^\circ\text{C}$ |
| Input Impedance | Z_{in} | — | 300 | — | — | 300 | — | $\text{k}\Omega$ |
| Input Common-Mode Voltage Swing | CMV_{in} | — | ± 12 | — | — | ± 12 | — | V _{pk} |
| Common Mode Rejection Ratio ($f = 1.0$ kHz) | CM_{rej} | — | 110 | — | — | 110 | — | dB |
| Open Loop Voltage Gain ($V_O = \pm 10$ V, $R_L = 10 \text{ k}\Omega$) | A_{VOL} | 50,000 | 120,000 | — | 15,000 | 100,000 | — | — |
| Power Bandwidth ($A_V = 1$, $THD \leq 5\%$, ($V_O = 20$ V _{p-p} , $R_L = 1.0 \text{ k}\Omega$) | PBW | — | 50 | — | — | 50 | — | kHz |
| Step Response | | | | | | | | |
| Gain = 1000, no overshoot, | t_f | — | 130 | — | — | 130 | — | ns |
| | t_{pd} | — | 190 | — | — | 190 | — | ns |
| | dV_{out}/dt | — | 6.0 | — | — | 6.0 | — | V/ μs |
| Gain = 1000, 15% overshoot, | t_f | — | 80 | — | — | 80 | — | ns |
| | t_{pd} | — | 100 | — | — | 100 | — | ns |
| | dV_{out}/dt | — | 14 | — | — | 14 | — | V/ μs |
| Gain = 100, no overshoot, | t_f | — | 60 | — | — | 60 | — | ns |
| | t_{pd} | — | 100 | — | — | 100 | — | ns |
| | dV_{out}/dt | — | 34 | — | — | 34 | — | V/ μs |
| Gain = 10, 15% overshoot, | t_f | — | 120 | — | — | 120 | — | ns |
| | t_{pd} | — | 80 | — | — | 80 | — | ns |
| | dV_{out}/dt | — | 6.25 | — | — | 6.25 | — | V/ μs |
| Gain = 1, 15% overshoot, | t_f | — | 160 | — | — | 160 | — | ns |
| | t_{pd} | — | 80 | — | — | 80 | — | ns |
| | dV_{out}/dt | — | 4.2 | — | — | 4.2 | — | V/ μs |
| Output Impedance ($f = 20$ Hz) | Z_{out} | — | 4.0 | — | — | 4.0 | — | $\text{k}\Omega$ |
| Output Voltage Swing ($R_L = 2.0 \text{ k}\Omega$, $f = 1.0$ kHz) ($R_L = 1.0 \text{ k}\Omega$, $f = 1.0$ kHz) | V_{out} | — | — | — | ± 10 | ± 13 | — | V _{pk} |
| Positive Supply Sensitivity (V^- constant) | S^+ | — | 50 | 150 | — | 50 | 200 | $\mu\text{V}/\text{V}$ |
| Negative Supply Sensitivity (V^+ constant) | S^- | — | 50 | 150 | — | 50 | 200 | $\mu\text{V}/\text{V}$ |
| Power Supply Current ($V_O = 0$) | I_{D^+} I_{D^-} | — | 3.0 3.0 | 5.0 5.0 | — | 3.0 3.0 | 6.7 6.7 | mAdc |
| DC Quiescent Power Dissipation ($V_O = 0$) | P_D | — | 90 | 150 | — | 90 | 200 | mW |

See current MC1539/1439 data sheet for additional information.

PACKAGING AND HANDLING

The MCC1539/MCC1439 operational amplifier is now available as a single monolithic die or encapsulated in the TO-99 and TO-116 hermetic and plastic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1558
MCC1458

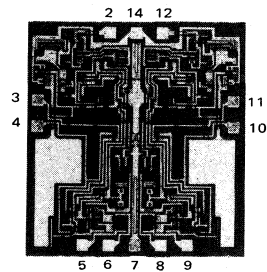
DUAL MC1741
INTERNALLY COMPENSATED, HIGH PERFORMANCE
MONOLITHIC OPERATIONAL AMPLIFIER

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1558 and MCC1458 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

(DUAL MC1741)
DUAL
OPERATIONAL AMPLIFIER
INTEGRATED CIRCUIT
MONOLITHIC SILICON



MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | MCC1558 | MCC1458 | Unit |
|-------------------------------|----------------|------------------------|---------------------|------------------|
| Power Supply Voltage | V^+ V^- | +22 -22 | +18 -18 | Vdc |
| Differential Input Signal | V_{in} | ± 30 | | Volts |
| Common-Mode Input Swing | CMV_{in} | ± 15 | | Volts |
| Output Short Circuit Duration | t_S | Continuous | | |
| Operating Temperature Range | T_A | MCC1558 -55 to +125 | MCC1458 0 to +75 | $^\circ\text{C}$ |
| Junction Temperature Range | T_J | -65 to +150 | | $^\circ\text{C}$ |

FIGURE 1 – CIRCUIT SCHEMATIC

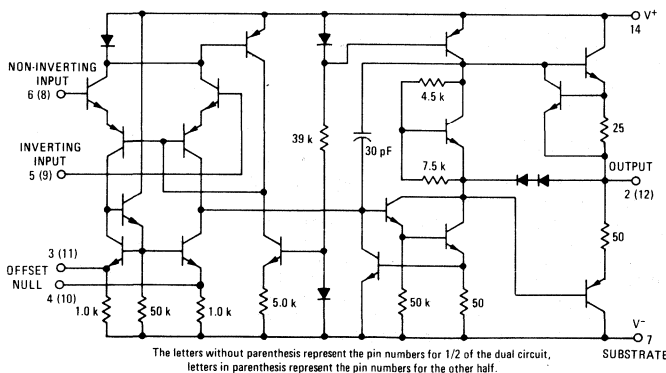
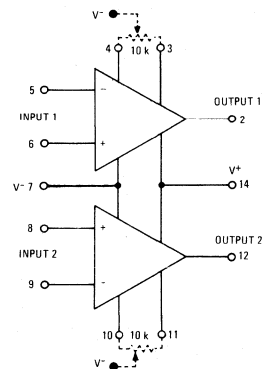


FIGURE 2 – OFFSET ADJUST



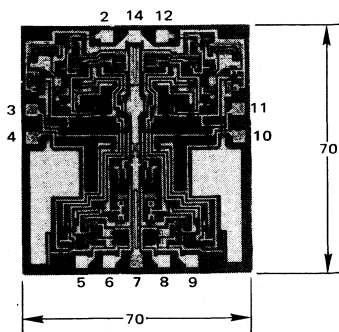
MCC1558, MCC1458 (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MCC1558 | | | MCC1458 | | | Unit |
|---|---------------|----------|----------|-----|----------|----------|-----|------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | I_b | — | 0.2 | 0.5 | — | 0.2 | 0.5 | μAdc |
| Input Offset Current | $ I_{io} $ | — | 0.03 | 0.2 | — | 0.03 | 0.2 | μAdc |
| Input Offset Voltage ($R_S \leq 10$ k ohms) | $ V_{io} $ | — | 1.0 | 5.0 | — | 2.0 | 6.0 | mVdc |
| Differential Input Impedance (Open-Loop, $f = 20$ Hz) | | | | | | | | |
| Parallel Input Resistance | R_p | — | 1.0 | — | — | 1.0 | — | Megohm |
| Parallel Input Capacitance | C_p | — | 6.0 | — | — | 6.0 | — | pF |
| Common-Mode Input Impedance ($f = 20$ Hz) | $Z_{(in)}$ | — | 200 | — | — | 200 | — | Megohms |
| Common-Mode Input Voltage Swing | CMV_{in} | — | ± 13 | — | — | ± 13 | — | Vpk |
| Common-Mode Rejection Ratio ($f = 100$ Hz) | CM_{rej} | — | 90 | — | — | 90 | — | dB |
| Open-Loop Voltage Gain ($V_o = \pm 10$ V, $R_L = 2.0$ k ohms) | A_{VOL} | 50,000 | 200,000 | — | 20,000 | 100,000 | — | V/V |
| Power Bandwidth ($A_V = 1$, $R_L = 2.0$ k ohms, THD $\leq 5\%$, $V_o = 20$ Vp-p) | P_{BW} | — | 14 | — | — | 14 | — | kHz |
| Unity Gain Crossover Frequency (open-loop) | | — | 1.1 | — | — | 1.1 | — | MHz |
| Phase Margin (open-loop, unity gain) | | — | 65 | — | — | 65 | — | degrees |
| Gain Margin | | — | 11 | — | — | 11 | — | dB |
| Slew Rate (Unity Gain) | dV_{out}/dt | — | 0.8 | — | — | 0.8 | — | V/ μs |
| Output Impedance ($f = 20$ Hz) | Z_{out} | — | 75 | — | — | 75 | — | ohms |
| Short-Circuit Output Current | I_{SC} | — | 20 | — | — | 20 | — | mAdc |
| Output Voltage Swing ($R_L = 10$ k ohms) | V_o | ± 12 | ± 14 | — | ± 12 | ± 14 | — | Vpk |
| Power Supply Sensitivity $V^- = \text{constant}$, $R_S \leq 10$ k ohms | S^+ | — | 30 | 150 | — | 30 | 150 | $\mu\text{V/V}$ |
| $V^+ = \text{constant}$, $R_S \leq 10$ k ohms | S^- | — | 30 | 150 | — | 30 | 150 | |
| Power Supply Current | I_{D^+} | — | 2.3 | 5.0 | — | 2.3 | 5.6 | mAdc |
| | I_{D^-} | — | 2.3 | 5.0 | — | 2.3 | 5.6 | |
| DC Quiescent Power Dissipation ($V_o = 0$) | P_D | — | 70 | 150 | — | 70 | 170 | mW |

See current MC1558/MC1458 data sheet for additional information.

MCC1558/MCC1458 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

PACKAGING AND HANDLING

The MCC1558/MCC1458 dual operational amplifiers are now available as a single monolithic die or encapsulated in a variety of hermetic and plastic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

NEGATIVE VOLTAGE REGULATORS

MCC1563 MCC1463

MONOLITHIC NEGATIVE VOLTAGE REGULATOR

The MCC1563/MCC1463 is a "three terminal" negative regulator designed to deliver continuous load current up to 500 mA dc and provide a maximum negative input voltage of -40 V dc. Output current capability can be increased to greater than 10 A dc through use of one or more external transistors.

The MCC1563 and MCC1463 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Electronic "Shutdown" and Short-Circuit Protection
- Low Output Impedance - 20 Milliohms typ
- Excellent Temperature Stability - $TCV_O = \pm 0.002\%/^{\circ}C$ typ
- High Ripple Rejection - 0.002% typ
- 500 mA Current Capability

NEGATIVE-POWER-SUPPLY VOLTAGE REGULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

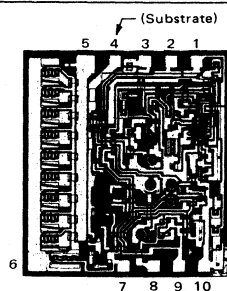


FIGURE 1 - TYPICAL CIRCUIT CONNECTION
 $-3.5 \leq V_O \leq -37$ V dc, $1 \leq I_L \leq 500$ mA

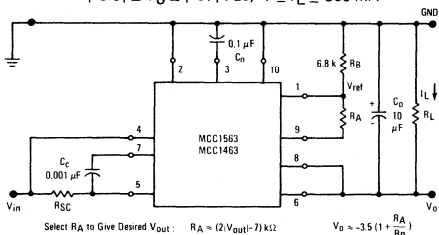


FIGURE 2 - TYPICAL NPN CURRENT BOOST CONNECTION
($V_O = -5.2$ V dc, $I_L = 10$ A dc [max])

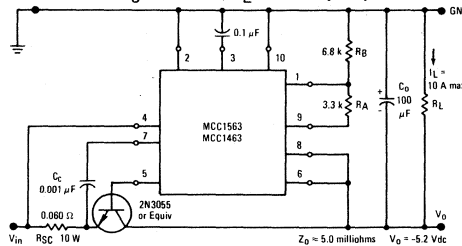
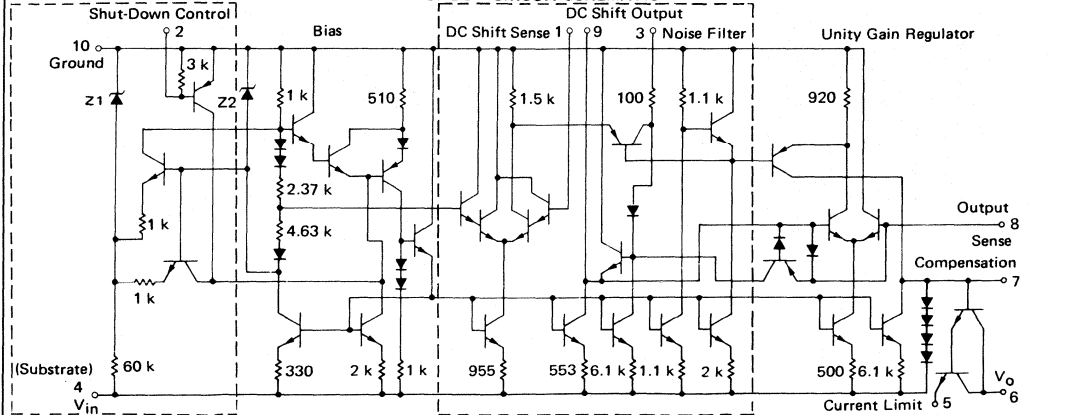


FIGURE 3 - CIRCUIT SCHEMATIC



MCC1563, MCC1463 (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

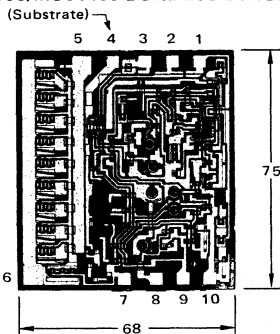
| Rating | | Symbol | MCC1563 | MCC1463 | Unit |
|-----------------------------|--|-----------------------------|-------------------------|---------|------------------|
| Input Voltage | | V_{in} | -40 | -35 | Vdc |
| Peak Load Current | | $I_{L\text{ pk}}$ | 600 | | mA |
| Current, Pin 2 | | $I_{\text{pin 2}}$ | 10 | | mA |
| Operating Temperature Range | | MCC1563 MCC1463 T_A | -55 to +125 0 to +75 | | $^\circ\text{C}$ |
| Junction Temperature Range | | T_J | -65 to +175 | | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS ($I_L = 100\text{ mAdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MCC1563 | | | MCC1463 | | | Unit |
|---|------------------|---------|-------------|------|---------|-------------|------|---------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage | V_{in} | — | — | -40 | — | — | -35 | Vdc |
| Output Voltage Range | V_O | -3.6 | — | -37 | -3.8 | — | -32 | Vdc |
| Reference Voltage (Pin 1 to Ground) | V_{ref} | -3.4 | -3.5 | -3.6 | -3.2 | -3.5 | -3.8 | Vdc |
| Minimum Input-Output Voltage Differential ($R_{SC} = 0$) | $ V_{in} - V_O $ | — | 1.5 | 2.7 | — | 1.5 | 3.0 | Vdc |
| Bias Current ($I_L = 1.0\text{ mAdc}$, $I_b = I_{in} - I_L$) | I_b | — | 7.0 | 11 | — | 7.0 | 14 | mAdc |
| Output Noise ($C_n = 0.1\ \mu\text{F}$, $f = 10\text{ Hz to }5.0\text{ MHz}$) | v_n | — | 120 | — | — | 120 | — | $\mu\text{V(rms)}$ |
| Temperature Coefficient of Output Voltage | TCV_O | — | ± 0.002 | — | — | ± 0.002 | — | $\%/^\circ\text{C}$ |
| Input Regulation | Reg_{in} | — | 0.002 | — | — | 0.003 | — | $\%/V_O$ |
| Load Regulation ($T_J = \text{Constant}$ [$1.0\text{ mA} \leq I_L \leq 20\text{ mA}$]) | Reg_L | — | 0.4 | — | — | 0.7 | — | mV |
| Output Impedance ($f = 1.0\text{ kHz}$) | Z_O | — | 20 | — | — | 35 | — | milliohms |
| Shutdown Current ($V_{in} = -35\text{ Vdc}$) | I_{sd} | — | 7.0 | 15 | — | 14 | 50 | μAdc |

See current MC1563/1463 data sheet for additional information

MCC1563/MCC1463 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).

Die Dimensions

Thickness = 8.0

Bonding Pads = 4.0×4.0

PACKAGING AND HANDLING

The MCC1563/MCC1463 voltage regulator is now available as a single monolithic die or encapsulated in the Case 602A and Case 614 hermetic packages. The phosphosilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

POSITIVE VOLTAGE REGULATORS

MCC1569 MCC1469

MONOLITHIC VOLTAGE REGULATOR

The MCC1569 and MCC1469 are positive voltage regulators designed to deliver continuous load current up to 500 mA dc. Output voltage is adjustable from 2.5 V dc to 37 V dc. Systems requiring both a positive and negative regulated voltage can use the MCC1569 and MCC1563 as complementary regulators with a common input ground.

The MCC1569 and MCC1469 employ phosphosilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Electronic "Shut-Down" Control
- Excellent Load Regulation (Low Output Impedance – 20 milliohms typ)
- High Power Capability: Up to 17.5 Watts
- Excellent Temperature Stability: $\pm 0.002\%/^{\circ}\text{C}$ typ
- High Ripple Rejection: 0.002%/V typ

POSITIVE VOLTAGE REGULATOR INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED

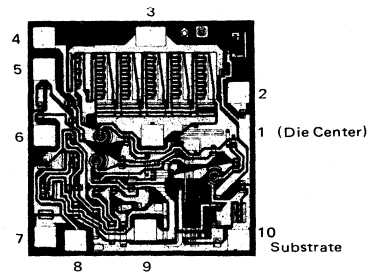
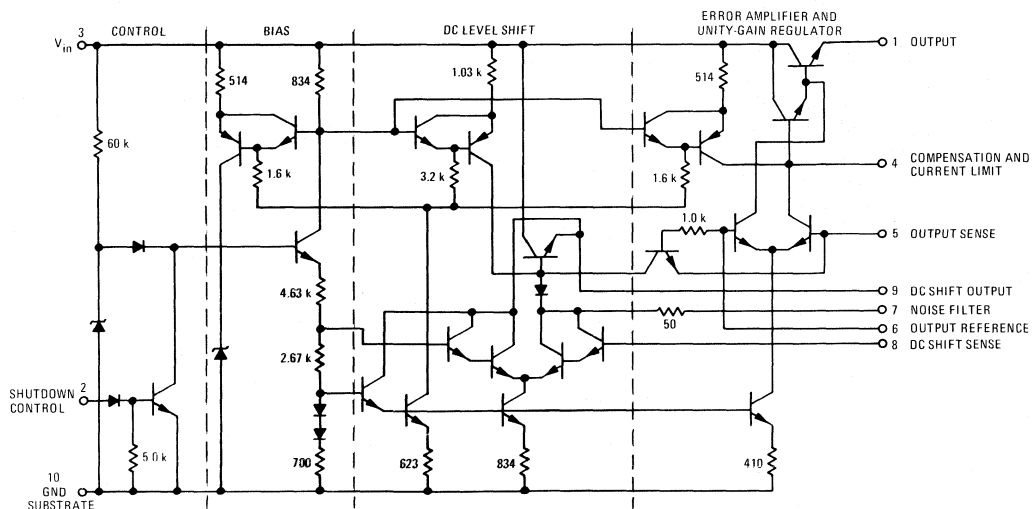


FIGURE 1 – CIRCUIT SCHEMATIC



MCC1569, MCC1469 (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

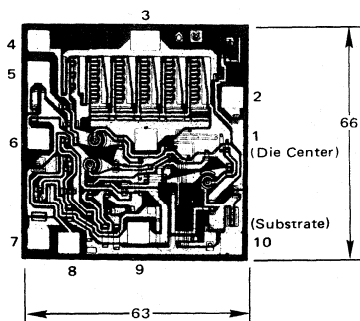
| Rating | Symbol | MCC1569 | MCC1469 | Unit |
|-----------------------------|--------------|-------------------------|---------|------------------|
| Input Voltage | V_{in} | 40 | 35 | Vdc |
| Peak Load Current | I_{pk} | 600 | | mA |
| Current, Pin 2 | $I_{pin\ 2}$ | 10 | | mA |
| Current, Pin 9 | $I_{pin\ 9}$ | 5.0 | | |
| Operating Temperature Range | T_A | -55 to +125 0 to +75 | | $^\circ\text{C}$ |
| Junction Temperature Range | T_J | -65 to +150 | | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MCC1569 | | | MCC1469 | | | Unit |
|---|----------------|---------|-------------|-----|---------|-------------|-----|---------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage | V_{in} | — | — | 40 | — | — | 35 | Vdc |
| Output Voltage Range | V_o | 2.5 | — | 37 | 2.5 | — | 32 | Vdc |
| Reference Voltage (Pin 8 to Ground) | V_{ref} | 3.4 | 3.5 | 3.6 | 3.2 | 3.5 | 3.8 | Vdc |
| Minimum Input-Output Voltage Differential | $V_{in} - V_o$ | — | 2.1 | 2.7 | — | 2.1 | 3.0 | Vdc |
| Bias Current ($I_L = 1.0\text{ mAdc}$, $R_Z = 6.8\text{ k ohms}$, $I_b = I_{in} - I_L$) | I_b | — | 4.0 | 9.0 | — | 5.0 | 12 | mAdc |
| Output Noise ($C_n = 0.1\ \mu\text{F}$, $f = 10\text{ Hz to } 5.0\text{ MHz}$) | v_n | — | 0.150 | — | — | 0.150 | — | mV(rms) |
| Temperature Coefficient of Output Voltage | TCV_o | — | ± 0.002 | — | — | ± 0.002 | — | $\%/^\circ\text{C}$ |
| Input Regulation | Reg_{in} | — | 0.002 | — | — | 0.003 | — | $\%/V_{in}$ |
| Output Impedance ($C_c = 0.001\ \mu\text{F}$, $R_{SC} = 1.0\text{ ohm}$, $f = 1.0\text{ kHz}$, $V_{in} = +14\text{ Vdc}$, $V_o = +10\text{ Vdc}$) | Z_{out} | — | 20 | — | — | 35 | — | milliohms |
| Shutdown Current ($V_{in} = +35\text{ Vdc}$) | I_{sd} | — | 70 | 150 | — | 140 | 500 | μAdc |

See current MC1569/1469 data sheet for additional information.

MCC1569/MCC1469 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).

Die Dimensions

Thickness = 8.0

Bonding Pads = 4.0×4.0

PACKAGING AND HANDLING

The MCC1569/MCC1469 voltage regulator is now available as a single monolithic die or encapsulated in the Case 602A and Case 614 hermetic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1595 MCC1495

MONOLITHIC FOUR-QUADRANT MULTIPLIER

... designed for uses where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

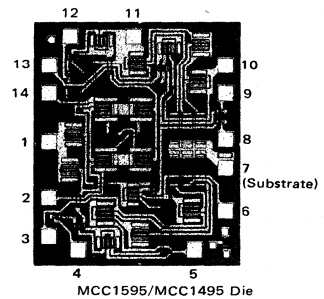
The MCC1595 and MCC1495 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

*When used with an operational amplifier.

- Excellent Linearity – 0.5% typ Error on X-Input, 1% typ Error on Y-Input – MCC1595
- Excellent Linearity – 1% typ Error on X-Input, 2% typ Error on Y-Input – MCC1495
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts

LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

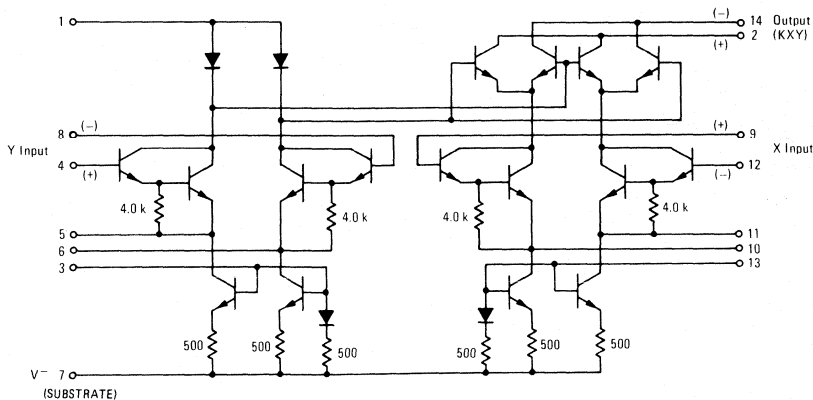
MONOLITHIC SILICON
EPITAXIAL PASSIVATED



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---------------------------|--------------------------------------|------------------|
| Applied Voltage ($V_2-V_1, V_{14}-V_1, V_1-V_9, V_1-V_{12}, V_1-V_4,$ $V_1-V_9, V_{12}-V_7, V_9-V_7, V_8-V_7, V_4-V_7$) | ΔV | 30 | Vdc |
| Differential Input Signal | $V_{12}-V_9$ V_4-V_8 | $\pm(6+1/3 R_X)$ $\pm(6+1/3 R_Y)$ | Vdc Vdc |
| Maximum Bias Current | I_3 I_{13} | 10 10 | mA |
| Operating Temperature Range | MCC1595 MCC1495 | T_A | $^\circ\text{C}$ |
| Junction Temperature Range | T_J | -55 to +125 0 to +70 | $^\circ\text{C}$ |

CIRCUIT SCHEMATIC



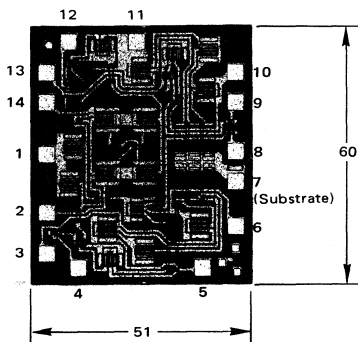
MCC1595, MCC1495 (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +32\text{ V}$, $V^- = -15\text{ V}$, $T_A = 25^\circ\text{C}$, $I_3 = I_{13} = 1\text{ mA}$, $R_X = R_Y = 15\text{ k}\Omega$, $R_L = 11\text{ k}\Omega$ unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|--|--------------------|-------------|--------|-------------|--------|---------------|
| Linearity: Output Error in Percent of Full Scale: $-10 < V_X < +10$ ($V_Y = \pm 10\text{ V}$) $-10 < V_Y < +10$ ($V_X = \pm 10\text{ V}$) | MCC1495 | E_{RX} | — | 1.0 | — | % |
| | MCC1595 | | — | 0.5 | — | |
| | MCC1495 | E_{RY} | — | 2.0 | — | % |
| | MCC1595 | | — | 1.0 | — | |
| Squaring Mode Error: Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment | MCC1495 MCC1595 | E_{SQ} | — — | 0.75 0.5 | — — | % |
| Scale Factor (Adjustable) $(K = \frac{2R_L}{I_3 R_X R_Y})$ | | K | — | 0.1 | — | — |
| Input Resistance ($f = 20\text{ Hz}$) | MCC1495 | R_{INX} | — | 20 | — | Megohms |
| | MCC1595 | | — | 35 | — | |
| | MCC1495 | R_{INY} | — | 20 | — | Megohms |
| | MCC1595 | | — | 35 | — | |
| Differential Output Resistance ($f = 20\text{ Hz}$) | | R_o | — | 300 | — | k Ohms |
| Input Bias Current $I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$ | MCC1495 | I_{bx} | — | 2.0 | 12 | μA |
| | MCC1595 | | — | 2.0 | 8.0 | |
| | MCC1495 | I_{by} | — | 2.0 | 12 | μA |
| | MCC1595 | | — | 2.0 | 8.0 | |
| Input Offset Current $ I_9 - I_{12} $ $ I_4 - I_8 $ | MCC1495 | $ I_{iox} $ | — | 0.4 | 2.0 | μA |
| | MCC1595 | | — | 0.2 | 1.0 | |
| | MCC1495 | $ I_{ioy} $ | — | 0.4 | 2.0 | μA |
| | MCC1595 | | — | 0.2 | 1.0 | |
| Output Offset Current $ I_{14} - I_{12} $ | MCC1495 | $ I_{oo} $ | — | 20 | 100 | μA |
| | MCC1595 | | — | 10 | 50 | |
| Frequency Response 3.0 dB Bandwidth 3° Relative Phase Shift Between V_X and V_Y 1% Absolute Error Due to Input-Output Phase Shift | | BW_{3dB} | — | 3.0 | — | MHz |
| | | f_ϕ | — | 750 | — | kHz |
| | | f_θ | — | 30 | — | kHz |
| Common Mode Input Swing (Either input) | MCC1495 | CMV | — | ± 12 | — | Vdc |
| | MCC1595 | | — | ± 13 | — | |
| Common Mode Quiescent Output Voltage | | V_{o1} | — | 21 | — | Vdc |
| | | V_{o2} | — | 21 | — | |
| Differential Output Voltage Swing Capability | | V_{out} | — | ± 14 | — | V_{peak} |
| Power Supply Sensitivity | | S^+ | — | 5.0 | — | mV/V |
| | | S^- | — | 10 | — | |
| Power Supply Current | | I_7 | — | 6.0 | 7.0 | mA |
| DC Power Dissipation | | P_D | — | 135 | 170 | mW |

See current MCC1595/1495 data sheet for additional information.

MCC1595/MCC1495 BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).

Die Dimensions

Thickness = 8.0

Bonding Pads = 4.0×4.0

PACKAGING AND HANDLING

The MCC1595/MCC1495 is the Four-Quadrant Multiplier now available in die (chip) form. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1709
MCC1709C

MONOLITHIC OPERATIONAL AMPLIFIER

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1709 and MCC1709C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

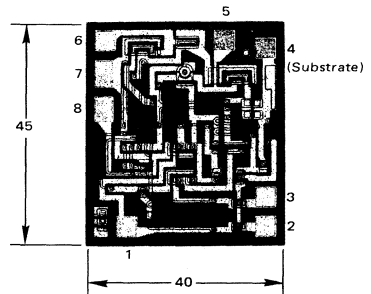
- High-Performance Open Loop Gain Characteristics
AVOL = 45,000 typical
- Low Temperature Drift – $\pm 3.0 \mu V/^\circ C$
- Large Output Voltage Swing – $\pm 14 V$ typical @ $\pm 15 V$ Supply
- Low Output Impedance – $Z_{out} = 150$ ohms typical

MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|-------------------------------|------------------------------|-------------------------|------------|
| Power Supply Voltage | V^+ V^- | +18 -18 | Vdc |
| Differential Input Signal | V_{in} | ± 5.0 | Volts |
| Common Mode Input Swing | CMV_{in} | $\pm V^+$ | Volts |
| Load Current | I_L | 10 | mA |
| Output Short Circuit Duration | t_S | 5.0 | s |
| Operating Temperature Range | MCC1709 MCC1709C T_A | -55 to +125 0 to +75 | $^\circ C$ |
| Junction Temperature Range | T_J | -55 to +150 | $^\circ C$ |

**OPERATIONAL AMPLIFIER
INTEGRATED CIRCUIT
MONOLITHIC SILICON**

**OUTLINE DIMENSIONS
and BONDING DIAGRAM**



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0×4.0

FIGURE 1 – CIRCUIT SCHEMATIC

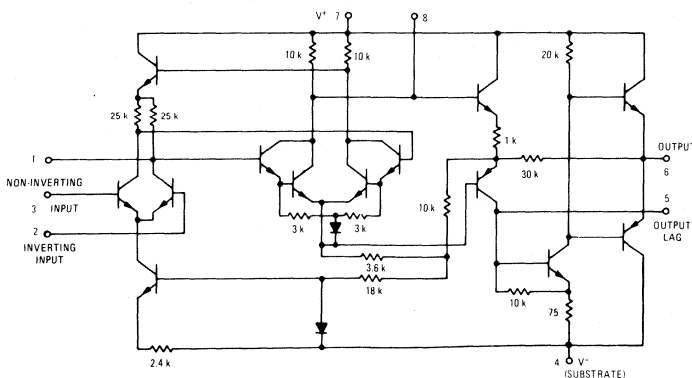
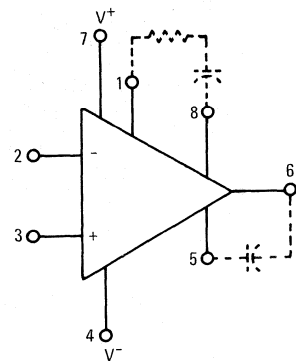


FIGURE 2 – EQUIVALENT CIRCUIT



MCC1709, MCC1709C (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MCC1709 | | | MCC1709C | | | Unit |
|---|---------------|----------------------|----------------------|--------|----------------------|----------------------|-----|------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Open Loop Voltage Gain ($V_O = \pm 10$ V) | A_{VOL} | 25,000 | 45,000 | 70,000 | 15,000 | 45,000 | — | — |
| Output Impedance ($f = 20$ Hz) | Z_{out} | — | 150 | — | — | 150 | — | Ω |
| Input Impedance ($f = 20$ Hz) | Z_{in} | — | 400 | — | — | 250 | — | $k\Omega$ |
| Output Voltage Swing ($R_L = 10$ $k\Omega$) ($R_L = 2.0$ $k\Omega$) | V_O | ± 12 ± 10 | ± 14 ± 13 | — | ± 12 ± 10 | ± 14 ± 13 | — | V_{peak} |
| Input Common-Mode Voltage Swing | CMV_{in} | — | ± 10 | — | — | ± 10 | — | V_{peak} |
| Common-Mode Rejection Ratio ($f = 20$ Hz) | CM_{rej} | — | 90 | — | — | 90 | — | dB |
| Input Bias Current | I_b | — | 0.2 | 0.5 | — | 0.3 | 1.5 | μA |
| Input Offset Current | $ I_{io} $ | — | 0.05 | 0.2 | — | 0.1 | 0.5 | μA |
| Input Offset Voltage | $ V_{io} $ | — | 1.0 | 5.0 | — | 2.0 | 7.5 | mV |
| Step Response | | | | | | | | |
| Gain = 100, 5.0% overshoot | t_f | — | 0.8 | — | — | 0.8 | — | μs |
| | t_{pd} | — | 0.38 | — | — | 0.38 | — | μs |
| | dV_{out}/dt | — | 12 | — | — | 12 | — | $\text{V}/\mu\text{s}$ |
| Gain = 10, 10% overshoot | t_f | — | 0.6 | — | — | 0.6 | — | μs |
| | t_{pd} | — | 0.34 | — | — | 0.34 | — | μs |
| | dV_{out}/dt | — | 1.7 | — | — | 1.7 | — | $\text{V}/\mu\text{s}$ |
| Gain = 1, 5.0% overshoot | t_f | — | 2.2 | — | — | 2.2 | — | μs |
| | t_{pd} | — | 1.3 | — | — | 1.3 | — | μs |
| | dV_{out}/dt | — | 0.25 | — | — | 0.25 | — | $\text{V}/\mu\text{s}$ |
| Power Supply Current | I_{D^+} | — | 2.7 | 5.5 | — | 2.7 | 6.7 | mA_{dc} |
| | I_{D^-} | — | 2.7 | 5.5 | — | 2.7 | 6.7 | |
| DC Quiescent Power Dissipation (Power Supply = ± 15 V, $V_O = 0$) | P_D | — | 80 | 165 | — | 80 | 200 | mW |
| Positive Supply Sensitivity (V^- constant) | S^+ | — | 25 | 150 | — | 25 | 200 | $\mu\text{V}/\text{V}$ |
| Negative Supply Sensitivity (V^+ constant) | S^- | — | 25 | 150 | — | 25 | 200 | $\mu\text{V}/\text{V}$ |

See current MC1709/1709C data sheet for additional information

PACKAGING AND HANDLING

The MCC1709/MCC1709C operational amplifier is now available as a single monolithic die or encapsulated in a variety of hermetic and plastic packages. The phosphosilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

DIFFERENTIAL COMPARATORS

MCC1710 MCC1710C

MONOLITHIC DIFFERENTIAL VOLTAGE COMPARATOR

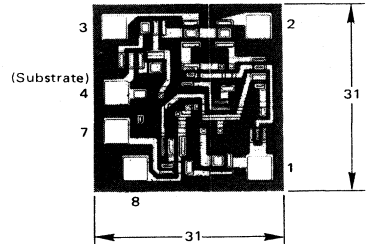
... designed for use in level detection, low-level sensing, and memory applications.

The MCC1710 and MCC1710C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Differential Input Characteristics -
Input Offset Voltage = 1.0 mV
Offset Voltage Drift = 3.0 $\mu\text{V}/^\circ\text{C}$
- Fast Response Time - 40 ns
- Output Compatible With All Saturating Logic Forms -
 $V_{\text{out}} = +3.2 \text{ V to } -0.5 \text{ V typical}$
- Low Output Impedance - 200 ohms

DIFFERENTIAL COMPARATOR INTEGRATED CIRCUIT MONOLITHIC SILICON EPITAXIAL PASSIVATED

OUTLINE DIMENSIONS and BONDING DIAGRAM

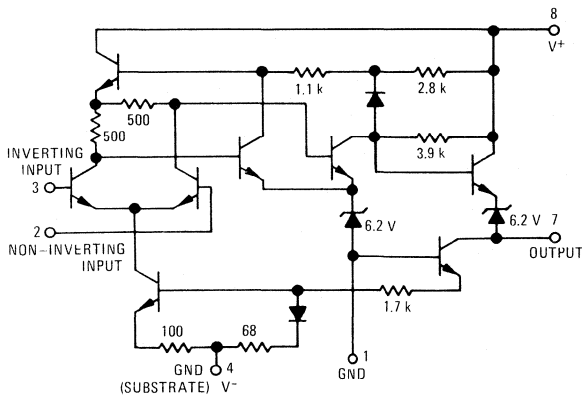


All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

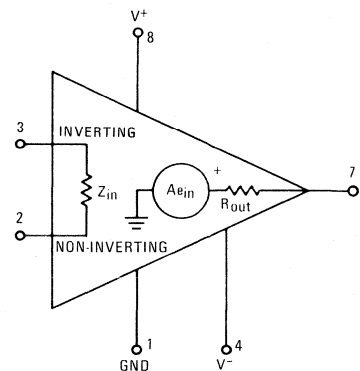
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit | |
|-----------------------------|-------------------|-------------|------------------|------------------|
| Power Supply Voltage | V^+ | +14 | Vdc | |
| | V^- | -7.0 | | |
| Differential Input Signal | V_{in} | ± 5.0 | Volts | |
| Common Mode Input Swing | CMV_{in} | ± 7.0 | Volts | |
| Peak Load Current | I_L | 10 | mA | |
| Operating Temperature Range | T_A | MCC1710 | -55 to +125 | $^\circ\text{C}$ |
| | | MCC1710C | 0 to +75 | |
| Junction Temperature Range | T_J | -65 to +150 | $^\circ\text{C}$ | |

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



MCC1710, MCC1710C(continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +12$ Vdc, $V^- = -6.0$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MCC1710 | | | MCC1710C | | | Unit |
|--|------------|---------|------|-----|----------|------|-----|-----------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($V_O = 1.4$ Vdc) | V_{io} | — | 1.0 | 2.0 | — | 1.5 | 5.0 | mVdc |
| Input Bias Current ($V_O = 1.4$ Vdc) | I_b | — | 12 | 20 | — | 15 | 25 | μAdc |
| Output Resistance | R_{out} | — | 200 | — | — | 200 | — | Ohms |
| Positive Output Voltage ($V_{in} \geq 5.0$ mV, $0 \leq I_O \leq 5.0$ mA) | V_{OH} | 2.5 | 3.2 | 4.0 | 2.5 | 3.2 | 4.0 | Vdc |
| Negative Output Voltage ($V_{in} \leq -5.0$ mV) | V_{OL} | -1.0 | -0.5 | 0 | -1.0 | -0.5 | 0 | Vdc |
| Output Sink Current ($V_{in} \geq -5.0$ mV, $V_{out} \geq 0$) | I_s | 2.0 | 2.5 | — | 2.0 | 2.5 | — | mAdc |
| Common Mode Rejection Ratio ($V^- = -7.0$ Vdc, $R_S \leq 200 \Omega$) | CM_{rej} | — | 100 | — | — | 100 | — | dB |
| Propagation Delay Time For Positive and Negative Going Input Pulse | t_{pd} | — | 40 | — | — | 40 | — | ns |
| Power Supply Current ($V_{out} \leq 0$ Vdc) | I_{D^+} | — | 6.4 | 9.0 | — | 6.4 | 9.0 | mAdc |
| | I_{D^-} | — | 5.5 | 7.0 | — | 5.5 | 7.0 | |
| DC Quiescent Power Dissipation | P_D | — | 115 | 150 | — | 110 | 150 | mW |

See current MC1710/1710C data sheet for additional information.

PACKAGING AND HANDLING

The MCC1710/MCC1710C differential comparator is now available as a single monolithic die or encapsulated in the TO-91, TO-99, and TO-116 hermetic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

DIFFERENTIAL COMPARATORS

MCC1711 MCC1711C

MONOLITHIC DUAL DIFFERENTIAL VOLTAGE COMPARATOR

... designed for use in level detection, low-level sensing, and memory applications.

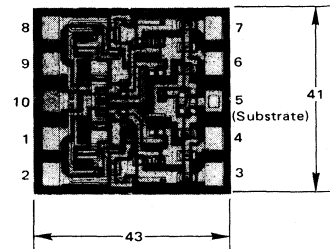
The MCC1711 and MCC1711C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Differential Input –
Input Offset Voltage = 1.0 mV
Offset Voltage Drift = 5.0 $\mu\text{V}/^\circ\text{C}$
- Fast Response Time – 40 ns
- Output Compatible with All Saturating Logic Forms –
 $V_{\text{out}} = +4.5 \text{ V to } -0.5 \text{ V Typical}$
- Low Output Impedance – 200 Ohms

DUAL DIFFERENTIAL COMPARATOR INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED

OUTLINE DIMENSIONS and BONDING DIAGRAM

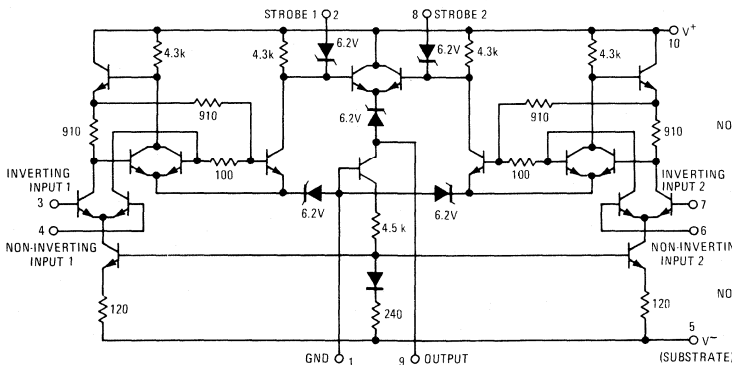


All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

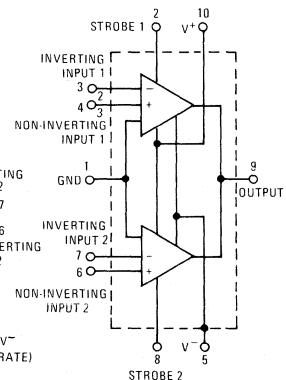
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit | |
|-----------------------------|--------------------------|-----------------|------------------|------------------|
| Power Supply Voltage | V^+ | +14 | Vdc | |
| | V^- | -7.0 | Vdc | |
| Differential Input Signal | V_{in} | ± 5.0 | Volts | |
| Common Mode Input Swing | $\text{CM}V_{\text{in}}$ | ± 7.0 | Volts | |
| Peak Load Current | I_L | 50 | mA | |
| Operating Temperature Range | MCC1711 | T_A | -55 to $+125$ | $^\circ\text{C}$ |
| | MCC1711C | | 0 to $+75$ | |
| Junction Temperature Range | T_J | -65 to $+150$ | $^\circ\text{C}$ | |

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (each comparator) ($V^+ = +12$ Vdc, $V^- = -6.0$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MCC1711 | | | MCC1711C | | | Unit |
|---|--------------|---------|------|-----|----------|------|-----|-----------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($V_O = 1.4$ Vdc) | V_{io} | — | 1.0 | 3.5 | — | 1.0 | 5.0 | mVdc |
| Input Bias Current ($V_O = 1.4$ Vdc) | I_b | — | 25 | 75 | — | 25 | 100 | μAdc |
| Output Resistance | R_{out} | — | 200 | — | — | 200 | — | Ohms |
| Positive Output Voltage ($V_{in} \geq 10$ mVdc, $0 \leq I_O \leq 5.0$ mA) | V_{OH} | 2.5 | 3.2 | 5.0 | 2.5 | 3.2 | 5.0 | Vdc |
| Negative Output Voltage ($V_{in} \leq -10$ mVdc) | V_{OL} | -1.0 | -0.5 | 0 | -1.0 | -0.5 | 0 | Vdc |
| Strobed Output Level ($V_{strobe} \leq 0.3$ Vdc) | $V_{OL(st)}$ | -1.0 | — | 0 | -1.0 | — | 0 | Vdc |
| Output Sink Current ($V_{in} \geq -10$ mV, $V_O \geq 0$) | I_S | 0.5 | 0.8 | — | 0.5 | 0.8 | — | mAdc |
| Strobe Current ($V_{strobe} = 100$ mVdc) | I_{st} | — | 1.2 | 2.5 | — | 1.2 | 2.5 | mAdc |
| Response Time ($V_b = 5.0$ mV + V_{io}) | t_R | — | 40 | — | — | 40 | — | ns |
| Strobe Release Time | t_{SR} | — | 12 | — | — | 12 | — | ns |
| Power Supply Current ($V_O \leq 0$ Vdc) | I_{D^+} | — | 8.6 | — | — | 8.6 | — | mAdc |
| | I_{D^-} | — | 3.9 | — | — | 3.9 | — | |
| Power Consumption | | — | 130 | 200 | — | 130 | 200 | mW |

See current MC1711/1711C data sheet for additional information.

PACKAGING AND HANDLING

The MCC1711/MCC1711C dual differential comparator is now available as a single monolithic die or encapsulated in the TO-91, TO-100, and TO-116 hermetic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1723 MCC1723C

MONOLITHIC VOLTAGE REGULATOR CHIP

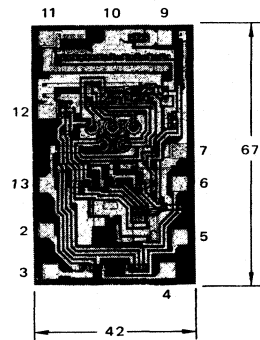
The MCC1723/MCC1723C is a positive or negative voltage regulator designed to deliver load current to 150 mA dc. Output current capability can be increased to several amperes through use of one or more external pass transistors.

The MCC1723 and MCC1723C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mA dc Without External Pass Transistors
- 0.01% Line Regulation
- Adjustable Short-Circuit Protection

VOLTAGE REGULATOR CHIP

MONOLITHIC SILICON
EPITAXIAL PASSIVATED
INTEGRATED CIRCUIT



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

FIGURE 1 - TYPICAL CIRCUIT CONNECTION

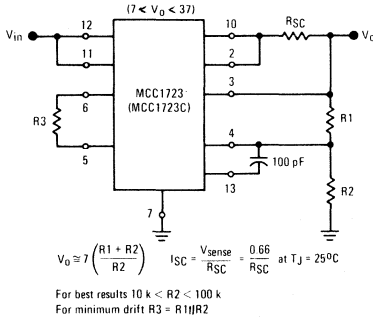
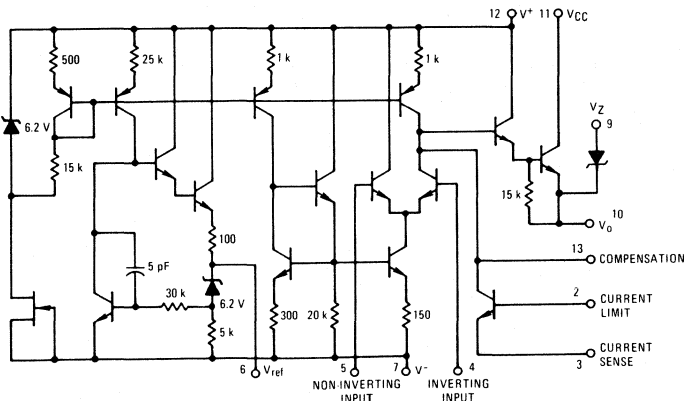


FIGURE 2 - CIRCUIT SCHEMATIC



MCC1723, MCC1723C (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|------------------------------|-------------------------|------------------|
| Pulse Voltage from V^+ to V^- (50 ms) | MCC1723 $V_{in(p)}$ | 50 | V_{peak} |
| Continuous Voltage from V^+ to V^- | V_{in} | 40 | Vdc |
| Input-Output Voltage Differential | $V_{in}-V_o$ | 40 | Vdc |
| Maximum Output Current | I_L | 150 | mAdc |
| Current from V_{ref} | I_{ref} | 15 | mAdc |
| Operating Temperature Range | MCC1723 MCC1723C T_A | -55 to +125 0 to +75 | $^\circ\text{C}$ |
| Junction Temperature Range | T_J | -65 to +150 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: $T_A = +25^\circ\text{C}$, $V_{in} = 12\text{ Vdc}$, $V_o = 5\text{ Vdc}$, $I_L = 1\text{ mAdc}$, $R_{SC} = 0$, $C_1 = 100\text{ pF}$, $C_{ref} = 0$ and divider impedance as seen by the error amplifier $\leq 10\text{ k}\Omega$ connected as shown in Figure 1)

| Characteristic | Symbol | MCC1723 | | | MCC1723C | | | Unit |
|--|--------------|---------|------|------|----------|------|------|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage Range | V_{in} | 9.5 | — | 40 | 9.5 | — | 40 | Vdc |
| Output Voltage Range | V_o | 2.0 | — | 37 | 2.0 | — | 37 | Vdc |
| Input-Output Voltage Differential | $V_{in}-V_o$ | 3.0 | — | 38 | 3.0 | — | 38 | Vdc |
| Reference Voltage | V_{ref} | 6.95 | 7.15 | 7.35 | 6.80 | 7.15 | 7.50 | Vdc |
| Standby Current Drain ($I_L = 0$, $V_{in} = 30\text{ V}$) | I_{sb} | — | 2.3 | 3.5 | — | 2.3 | 4.0 | mAdc |
| Output Noise Voltage ($f = 100\text{ Hz}$ to 10 kHz) $C_{ref} = 0$ $C_{ref} = 5.0\text{ }\mu\text{F}$ | V_n | — | 20 | — | — | 20 | — | $\mu\text{V(rms)}$ |
| Line Regulation ($12\text{ V} < V_{in} < 15\text{ V}$) ($12\text{ V} < V_{in} < 40\text{ V}$) | Reg_{in} | — | 0.01 | 0.1 | — | 0.01 | 0.1 | % V_o |
| Load Regulation ($1.0\text{ mA} < I_L < 50\text{ mA}$) | Reg_{load} | — | 0.03 | 0.15 | — | 0.03 | 0.2 | % V_o |
| Ripple Rejection ($f = 50\text{ Hz}$ to 10 kHz) $C_{ref} = 0$ $C_{ref} = 5.0\text{ }\mu\text{F}$ | Rej_R | — | 74 | — | — | 74 | — | dB |
| Short Circuit Current Limit ($R_{SC} = 10\text{ }\Omega$, $V_o = 0$) | I_{SC} | — | 65 | — | — | 65 | — | mAdc |

See current MC1723/1723C data sheet for additional information.

PACKAGING AND HANDLING

The MCC1723/MCC1723C voltage regulator is now available as a single monolithic die or encapsulated in the Motorola Case 603-03 hermetic package. The phosphosilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1741 MCC1741C

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER CHIP

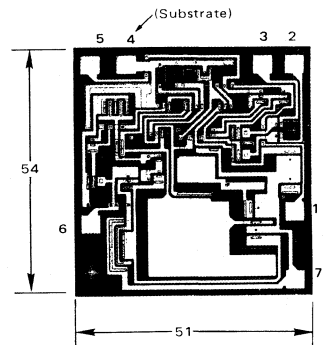
... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1741 and MCC1741C employ phosphosilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER CHIP MONOLITHIC SILICON INTEGRATED CIRCUIT

OUTLINE DIMENSIONS and BONDING DIAGRAM



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0 x 4.0

MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | | Unit |
|--|------------|-------------|-------------|--------------------|
| | | MCC1741C | MCC1741 | |
| Power Supply Voltage | V^+ | +18 | +22 | Vdc |
| | V^- | -18 | -22 | Vdc |
| Differential Input Signal | V_{in} | ± 30 | | Volts |
| Common Mode Input Swing (Note 1) | CMV_{in} | ± 15 | | Volts |
| Output Short Circuit Duration (Note 2) | t_S | Continuous | | |
| Operating Temperature Range | T_A | MCC1741 | -55 to +125 | $^{\circ}\text{C}$ |
| | | MCC1741C | 0 to +75 | |
| Junction Temperature Range | T_J | -65 to +150 | | $^{\circ}\text{C}$ |

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

FIGURE 1 - CIRCUIT SCHEMATIC

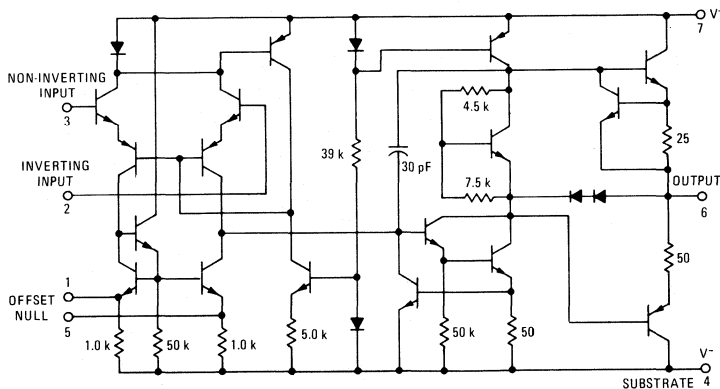
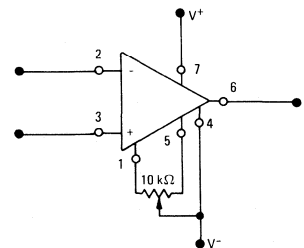


FIGURE 2 - OFFSET ADJUST CIRCUIT



MCC1741, MCC1741C (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = 15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | MCC1741 | | | MCC1741C | | | Unit |
|---|-----------------|----------------------|----------------------|--------|----------------------|----------------------|--------|------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Open Loop Voltage Gain ($R_L = 2.0\text{ k}\Omega$) ($V_O = \pm 10$ V) | A_{VOL} | 50,000 | 200,000 | — | 20,000 | 100,000 | — | — |
| Output Impedance ($f = 20$ Hz) | Z_O | — | 75 | — | — | 75 | — | Ω |
| Input Impedance ($f = 20$ Hz) | Z_{in} | — | 1.0 | — | — | 1.0 | — | Meg Ω |
| Output Voltage Swing ($R_L = 10\text{ k}\Omega$) ($R_L = 2.0\text{ k}\Omega$) | V_O | ± 12 ± 10 | ± 14 ± 13 | — — | ± 12 ± 10 | ± 14 ± 13 | — — | V_{peak} |
| Input Common-Mode Voltage Swing | CMV_{in} | — | ± 13 | — | — | ± 13 | — | V_{peak} |
| Common-Mode Rejection Ratio ($f = 20$ Hz) | CM_{rej} | — | 90 | — | — | 90 | — | dB |
| Input Bias Current | I_b | — | 0.2 | 0.5 | — | 0.2 | 0.5 | μA |
| Input Offset Current | $ I_{io} $ | — | 0.03 | 0.2 | — | 0.03 | 0.2 | μA |
| Input Offset Voltage ($R_S = \leq 10\text{ k}\Omega$) | $ V_{io} $ | — | 1.0 | 5.0 | — | 2.0 | 6.0 | mV |
| Step Response Gain = 100 | t_f | — | 29 | — | — | 29 | — | μs |
| | t_{pd} | — | 8.5 | — | — | 8.5 | — | μs |
| | dV_{out}/dt ① | — | 1.0 | — | — | 1.0 | — | $\text{V}/\mu\text{s}$ |
| Gain = 10 | t_f | — | 3.0 | — | — | 3.0 | — | μs |
| | t_{pd} | — | 1.0 | — | — | 1.0 | — | μs |
| | dV_{out}/dt ① | — | 1.0 | — | — | 1.0 | — | $\text{V}/\mu\text{s}$ |
| Gain = 1 | t_f | — | 0.6 | — | — | 0.6 | — | μs |
| | t_{pd} | — | 0.38 | — | — | 0.38 | — | μs |
| | dV_{out}/dt ① | — | 0.8 | — | — | 0.8 | — | $\text{V}/\mu\text{s}$ |
| Power Supply Current | I_{D^+} | — | 1.67 | 2.83 | — | 1.67 | 2.83 | mA |
| | I_{D^-} | — | 1.67 | 2.83 | — | 1.67 | 2.83 | mA |
| DC Quiescent Power Dissipation (Power Supply = ± 15 V, $V_O = 0$) | P_D | — | 50 | 85 | — | 50 | 85 | mW |
| Positive Supply Sensitivity (V^- constant) | S^+ | — | 30 | 150 | — | 30 | 150 | $\mu\text{V}/\text{V}$ |
| Negative Supply Sensitivity (V^+ constant) | S^- | — | 30 | 150 | — | 30 | 150 | $\mu\text{V}/\text{V}$ |

PACKAGING AND HANDLING

The MCC1741/MCC1741C operational amplifier is now available as a single monolithic die or encapsulated in a variety of hermetic and plastic packages. The phosphorsilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCC1748
MCC1748C

HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIER

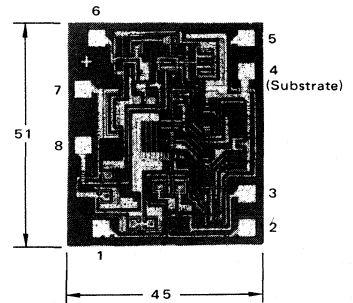
... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCC1748 and MCC1748C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. All dice have a minimum gold-backed thickness of 4000 Angstroms. The interconnecting metalization and bonding pads are of evaporated aluminum.

- Noncompensated MC1741G
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED



All dimensions are nominal and in mils (10^{-3} inches).
Die Dimensions
Thickness = 8.0
Bonding Pads = 4.0×4.0

FIGURE 1 – CIRCUIT SCHEMATIC

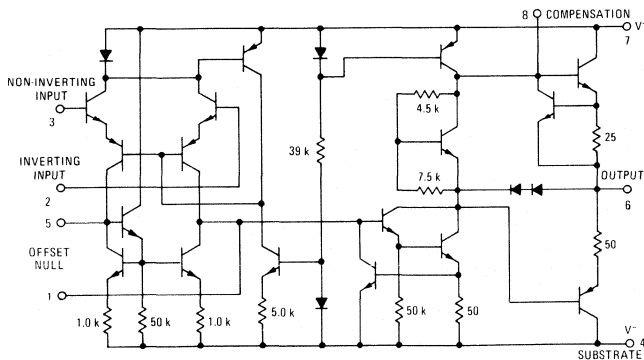
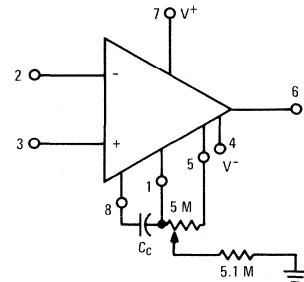


FIGURE 2 – OFFSET ADJUST AND FREQUENCY COMPENSATION



MCC1748, MCC1748C (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | MCC1748 | MCC1748C | Unit |
|--------------------------------------|------------------------------|-------------------------|------------|-------|
| Power Supply Voltage | V^+ V^- | +22 -22 | +18 -18 | Vdc |
| Differential Input Signal | V_{in} | ±30 | | Volts |
| Common-Mode Input Swing ^① | CMV_{in} | ±15 | | Volts |
| Output Short Circuit Duration | t_S | Continuous | | |
| Operating Temperature Range | MCC1748 MCC1748C T_A | -55 to +125 0 to +75 | | °C |
| Junction Temperature Range | T_J | -65 to +150 | | °C |

ELECTRICAL CHARACTERISTICS ($V^+ = +15\text{ Vdc}$, $V^- = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristics | Symbol | MCC1748 | | | MCC1748C | | | Unit |
|---|------------------------|------------|--------------|--------------|------------|--------------|--------------|-----------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | I_b | — | 0.08 | 0.5 | — | 0.08 | 0.5 | μAdc |
| Input Offset Current | $ I_{io} $ | — | 0.02 | 0.2 | — | 0.02 | 0.2 | μAdc |
| Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$) | $ V_{io} $ | — | 1.0 | 5.0 | — | 1.0 | 6.0 | mVdc |
| Differential Input Impedance (Open-Loop, $f = 20\text{ Hz}$) | | | | | | | | |
| Parallel Input Resistance | R_p | — | 2.0 | — | — | 2.0 | — | Megohm |
| Parallel Input Capacitance | C_p | — | 1.4 | — | — | 1.4 | — | pF |
| Common-Mode Input Impedance ($f = 20\text{ Hz}$) | $Z_{(in)}$ | — | 200 | — | — | 200 | — | Megohms |
| Common-Mode Input Voltage Swing | CMV_{in} | — | ±13 | — | — | ±13 | — | V _{pk} |
| Common-Mode Rejection Ratio ($f = 100\text{ Hz}$) | CM_{rej} | — | 90 | — | — | 90 | — | dB |
| Open-Loop Voltage Gain, ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$) | A_{VOL} | 50,000 | 200,000 | — | 20,000 | 200,000 | — | V/V |
| Step Response ($V_{in} = 20\text{ mV}$, $C_C = 30\text{ pF}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$) | | | | | | | | |
| Rise Time | t_r | — | 0.3 | — | — | 0.3 | — | μs |
| Overshoot Percentage | | — | 5.0 | — | — | 5.0 | — | % |
| Slew Rate | dV_{out}/dt | — | 0.8 | — | — | 0.8 | — | V/μs |
| Output Impedance ($f = 20\text{ Hz}$) | Z_{out} | — | 75 | — | — | 75 | — | ohms |
| Short-Circuit Output Current | I_{SC} | — | 25 | — | — | 25 | — | mAdc |
| Output Voltage Swing ($R_L = 10\text{ k}\Omega$) $R_L = 2\text{ k}\Omega$ ($T_A = T_{low}$ to t_{high}) | V_o | ±12 ±10 | ±14 ±13 | — | ±12 ±10 | ±14 ±13 | — | V _{pk} |
| Power Supply Sensitivity | | | | | | | | μV/V |
| $V^- = \text{constant}$, $R_S \leq 10\text{ k}\Omega$ | S+ | — | 30 | 150 | — | 30 | 150 | |
| $V^+ = \text{constant}$, $R_S \leq 10\text{ k}\Omega$ | S- | — | 30 | 150 | — | 30 | 150 | |
| Power Supply Current | I_{D^+} I_{D^-} | — | 1.67 1.67 | 2.83 2.83 | — | 1.67 1.67 | 2.83 2.83 | mAdc |
| DC Quiescent Power Dissipation ($V_O = 0$) | P_D | — | 50 | 85 | — | 50 | 85 | mW |

① For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage.
See current MC1748/1748C data sheet for additional information.

PACKAGING AND HANDLING

The MCC1748/MCC1748C operational amplifier is now available as a single monolithic die or encapsulated in the TO-99 hermetic package. The phosphosilicate passivation protects the metalization and active area of the die but care must be exercised when removing the dice from the shipping carrier to avoid scratching the bonding pads. A vacuum pickup is useful for handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

OPERATIONAL AMPLIFIERS

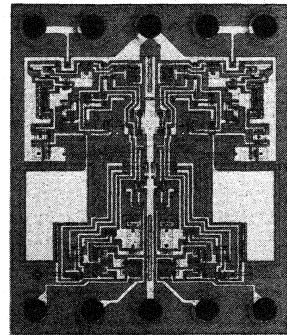
MCCF1558 MCCF1458

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCCF1558 and MCCF1458 employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. The bumps are 90-10 solder on a chrome-copper-gold base. The interconnecting metalization is evaporated aluminum.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

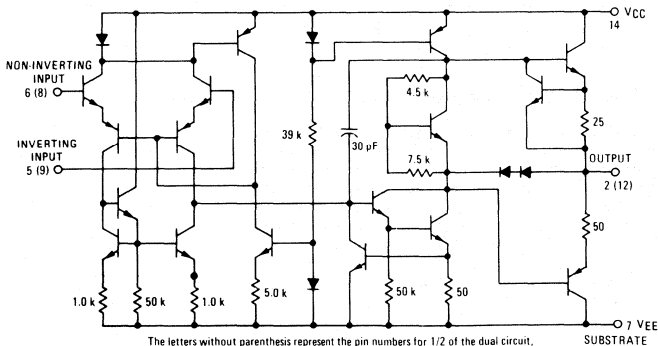
(DUAL MC1741)
DUAL
OPERATIONAL AMPLIFIER
MONOLITHIC SILICON
INTEGRATED CIRCUIT



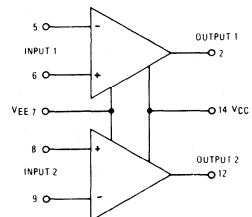
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

| Rating | Symbol | MCCF1558 | MCCF1458 | Unit |
|-------------------------------|----------------------|----------------|----------|-------|
| Power Supply Voltage | V _{CC} | +22 | +18 | Vdc |
| | V _{EE} | -22 | -18 | |
| Differential Input Signal | V _{ID} | ±30 | | Volts |
| Common-Mode Input Swing | V _{IC} | ±15 | | Volts |
| Output Short Circuit Duration | t _S | Continuous | | |
| Operating Temperature Range | MCCF1558 MCCF1458 | T _A | | °C |
| | | -55 to +125 | | |
| Junction Temperature Range | T _J | 0 to +75 | | °C |
| | | -65 to +150 | | |

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The letters without parenthesis represent the pin numbers for 1/2 of the dual circuit, letters in parenthesis represent the pin numbers for the other half.

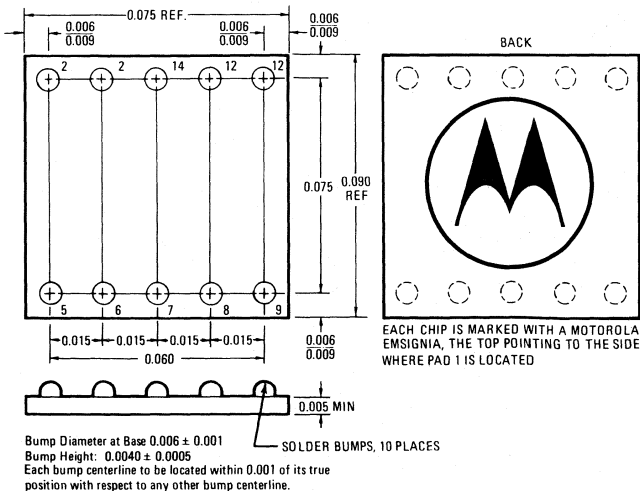


MCCF1558, MCCF1458 (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Symbol | MCCF1558 | | | MCCF1458 | | | Unit |
|--|------------------------|----------|------------|------------|----------|------------|------------|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | I_{IB} | — | 0.2 | 0.5 | — | 0.2 | 0.5 | μA_{dc} |
| Input Offset Current | $ I_{IO} $ | — | 0.03 | 0.2 | — | 0.03 | 0.2 | μA_{dc} |
| Input Offset Voltage ($R_S \leq 10$ k ohms) | $ V_{IO} $ | — | 1.0 | 5.0 | — | 2.0 | 6.0 | mVdc |
| Differential Input Impedance (Open-Loop, $f = 20$ Hz) | | | | | | | | |
| Parallel Input Resistance | R_p | — | 1.0 | — | — | 1.0 | — | Megohm |
| Parallel Input Capacitance | C_p | — | 6.0 | — | — | 6.0 | — | pF |
| Common-Mode Input Impedance ($f = 20$ Hz) | z_{in} | — | 200 | — | — | 200 | — | Megohms |
| Common-Mode Input Voltage Swing | V_{IC} | — | ± 13 | — | — | ± 13 | — | Vpk |
| Common-Mode Rejection Ratio ($f = 100$ Hz) | CMRR | — | 90 | — | — | 90 | — | dB |
| Open-Loop Voltage Gain ($V_O = \pm 10$ V, $R_L = 2.0$ k ohms) | A_{vol} | 50,000 | 200,000 | — | 20,000 | 100,000 | — | V/V |
| Power Bandwidth ($A_v = 1$, $R_L = 2.0$ k ohms, THD $\leq 5\%$, $v_O = 20$ Vp-p) | P_{BW} | — | 14 | — | — | 14 | — | kHz |
| Unity Gain Crossover Frequency (open-loop) | | — | 1.1 | — | — | 1.1 | — | MHz |
| Phase Margin (open-loop, unity gain) | | — | 65 | — | — | 65 | — | degrees |
| Gain Margin | | — | 11 | — | — | 11 | — | dB |
| Slew Rate (Unity Gain) | dV_O/dt | — | 0.8 | — | — | 0.8 | — | V/ μs |
| Output Impedance ($f = 20$ Hz) | z_o | — | 75 | — | — | 75 | — | ohms |
| Short-Circuit Output Current | I_S | — | 20 | — | — | 20 | — | mA_{dc} |
| Output Voltage Swing ($R_L = 10$ k ohms) | V_O | ± 12 | ± 14 | — | ± 12 | ± 14 | — | Vpk |
| Power Supply Sensitivity $V_{EE} = \text{constant}$, $R_S \leq 10$ k ohms $V_{CC} = \text{constant}$, $R_S \leq 10$ k ohms | S^+ S^- | — | 30 30 | 150 150 | — | 30 30 | 150 150 | $\mu\text{V/V}$ |
| Power Supply Current | I_{DCC} I_{DEE} | — | 2.3 2.3 | 5.0 5.0 | — | 2.3 2.3 | 5.6 5.6 | mA_{dc} |
| DC Quiescent Power Dissipation ($V_O = 0$) | P_D | — | 70 | 150 | — | 70 | 170 | mW |

See current MC1558/MC1458 data sheet for additional information.
Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.



The popular 1558 type dual operational amplifier is now available in three chip forms: 1) conventional chips, 2) beam-lead chips and 3) flip-chips, as well as in a variety of plastic and hermetic packages. The flip-chip consists of a silicon chip with solder bumps on the geometry surface to provide easy mechanical mounting and electrical connection. These devices are protected by a thin layer of phosphorsilicate passivation which covers the interconnect metalization and active areas of the die.

Care must be exercised when removing the dice from the shipping carrier to avoid scratching the solder bumps. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCCF1709
MCCF1709C

MONOLITHIC OPERATIONAL AMPLIFIER FLIP-CHIP

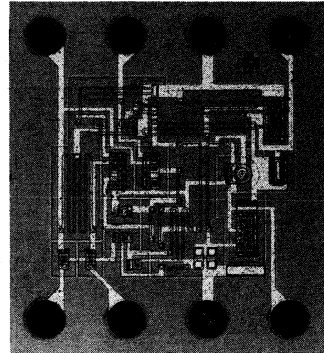
... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCCF1709 and MCCF1709C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. The bumps are 90-10 solder on a chrome-copper-gold base. The interconnecting metalization is evaporated aluminum.

- High-Performance Open Loop Gain Characteristics
 $A_{VOL} = 45,000$ typical
- Low Temperature Drift $-\pm 3.0 \mu V/^{\circ}C$
- Large Output Voltage Swing $-\pm 14 V$ typical @ $\pm 15 V$ Supply
- Low Output Impedance $-z_o = 150$ ohms typical

OPERATIONAL AMPLIFIER

**MONOLITHIC SILICON
INTEGRATED CIRCUIT**



MAXIMUM RATINGS ($T_A = +25^{\circ}C$ unless otherwise noted.)

| Rating | Symbol | Value | Unit | |
|-------------------------------|-------------------------|----------------|-------------|-------------|
| Power Supply Voltage | VCC | +18 | Vdc | |
| | VEE | -18 | | |
| Differential Input Signal | V _{ID} | ± 5.0 | Volts | |
| Common Mode Input Swing | V _{IC} | $\pm V_S$ | Volts | |
| Load Current | I _L | 10 | mA | |
| Output Short Circuit Duration | t _S | 5.0 | s | |
| Operating Temperature Range | MCCF 1709 MCCF 1709C | T _A | -55 to +125 | $^{\circ}C$ |
| | | | 0 to +75 | |
| Junction Temperature Range | T _J | -55 to +150 | $^{\circ}C$ | |

FIGURE 1 - CIRCUIT SCHEMATIC

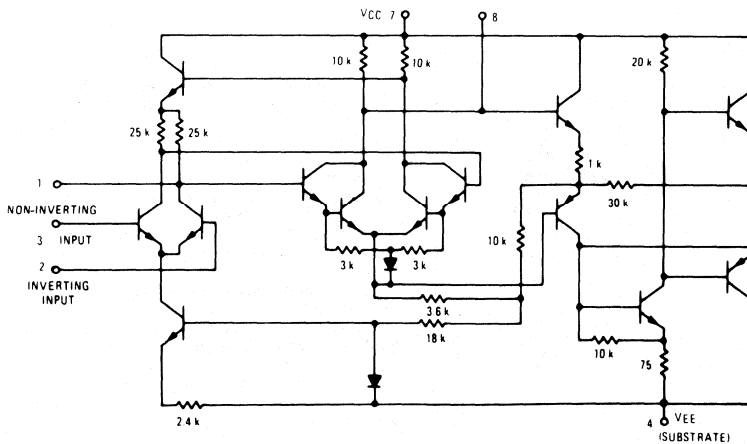
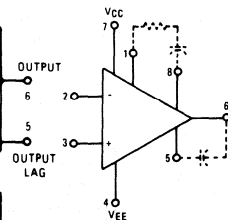


FIGURE 2 - EQUIVALENT CIRCUIT



7

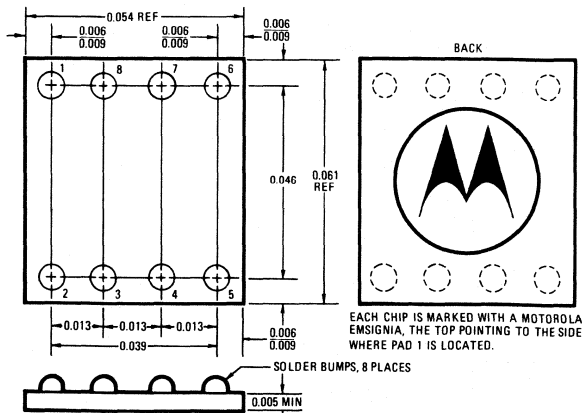
MCCF1709, MCCF1709C (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ Vdc, $V_{EE} = -15$ Vdc, $T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

| Characteristic | Symbol | MCCF1709 | | | MCCF1709C | | | Unit |
|---|------------|----------------------|----------------------|--------|----------------------|----------------------|-----|------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Open Loop Voltage Gain ($V_O = \pm 10\text{V}$) | A_{VOL} | 25,000 | 45,000 | 70,000 | 15,000 | 45,000 | — | — |
| Output Impedance ($f = 20$ Hz) | z_o | — | 150 | — | — | 150 | — | Ω |
| Input Impedance ($f = 20$ Hz) | z_{in} | — | 400 | — | — | 250 | — | $k\Omega$ |
| Output Voltage Swing ($R_L = 10$ $k\Omega$) ($R_L = 2.0$ $k\Omega$) | V_O | ± 12 ± 10 | ± 14 ± 13 | — | ± 12 ± 10 | ± 14 ± 13 | — | V_{peak} |
| Input Common-Mode Voltage Swing | V_{IC} | — | ± 10 | — | — | ± 10 | — | V_{peak} |
| Common-Mode Rejection Ratio ($f = 20$ Hz) | CMRR | — | 90 | — | — | 90 | — | dB |
| Input Bias Current | I_{IB} | — | 0.2 | 0.5 | — | 0.3 | 1.5 | μA |
| Input Offset Current | $ I_{IO} $ | — | 0.05 | 0.2 | — | 0.1 | 0.5 | μA |
| Input Offset Voltage | $ V_{IO} $ | — | 1.0 | 5.0 | — | 2.0 | 7.5 | mV |
| Step Response Gain = 100, 5.0% overshoot | t_{THL} | — | 0.8 | — | — | 0.8 | — | μs |
| | t_d | — | 0.38 | — | — | 0.38 | — | μs |
| | dV_O/dt | — | 12 | — | — | 12 | — | $\text{V}/\mu\text{s}$ |
| Step Response Gain = 10, 10% overshoot | t_{THL} | — | 0.6 | — | — | 0.6 | — | μs |
| | t_d | — | 0.34 | — | — | 0.34 | — | μs |
| | dV_O/dt | — | 1.7 | — | — | 1.7 | — | $\text{V}/\mu\text{s}$ |
| Step Response Gain = 1, 5.0% overshoot | t_{THL} | — | 2.2 | — | — | 2.2 | — | μs |
| | t_d | — | 1.3 | — | — | 1.3 | — | μs |
| | dV_O/dt | — | 0.25 | — | — | 0.25 | — | $\text{V}/\mu\text{s}$ |
| Power Supply Current | I_{DCC} | — | 2.7 | 5.5 | — | 2.7 | 6.7 | mAdc |
| | I_{DEE} | — | 2.7 | 5.5 | — | 2.7 | 6.7 | mAdc |
| DC Quiescent Power Dissipation (Power Supply = ± 15 V, $V_O = 0$) | P_D | — | 80 | 165 | — | 80 | 200 | mW |
| Positive Supply Sensitivity (V_{EE} constant) | S^+ | — | 25 | 150 | — | 25 | 200 | $\mu\text{V}/\text{V}$ |
| Negative Supply Sensitivity (V_{CC} constant) | S^- | — | 25 | 150 | — | 25 | 200 | $\mu\text{V}/\text{V}$ |

See current MC1709/1709C data sheet for additional information.

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.



Bump Dia. at Base: 0.006 ± 0.001 in. Bump Height: 0.0040 ± 0.0005 in.
Each bump centerline to be located within 0.001 in. of its true position with respect to any other bump centerline.

PACKAGING AND HANDLING

The popular 1709 type operational amplifier is now available in three chip forms: 1) conventional chips, 2) beam-lead chips and 3) flip-chips, as well as in a variety of plastic and hermetic packages. The flip-chip consists of a silicon chip with solder bumps on the geometry surface to provide easy mechanical mounting and electrical connection. These devices are protected by a thin layer of phosphosilicate passivation which covers the interconnect metalization and active areas of the die. Care must be exercised when removing the dice from the shipping carrier to avoid scratching the solder bumps. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCCF1741 MCCF1741C

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC FLIP-CHIP OPERATIONAL AMPLIFIER

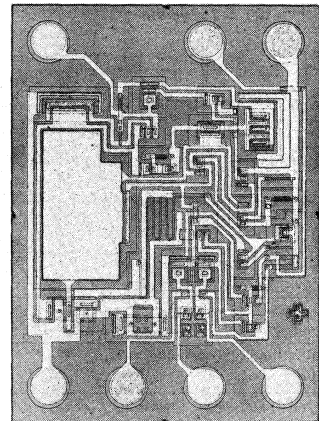
... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MCCF1741 and MCCF1741C employ phosphorsilicate passivation that protects the entire die surface area, including metalization interconnects. The bumps are 90-10 solder on a chrome-copper-gold base. The interconnecting metalization is evaporated aluminum.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER

MONOLITHIC SILICON INTEGRATED CIRCUIT



MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

| Rating | Symbol | Value | | Unit |
|--|----------|-------------|-------------|--------------------|
| | | MCCF1741C | MCCF1741 | |
| Power Supply Voltage | V_{CC} | +18 | +22 | Vdc |
| | V_{EE} | -18 | -22 | |
| Differential Input Signal | V_{ID} | ± 30 | | Volts |
| Common Mode Input Swing (Note 1) | V_{IC} | ± 15 | | Volts |
| Output Short Circuit Duration (Note 2) | t_S | Continuous | | |
| Operating Temperature Range | T_A | 0 to +75 | -55 to +125 | $^{\circ}\text{C}$ |
| Junction Temperature Range | T_J | -65 to +150 | | $^{\circ}\text{C}$ |

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

FIGURE 1 - CIRCUIT SCHEMATIC

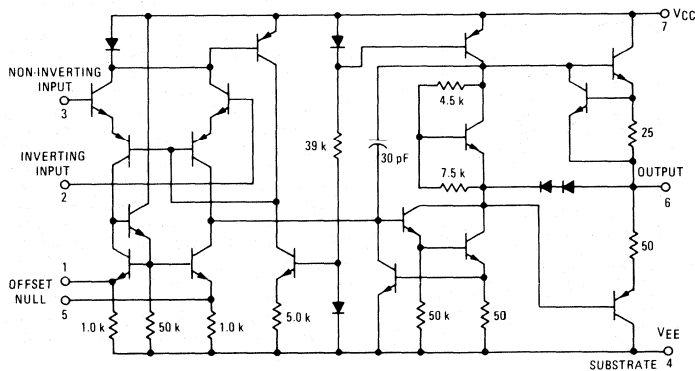
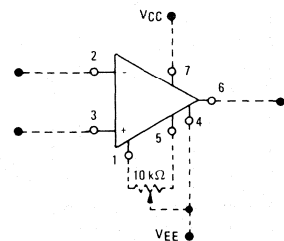


FIGURE 2 - OFFSET ADJUST CIRCUIT



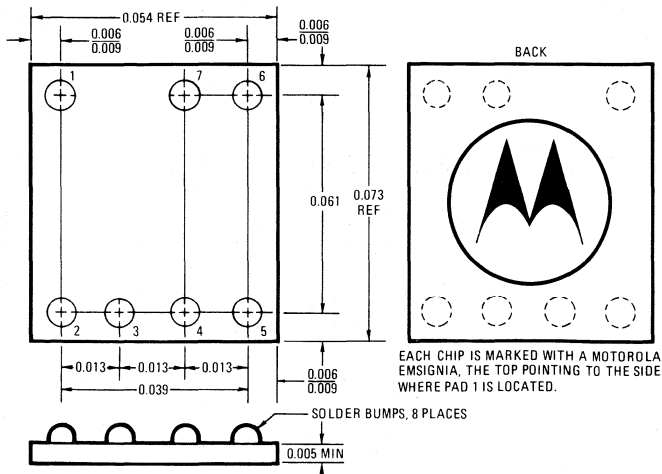
MCCF1741, MCCF1741C (continued)

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = 15 Vdc, T_A = +25°C unless otherwise noted.)

| Characteristic | Symbol | MCCF1741 | | | MCCF1741C | | | Unit |
|---|-----------------------|------------|------------|------|------------|------------|------|-------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Open Loop Voltage Gain (R _L = 2.0 kΩ) (V _O = ±10 V) | A _{vOL} | 50,000 | 200,000 | — | 20,000 | 100,000 | — | — |
| Output Impedance (f = 20 Hz) | z _o | — | 75 | — | — | 75 | — | Ω |
| Input Impedance (f = 20 Hz) | z _{in} | — | 1.0 | — | — | 1.0 | — | MegΩ |
| Output Voltage Swing (R _L = 10 kΩ) (R _L = 2.0 kΩ) | V _O | ±12 ±10 | ±14 ±13 | — | ±12 ±10 | ±14 ±13 | — | V _{peak} |
| Input Common-Mode Voltage Swing | V _{IC} | — | ±13 | — | — | ±13 | — | V _{peak} |
| Common-Mode Rejection Ratio (f = 20 Hz) | CMRR | — | 90 | — | — | 90 | — | dB |
| Input Bias Current | I _{IB} | — | 0.2 | 0.5 | — | 0.2 | 0.5 | μA |
| Input Offset Current | I _{IO} | — | 0.03 | 0.2 | — | 0.03 | 0.2 | μA |
| Input Offset Voltage (R _S = ≤ 10 kΩ) | V _{IO} | — | 1.0 | 5.0 | — | 2.0 | 6.0 | mV |
| Step Response Gain = 100 | t _{THL} | — | 29 | — | — | 29 | — | μs |
| | t _d | — | 8.5 | — | — | 8.5 | — | μs |
| | dV _O /dt ① | — | 1.0 | — | — | 1.0 | — | V/μs |
| | t _{THL} | — | 3.0 | — | — | 3.0 | — | μs |
| | t _d | — | 1.0 | — | — | 1.0 | — | μs |
| | dV _O /dt ① | — | 1.0 | — | — | 1.0 | — | V/μs |
| Gain = 10 | t _{THL} | — | 0.6 | — | — | 0.6 | — | μs |
| | t _d | — | 0.38 | — | — | 0.38 | — | μs |
| | dV _O /dt ① | — | 0.8 | — | — | 0.8 | — | V/μs |
| Power Supply Current | I _{DCC} | — | 1.67 | 2.83 | — | 1.67 | 2.83 | mA |
| | I _{DDEE} | — | 1.67 | 2.83 | — | 1.67 | 2.83 | mA |
| DC Quiescent Power Dissipation (Power Supply = ± 15 V, V _O = 0) | P _D | — | 50 | 85 | — | 50 | 85 | mW |
| Positive Supply Sensitivity (V _{EE} constant) | S ⁺ | — | 30 | 150 | — | 30 | 150 | μV/V |
| Negative Supply Sensitivity (V _{CC} constant) | S ⁻ | — | 30 | 150 | — | 30 | 150 | μV/V |

① dV_O/dt = Slew Rate See current MC1741/1741C data sheet for additional information.
Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

MCCF1741/MCCF1741C BONDING DIAGRAM AND DEVICE DIMENSIONS



Bump Dia. at Base: 0.006 ± 0.001 in. Bump Height: 0.0040 ± 0.0005 in.
Each bump centerline to be located within 0.001 in. of its true position with respect to any other bump centerline.

PACKAGING AND HANDLING

The popular 1741 type operational amplifier is now available in three chip forms: 1) conventional chips, 2) beam-lead chips and 3) flip-chips, as well as in a variety of plastic hermetic packages. The flip-chip consists of a silicon chip with solder bumps on the geometry surface to provide easy mechanical mounting and electrical connection. These devices are protected by a thin layer of phosphorsilicate passivation which covers the interconnect metalization and active areas of the die.

Care must be exercised when removing the dice from the shipping carrier to avoid scratching the solder bumps. A vacuum pickup is useful for the handling of dice. Tweezers are not recommended for this purpose.

The non-spill type shipping carrier consists of a compartmentalized tray and fitted cover. Die are placed in the carrier with geometry side up.

MCH2870MR MCH2870CR

POWER OPERATIONAL AMPLIFIER

... designed as a high-gain internally-compensated hybrid power operational amplifier that can deliver load currents up to ± 300 mA dc typ. This device is ideally suited for driving low impedance loads. Typical applications include buffer, line driver and servo/synchro amplifier or power amplifier with operating characteristics as a function of the external feedback components.

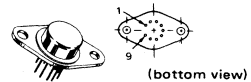
Output current is internally limited to 100 mA (typ) with an option of 200 mA (by shorting pins 2 and 4). With the addition of two external resistors, current can be limited to any value between 100 mA and 300 mA.

The MCH2870MR is specified over the military temperature range (-55°C to $+125^{\circ}\text{C}$) and the MCH2870CR over the commercial temperature range (0°C to $+75^{\circ}\text{C}$).

- High Current Capability to ± 300 mA typ
- Internally Compensated
- High Open-Loop Voltage Gain – 200,000 typ
- Low Open Loop Output Impedance – 10 Ohms typ
- Offset Voltage Null Capability

POWER OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

SILICON
EPITAXIAL PASSIVATED



CASE 614
METAL PACKAGE

TYPICAL APPLICATIONS

FIGURE 1 – POWER OPERATIONAL AMPLIFIER

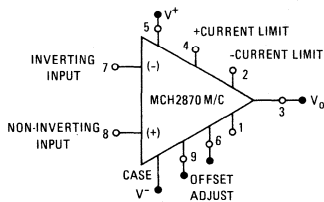


FIGURE 2 – VOLTAGE OFFSET NULL CIRCUIT

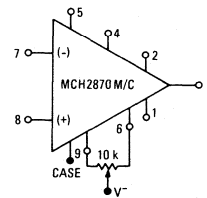


FIGURE 3 – TYPICAL INVERTING AMPLIFIER

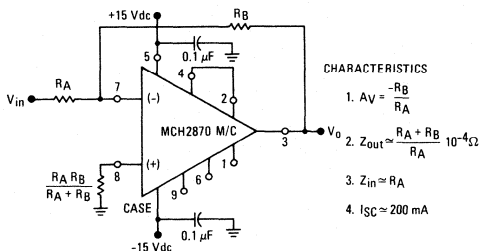
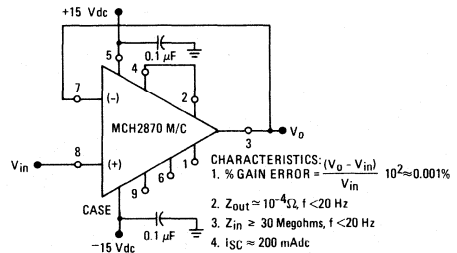


FIGURE 4 – UNITY GAIN VOLTAGE FOLLOWER



See Packaging Information Section for outline dimensions.

MCH2870MR, MCH2870CR (continued)

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

| Rating | Symbol | MCH2870MR | MCH2870CR | Unit |
|---|--|-------------------|------------|------------------------|
| Power Supply Voltage | V ⁺ V ⁻ | +22 -22 | +18 -18 | Vdc |
| Differential Input Signal | V _{in} | ±30 | | Volts |
| Common-Mode Input Swing | CMV _{in} | ±15 | | Volts |
| Output Short Circuit Duration | t _S | Continuous | | |
| Power Dissipation and Thermal Characteristics T _A = +25°C Derate above T _A = +25°C Thermal Resistance, Junction to Air | P _D 1/θ _{JA} θ _{JA} | 2.4 16 62 | | Watts mW/°C °C/W |
| T _C = +25°C Derate above T _C = +25°C Thermal Resistance, Junction to Case | P _D 1/θ _{JC} θ _{JC} | 9.0 60 16.7 | | Watts mW/°C °C/W |
| Operating Temperature Range | T _A | -55 to +125 | 0 to +75 | °C |
| Operating and Storage Junction Temperature Range | T _J , T _{stg} | -65 to +175 | | °C |

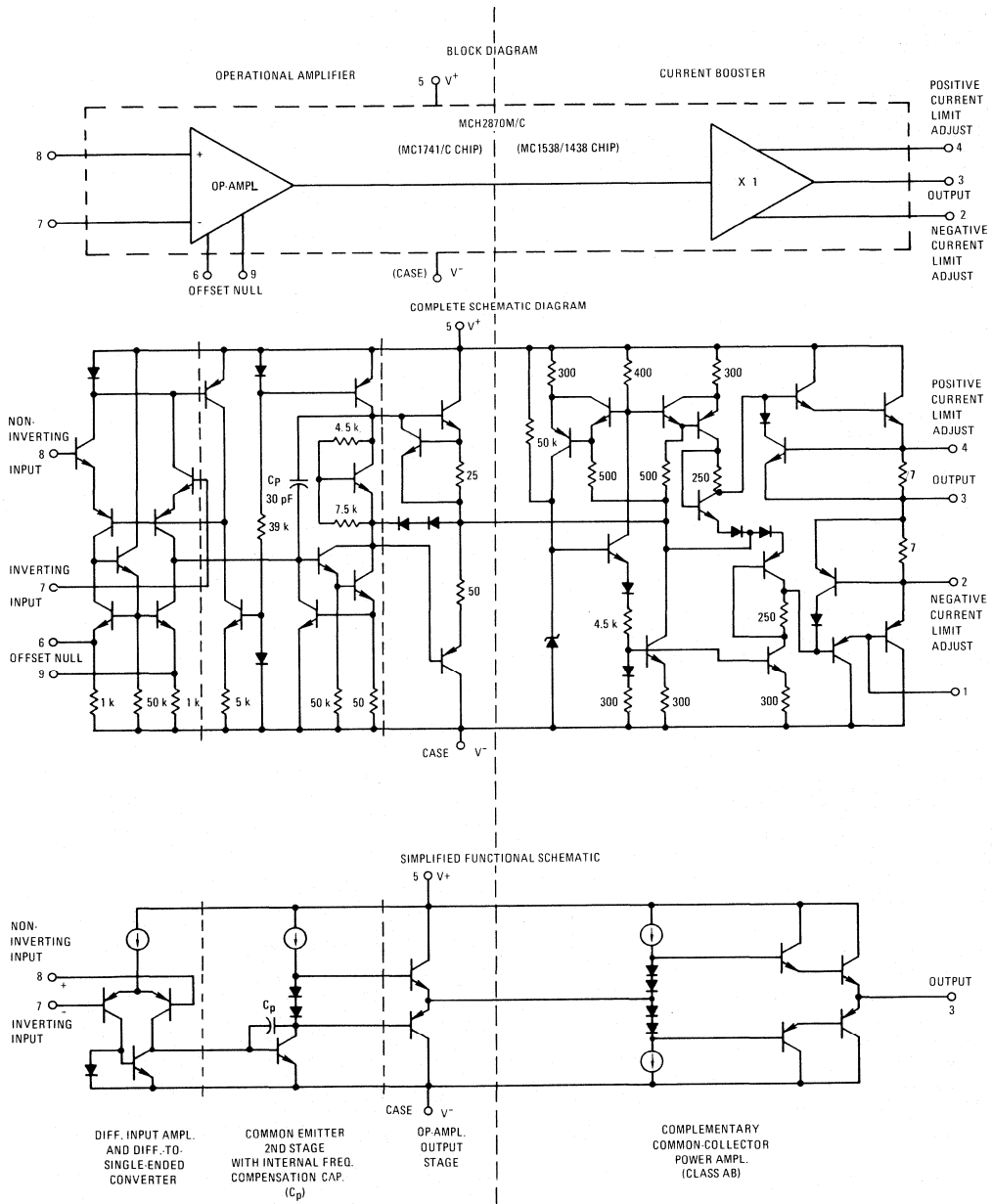
ELECTRICAL CHARACTERISTICS (V⁺ = +15 Vdc, V⁻ = -15 Vdc, T_C = +25°C unless otherwise noted)

| Characteristics | Symbol | MCH2870MR | | | MCH2870CR | | | Unit |
|--|--|------------------|---------|-----|------------------|---------|------|------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current T _C = +25°C T _C = T _{low} to T _{high} (See Note 1) | I _b | — | 0.2 | 0.5 | — | 0.2 | 0.5 | μAdc |
| Input Offset Current T _C = +25°C T _C = T _{low} to T _{high} | I _{io} | — | 0.03 | 0.2 | — | 0.03 | 0.2 | μAdc |
| Input Offset Voltage (R _S ≤ 10 kΩ) T _C = +25°C T _C = T _{low} to T _{high} | V _{io} | — | 1.0 | 5.0 | — | 2.0 | 6.0 | mVdc |
| Differential Input Impedance (Open-Loop, f = 20 Hz) Parallel Input Resistance Parallel Input Capacitance | R _p C _p | 0.3 | 1.0 | — | 0.3 | 1.0 | — | Megohm pF |
| Common-Mode Input Impedance (f = 20 Hz) | Z _{in} | — | 200 | — | — | 200 | — | Megohms |
| Common-Mode Input Voltage Swing | CMV _{in} | ±12 | ±13 | — | ±12 | ±13 | — | V _{pk} |
| Equivalent Input Noise Voltage A _V = 100, R _S = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz | e _n | — | 45 | — | — | 45 | — | nV/(Hz) ^{1/2} |
| Common-Mode Rejection Ratio (f = 100 Hz) | CM _{rej} | 70 | 90 | — | 70 | 90 | — | dB |
| DC Open-Loop Voltage Gain, (V _{out} = ±10 V, R _L = 300 ohms) T _C = +25°C T _C = T _{low} to T _{high} | A _{VOL} | 50,000 25,000 | 200,000 | — | 20,000 15,000 | 100,000 | — | V/V |
| Power Bandwidth A _V = 1, R _L = 300 ohms, THD ≤ 5%, V _{out} = 20 V _{p-p} | P _{BW} | — | 12 | — | — | 12 | — | kHz |
| Unity Gain Crossover Frequency (open-loop) | | — | 1.1 | — | — | 1.1 | — | MHz |
| Phase Margin (closed loop, unity gain) | | — | 65 | — | — | 65 | — | degrees |
| Gain Margin (closed loop, unity gain) | | — | 11 | — | — | 11 | — | dB |
| Slew Rate (Unity Gain) | dV _{out} /dt | — | 0.8 | — | — | 0.8 | — | V/μs |
| Output Impedance (open loop f = 20 Hz) | Z _{out} | — | 10 | — | — | 10 | — | ohms |
| Short-Circuit Output Current (See Figure 6) R ₁ = R ₂ = ∞ Pins 2 and 4 shorted Adjustable Range | I _{SC} | 75 | 100 | 125 | 65 | 100 | 140 | mAdc |
| Output Voltage Swing R _L = 300 ohms R _L = 300 ohm (T _C = T _{low} to T _{high}) | V _{out} | ±12 ±10 | ±13 | — | ±11 ±10 | ±12 | — | V _{pk} |
| Power Supply Sensitivity (dc) V ⁻ = constant, R _S ≤ 10 k ohms V ⁺ = constant, R _S ≤ 10 k ohms | S ⁺ S ⁻ | — | 30 | 150 | — | 30 | 200 | μV/V |
| Power Supply Current | I _D ⁺ I _D ⁻ | — | 7.7 | 13 | — | 7.7 | 16.5 | mAdc |
| DC Quiescent Power Dissipation V _{in} = 0 | P _D | — | 225 | 390 | — | 225 | 500 | mW |

Note 1: T_{low}: 0°C for MCH2870CR
 -55°C for MCH2870MR
 T_{high}: +75°C for MCH2870CR
 +125°C for MCH2870MR

MCH2870MR, MCH2870CR (continued)

FIGURE 5 – MCH2870M/C DEVICE CONFIGURATION



MCH2870MR, MCH2870CR (continued)

TYPICAL CHARACTERISTICS

($V^+ = +15\text{ Vdc}$, $V^- = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 6 – SHORT-CIRCUIT CURRENT versus R1 OR R2 (100 mA TO 300 mA)

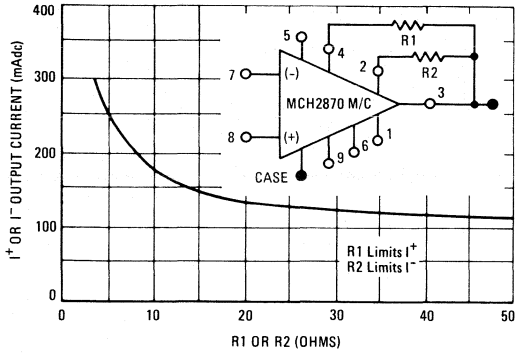


FIGURE 7 – DC SAFE OPERATING AREA

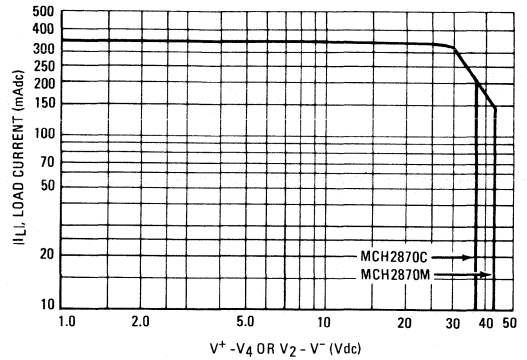


FIGURE 8 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

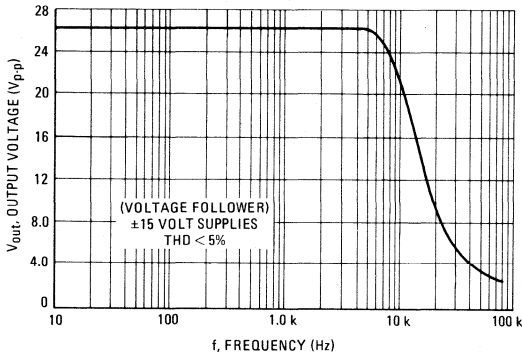


FIGURE 9 – OPEN LOOP FREQUENCY RESPONSE

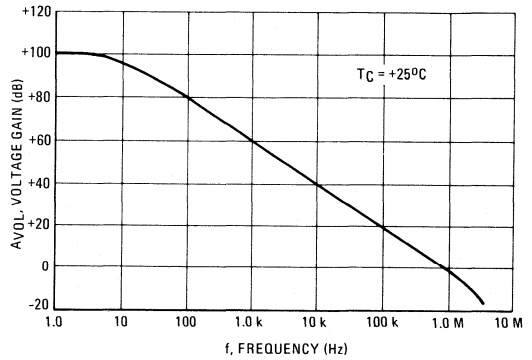


FIGURE 10 – OUTPUT NOISE versus SOURCE RESISTANCE

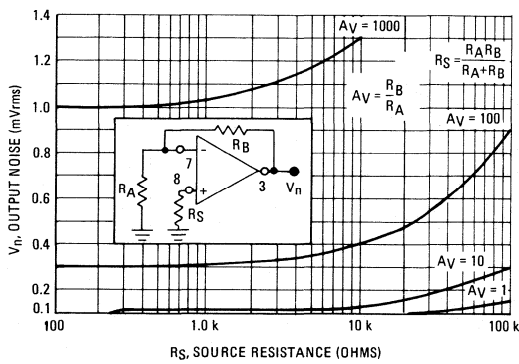
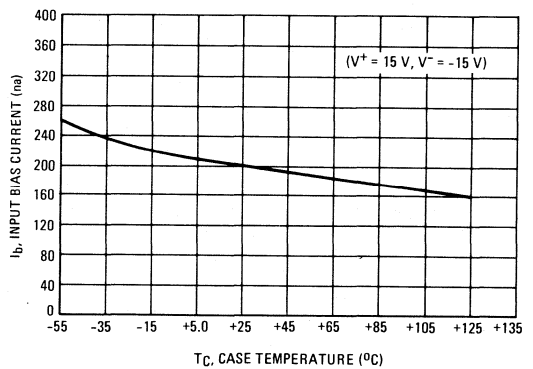


FIGURE 11 – INPUT BIAS CURRENT versus TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 12 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

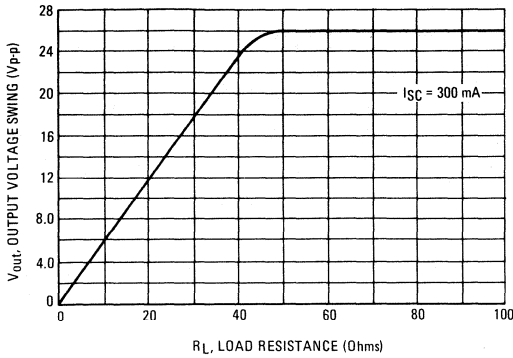
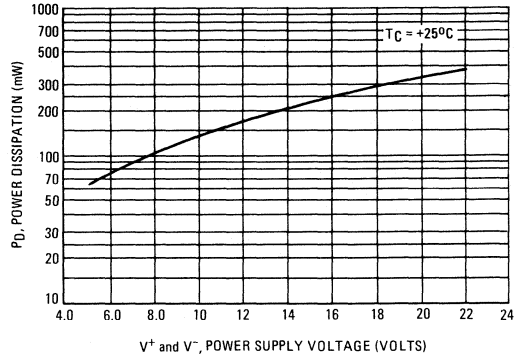


FIGURE 13 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



TYPICAL APPLICATIONS

FIGURE 14 – PROGRAMMABLE VOLTAGE SOURCE

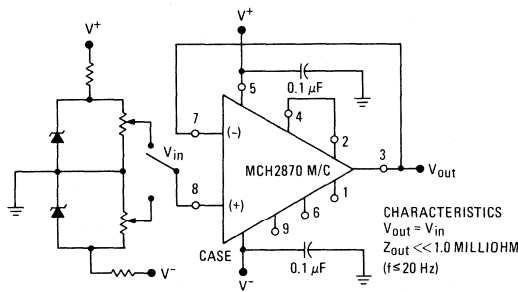


FIGURE 15 – CONSTANT CURRENT SOURCE OR TRANSCONDUCTANCE AMPLIFIER

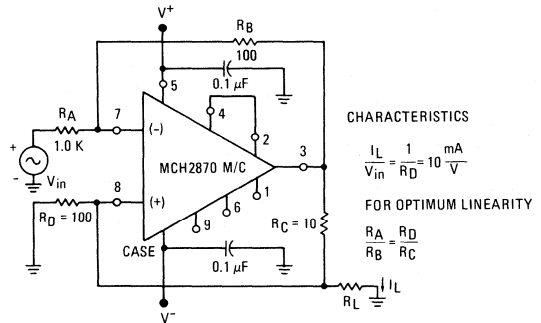


FIGURE 16 – POWER SUPPLY SPLITTER

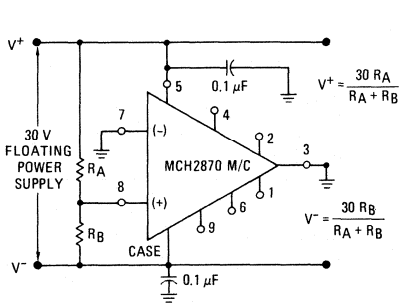
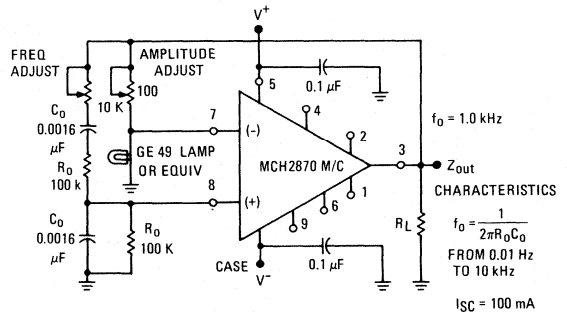


FIGURE 17 – WIEN BRIDGE OSCILLATOR



MCH2890R

DUAL POWER DRIVER

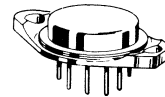
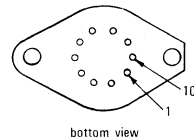
HYBRID DUAL POWER DRIVER

The MCH2890 Dual Power Driver is capable of driving a wide variety of inductive and resistive loads; included are hammer solenoids in high-speed digital printers, relays, lamps, paper-tape punches, and stepper motors in computer-operated plotters.

- High Current – to 6.0 Amperes
- High Breakdown Voltage – $BV_{CEX} = 120$ Volts min
- M TTL Compatibility
- Separate Integrated Circuit and Darlington Power Grounds
- Low V_{sat} at 3.0 and 6.0 Amperes
- Low Leakage Current – $0.1 \mu A$ typ

DUAL POWER DRIVER

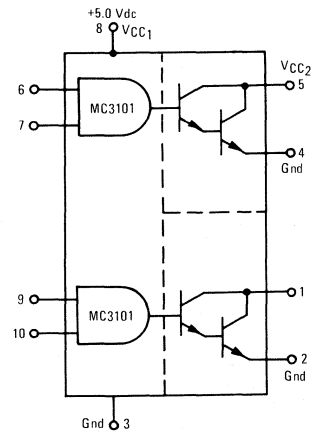
HYBRID SILICON INTEGRATED CIRCUIT



CASE 685
METAL PACKAGE

MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise noted)

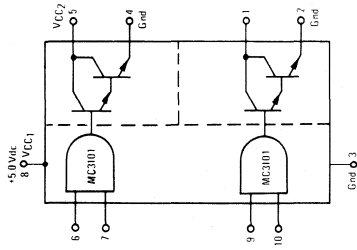
| Rating | Symbol | Value | Unit |
|---|---------------------------|-------------|----------------|
| Collector Current | I_C | 8.0 | A |
| | | 1.0 | |
| Collector Emitter Breakdown Voltage Minimum at $I_C \leq 0.5$ mA | BV_{CEX} (pins 1, 5) | 120 | Vdc |
| Power Supply Voltage (Integrated Circuit) | V_{CC1} | 7.0 | Vdc |
| Power Dissipation and Thermal Characteristics $T_A = 25^\circ C$ | P_D | 3.75 | Watts |
| Derate above $T_A = 25^\circ C$ | $1/\theta_{JA}$ | 25 | mW/ $^\circ C$ |
| Thermal Resistance, Junction to Air | θ_{JA} | 40 | $^\circ C/W$ |
| $T_C = 25^\circ C$ | P_D | 25 | Watts |
| Derate above $T_C = 25^\circ C$ | $1/\theta_{JC}$ | 167 | mW/ $^\circ C$ |
| Thermal Resistance, Junction to Case | θ_{JC} | 6.0 | $^\circ C/W$ |
| Operating Temperature Range | T_A | 0 to +70 | $^\circ C$ |
| Storage Temperature Range | T_{stg} | -55 to +175 | $^\circ C$ |



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one power driver. The other power driver is tested in the same manner.



TEST CURRENT/VOLTAGE VALUES

| Characteristics | Symbol | Pin Under Test | TEST LIMITS | | | | | | | | | | TEST CURRENT/VOLTAGE VALUES | | | | | | | | | | | | |
|-------------------------------------|-----------------------|----------------|-------------|------|-------|-----|------------|-----|------|------|---------|------|-----------------------------|----|---------|-------|-----|-----|-----|------|------|-------|-------------|-------------------------|-------|
| | | | 0°C | | +25°C | | +75°C | | Unit | | AMPERES | | | | | VOLTS | | | | | | | | | |
| | | | Min | Max | Min | Typ | Max | Min | Max | Unit | IOL1 | IOL2 | Iin | ID | IC(max) | VIH | VIL | VF | VR | VCC1 | VCC2 | VCCIL | VCCIH | VRRH | |
| Input Forward Current | IF | 6 | - | -2.0 | - | - | -2.0 | - | -2.0 | mAdc | - | - | - | - | - | - | - | - | 5.0 | - | 4.5 | 5.5 | 4.0 | | |
| Input Leakage Current | IR | 6 | - | 50 | - | - | 50 | - | 50 | µAdc | - | - | - | - | - | - | - | 2.4 | 5.0 | 90 | 4.5 | 5.5 | 4.0 | | |
| Input Breakdown Voltage | BVin | 6 | - | 5.5 | - | - | - | - | - | Vdc | 6 | - | - | - | - | - | - | - | 5.0 | - | 4.5 | 5.5 | 4.0 | | |
| Input Clamp Voltage | VD | 6 | - | - | - | - | -1.5 | - | - | Vdc | - | 6 | - | - | - | - | - | - | - | - | 8 | - | - | 2.3.4 | |
| Output Voltage (See Figure 1) | VOL1 VOL2 BVCEX | 5 5 5 | - | - | - | - | 1.5 2.5 | - | - | Vdc | 6 | - | - | - | - | - | - | - | - | - | - | - | 7 7 7 | 2.3.4 2.3.4 2.3.4 | |
| Output Leakage Current | ICEX | 5 | - | - | - | - | 0.1 | - | - | µAdc | - | - | - | - | 6 | - | - | - | - | - | 5 | - | - | 7 | 2.3.4 |
| Output Power Supply Drain Current | IPDL | 8 | - | - | - | - | 30 | - | - | mAdc | - | - | - | - | - | - | - | - | 8 | - | - | - | - | 2.3.4.6 7.9.10 | |
| Output Power Supply Drain Current | IPDH | 8 | - | - | - | - | 120 | - | - | mAdc | - | - | - | - | - | - | - | - | 8 | - | - | - | - | 6.7.9. 10 | 2.3.4 |
| Switching Parameters (See Figure 2) | t _{pd-} | 5.6 | - | - | - | - | 0.26 | - | - | µs | - | - | - | - | - | - | - | - | 8 | 5 | - | - | - | 7 | 2.3.4 |
| Turn-Off Delay Time | t _{pd+} | 5.6 | - | - | - | - | 1.8 | - | - | µs | 6 | 5 | - | - | - | - | - | - | 8 | 5 | - | - | - | 7 | 2.3.4 |



TEST CIRCUITS

FIGURE 1 - V_{OL} TEST CIRCUIT

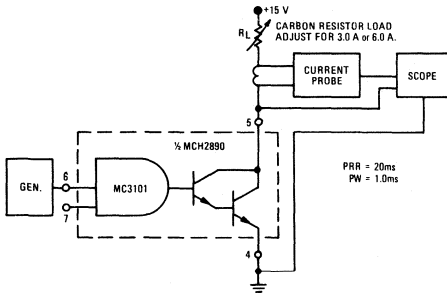
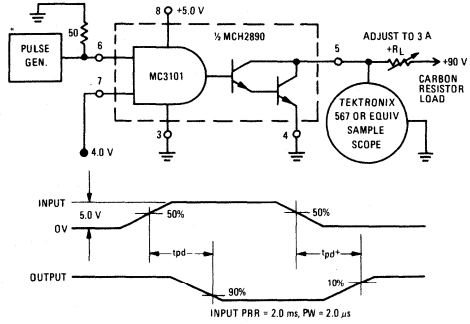


FIGURE 2 - PROPAGATION DELAY TIME TEST CIRCUIT



TYPICAL CHARACTERISTICS

FIGURE 3 - COLLECTOR-EMITTER VOLTAGE versus NEGATIVE EMITTER VOLTAGE

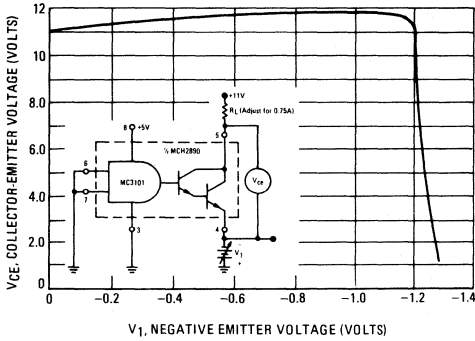
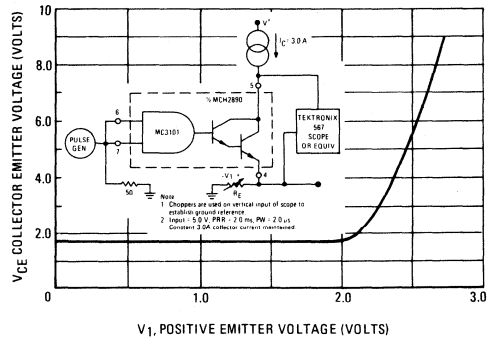


FIGURE 4 - COLLECTOR-EMITTER VOLTAGE versus POSITIVE EMITTER VOLTAGE



SAFE OPERATING AREA

FIGURE 5 - COLLECTOR-EMITTER VOLTAGE versus COLLECTOR CURRENT

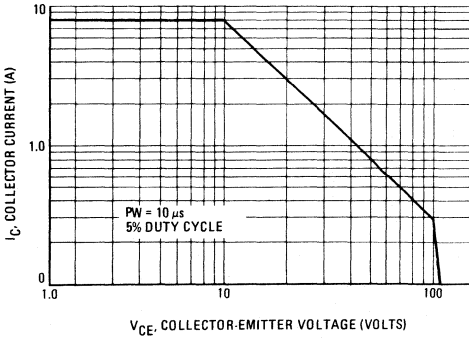
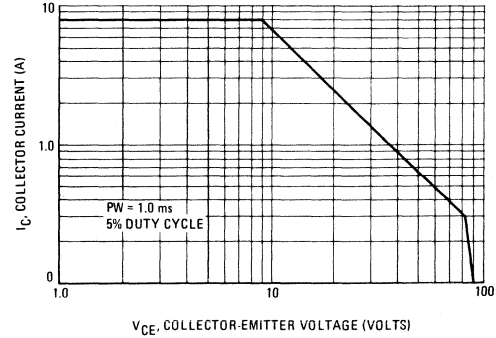
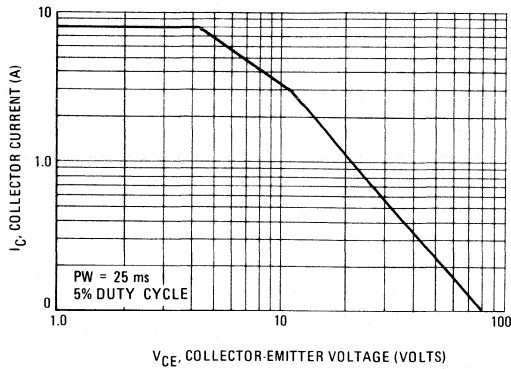


FIGURE 6 - COLLECTOR-EMITTER VOLTAGE versus COLLECTOR CURRENT



SAFE OPERATING AREA (Continued)

FIGURE 7 – COLLECTOR-EMITTER VOLTAGE versus COLLECTOR CURRENT



APPLICATIONS INFORMATION

The MCH2890 is designed for high-current and high-voltage applications such as hammer-drivers in high-speed printers, relay drivers, lamp drivers, paper tape punches, stepping motors, and other high current inductive and resistive loads.

This dual hybrid driver, which consists of a monolithic MTTL "AND" gate and two power Darlingtons, is capable of supplying up to 6.0 amperes at a maximum duty cycle of 10% with pulse widths up to 25 ms. In addition to the high-current drive capability the MCH2890 offers high collector-to-emitter breakdown ($BV_{CEX} = 120$ Volts min) which is desirable when driving inductive loads at high currents.

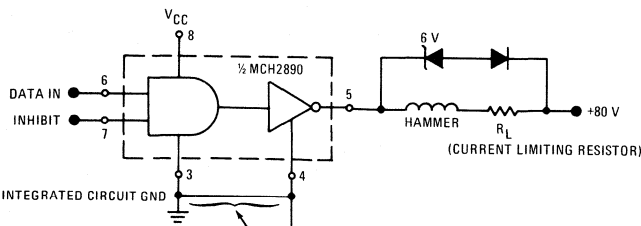
A typical high-speed hammer driver application is illustrated in Figure 8. The number of drivers per printer is large, and considerable electrical noise is generated when they are switched simultaneously. The ground line, which terminates all of the Darlingtons power drivers, may be several feet in length resulting in substantial inductance and series resistance. The effect of this inductance and resistance becomes appreciable at the high-current

levels required of hammer drivers. When the Darlington power drivers are switched "off", even a small inductance at the Darlington ground generates a negative voltage spike which tends to turn the Darlington power driver "on" rather than "off". This negative excursion of the emitter can result in oscillations. The oscillation can be stopped by tying the integrated circuit ground (pin 3) to the Darlington ground (pins 2 and 4) with as short a line as possible. (See Figure 8). This circuit configuration pulls the gate output lower when the negative spike is present on the power ground line which guarantees "turn off" of the Darlington power driver.

To insure that the Darlington power driver does not go into secondary breakdown and latch up, a diode clamp is employed as shown. For high-speed printers, the addition of a zener diode can aid in dissipating the stored inductive power (during "turn off") in the hammer solenoid.

Additional features of the MCH2890 include fast switching and low leakage for minimum standby power.

FIGURE 8 – TYPICAL HAMMER DRIVER APPLICATION



The Darlington power driver ground should be connected to the integrated circuit ground with a short line.

MFC4000B

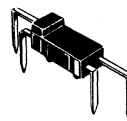
AUDIO AMPLIFIER

1/4-WATT AUDIO AMPLIFIER

... designed for the output stage of battery-powered portable radios.

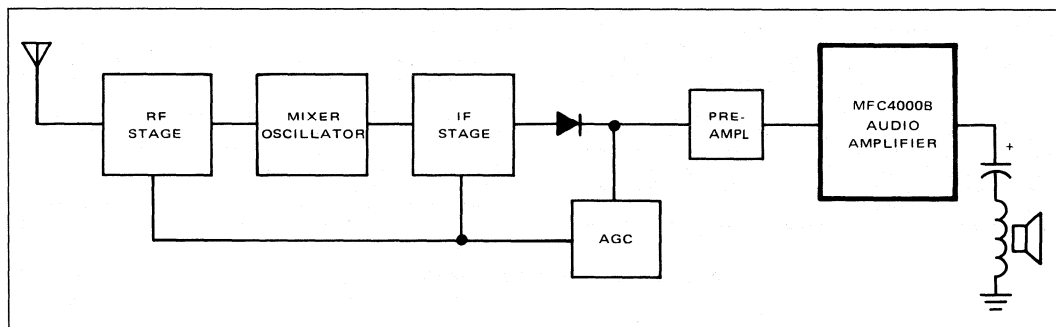
- 250 mW of Audio Output Power
- Low Standby Current – 3.5 mA typical
- Low Harmonic Distortion
- Reduces Component Count in Portable Radios by Two Transformers and Two Transistors
- Eliminates Costly Component Matching Requirements

1/4-WATT AUDIO AMPLIFIER SILICON MONOLITHIC FUNCTIONAL CIRCUIT



PLASTIC PACKAGE
CASE 206A

TYPICAL APPLICATION



7

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|--------|------------|------------------|
| Power Supply Voltage | V^+ | 12 | Vdc |
| Power Dissipation (Package Limitation) (Soldered on a circuit board and held in free air) Derate above $T_A = 25^\circ\text{C}$ | P_D | 1.0 | Watt |
| Operating Temperature Range | T_A | -10 to +75 | $^\circ\text{C}$ |

See Packaging Information Section for outline dimensions.

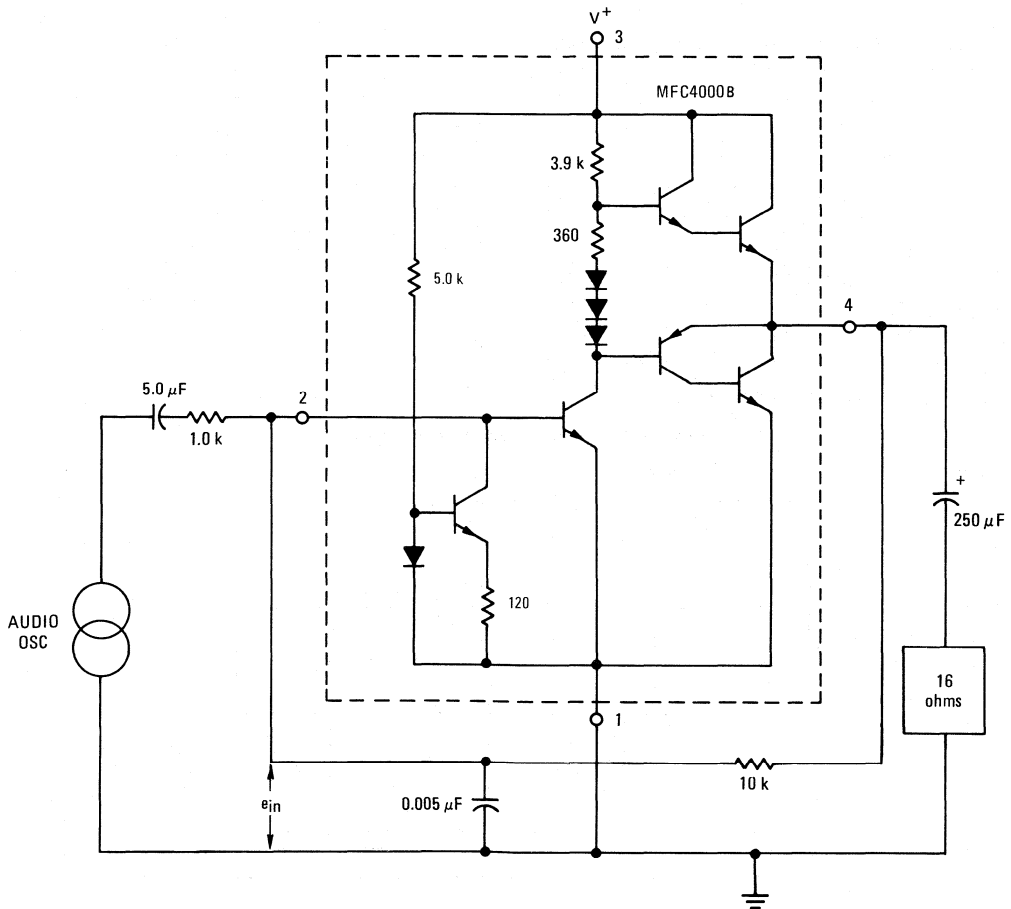
MFC4000B (continued)

ELECTRICAL CHARACTERISTICS* ($V^+ = 9.0$ Vdc, $R_L = 16$ Ohms, $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-----------|-----|------------|-----|---------|
| Zero Signal Current Drain | I_D | — | 3.5 | 6.0 | mAdc |
| Sensitivity $P_{out} = 50$ mW(rms) | e_{in} | — | — | 15 | mV(rms) |
| Output Power Total Harmonic Distortion $\leq 10\%$ | P_{out} | 250 | 350 | — | mW(rms) |
| Total Harmonic Distortion $P_{out} = 50$ mW(rms) $P_{out} = 50$ mW(rms), $V^+ = 6.0$ Vdc | THD | — | 0.7 4.5 | — | % |

*As measured in test circuit shown in Figure 1.

FIGURE 1 – TEST CIRCUIT



TOTAL HARMONIC DISTORTION versus OUTPUT POWER

FIGURE 2 – $V^+ = 9.0$ Vdc

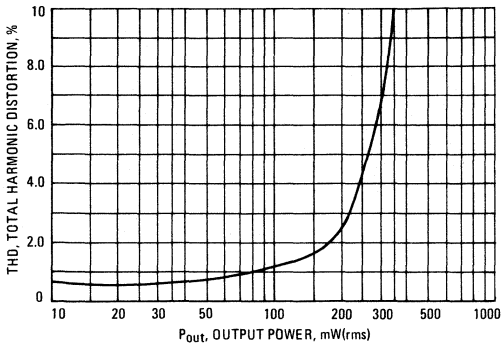


FIGURE 3 – $V^+ = 6.0$ Vdc

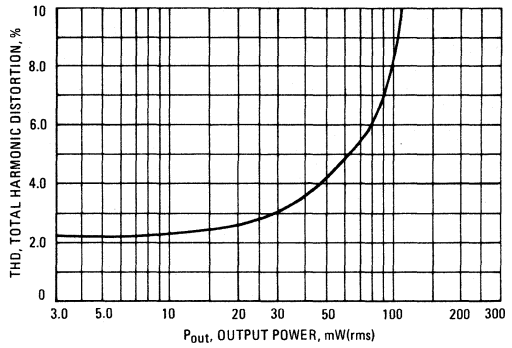


FIGURE 4 – CURRENT DRAIN versus OUTPUT POWER

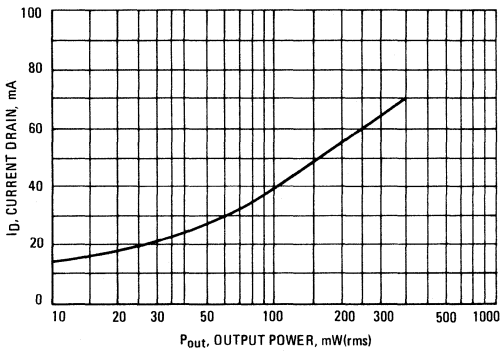


FIGURE 5 – TOTAL HARMONIC DISTORTION versus SUPPLY VOLTAGE

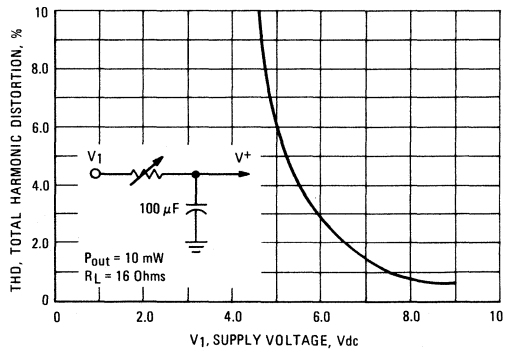
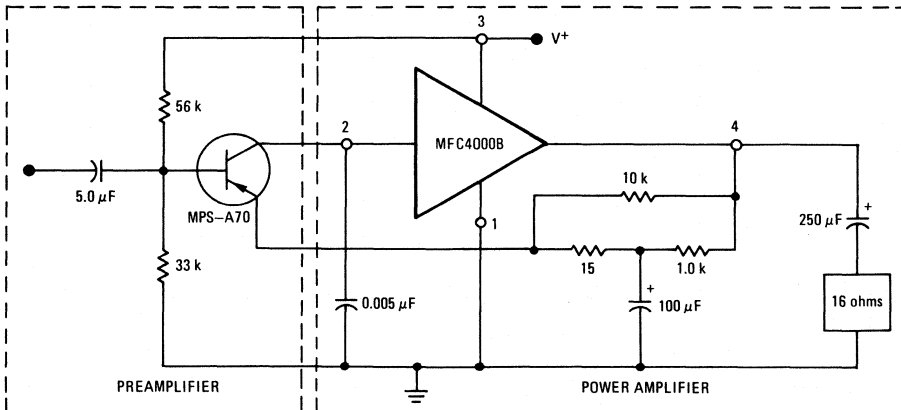


FIGURE 6 – TYPICAL CIRCUIT APPLICATION



MFC4010A

HIGH FREQUENCY CIRCUIT

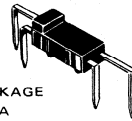
WIDE-BAND AMPLIFIER

... designed for FM/IF and low-level audio applications.

- High Audio Gain – 60 dB minimum
- Useful as a Microphone Amplifier and in Tape Recorders and Cassettes
- Excellent Performance as a 10.7 MHz FM/IF Amplifier
- High Transconductance (g_m) Ideally Suited to Low Impedance Ceramic Filters

WIDE-BAND AMPLIFIER

Silicon Monolithic
Functional Circuit



PLASTIC PACKAGE
CASE 206A

TYPICAL APPLICATIONS

FIGURE 1 – FM/IF AMPLIFIER

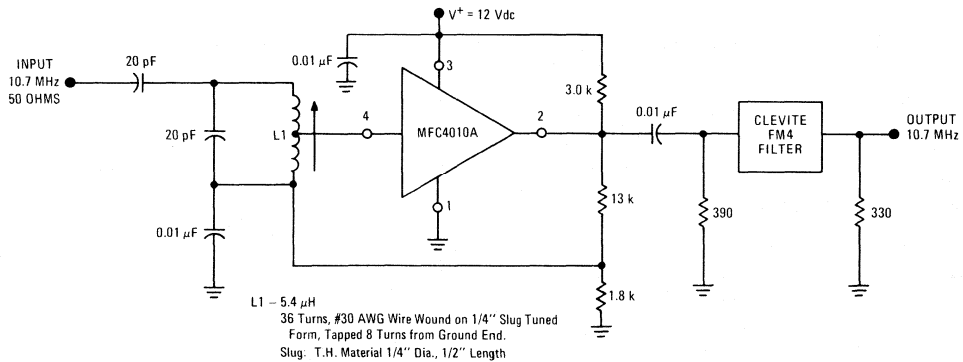
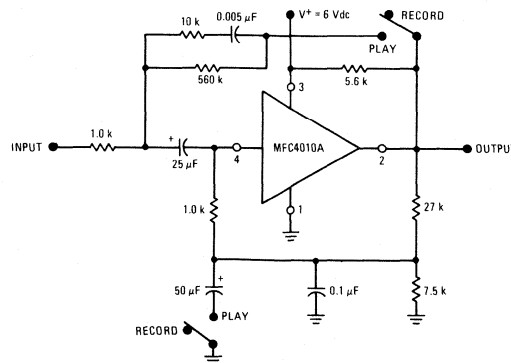


FIGURE 2 – RECORD/PLAY PREAMPLIFIER FOR CASSETTE AND PORTABLE TAPE RECORDERS



MFC4010A (continued)

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|--------|------------|----------------------|
| Power Supply Voltage | V^+ | 18 | Vdc |
| Power Dissipation @ $T_A = 25^\circ\text{C}$ (Package Limitation) Derate above 25°C | P_D | 0.5 | Watt |
| | | 5.0 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -10 to +75 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS ($V^+ = 6.0\text{ Vdc}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|--------------|-----|-----------|-----|---------|
| Open Loop Voltage Gain (Figure 3) ($f = 1.0\text{ kHz}$) | AVOL | 60 | 68 | — | dB |
| h Parameters (1) ($f = 1.0\text{ kHz}$) | h_{11} | — | 1.0 | — | k ohms |
| | h_{12} | — | 10^{-6} | — | — |
| | h_{21} | — | 1000 | — | — |
| | h_{22} | — | 10^{-5} | — | mhos |
| Output Noise Voltage (Figure 3) (BW = 20 Hz to 20 kHz, $R_S = 1.0\text{ k ohms}$) | $e_{n(out)}$ | — | 3.0 | — | mV(rms) |
| Current Drain | I_D | — | 3.0 | — | mA |

HIGH FREQUENCY CHARACTERISTICS ($V^+ = 12\text{ Vdc}$, $f = 10.7\text{ MHz}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

| | | | | | |
|--|----------|---|-----------------|---|------------------|
| Power Gain (Figure 1) ($e_{in} = 0.1\text{ mVrms}$) | — | — | 42 | — | dB |
| Noise Figure (Figure 1) ($R_S \approx 740\text{ Ohms}$) | NF | — | 6.0 | — | dB |
| y Parameters(1) ($f = 10.7\text{ MHz}$, $I_2 = 2.0\text{ mA}$) | Y_{11} | — | $1.3 + j1.5$ | — | mmhos |
| | Y_{12} | — | $-3.4 + j8.1$ | — | μmhos |
| | Y_{21} | — | $-0.33 + j0.68$ | — | mhos |
| | Y_{22} | — | $120 + j0$ | — | μmhos |

(1) Device only, without external passive components.

FIGURE 3 – AUDIO TEST CIRCUIT

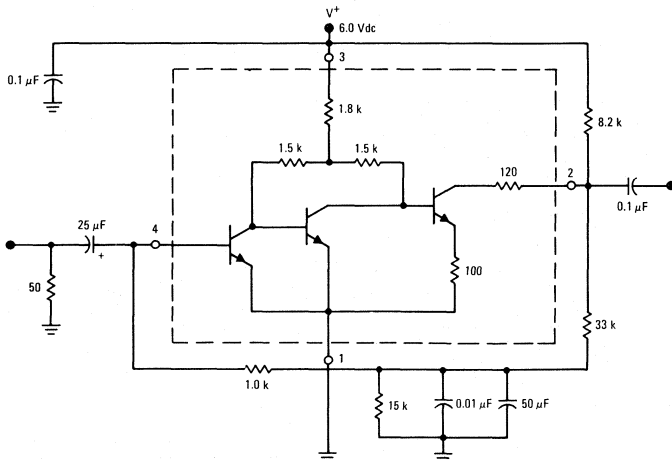
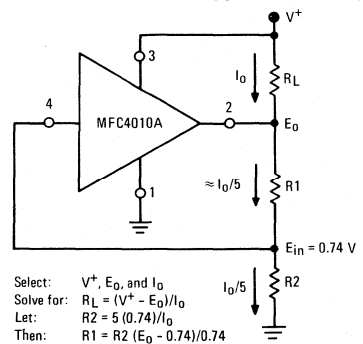


FIGURE 4 – BIASING RECOMMENDATIONS



AUDIO PERFORMANCE CHARACTERISTICS
(for Test Circuit Figure 3)

FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

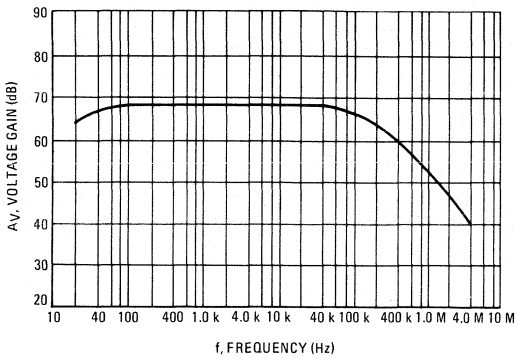
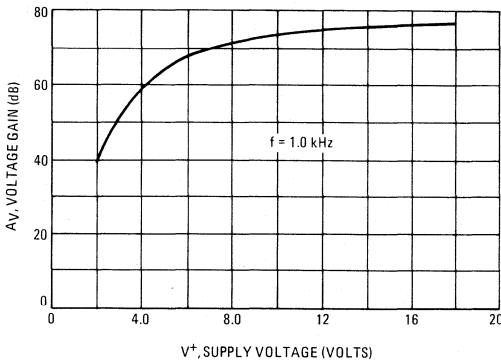


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY



TAPE PREAMPLIFIER PERFORMANCE
(for Circuit Figure 2)

FIGURE 7 – RECORD VOLTAGE GAIN versus FREQUENCY

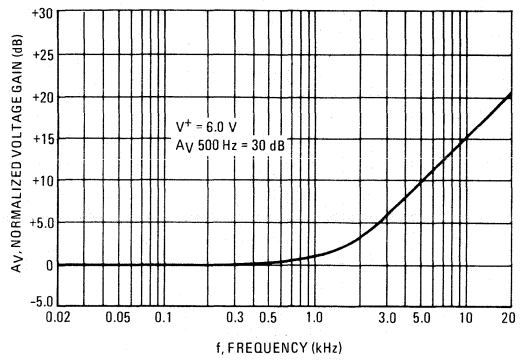
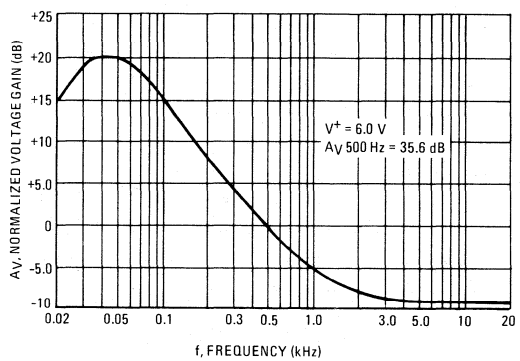


FIGURE 8 – PLAYBACK VOLTAGE GAIN versus FREQUENCY



Note:

The record/playback characteristics shown in Figures 8 and 9 were taken with the preamplifier driven by a 50 ohm source. The curves are typical of a desired response for the preamplifier; however, every type of tape recording and playback head is different and this circuit will not necessarily satisfy all requirements. No particular tape head was used as a basis for circuit design. The circuit is only an example showing the equalization network configuration.

The ideal preamplifier will have an input impedance approximately 10 times the highest impedance of the tape head and every preamplifier circuit must be designed using a test tape to verify the response of the design.

10.7 MHz y PARAMETERS

FIGURE 9 – INPUT ADMITTANCE

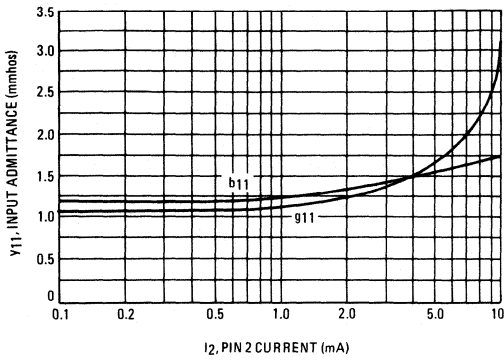


FIGURE 10 – REVERSE TRANSFER ADMITTANCE

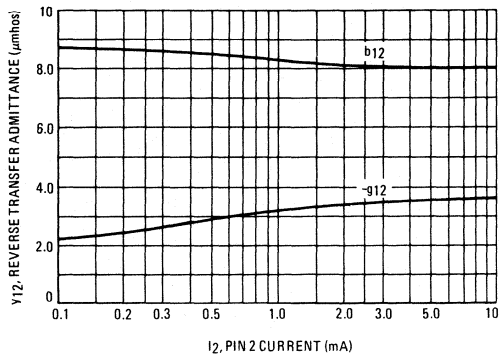


FIGURE 11 – FORWARD TRANSFER ADMITTANCE

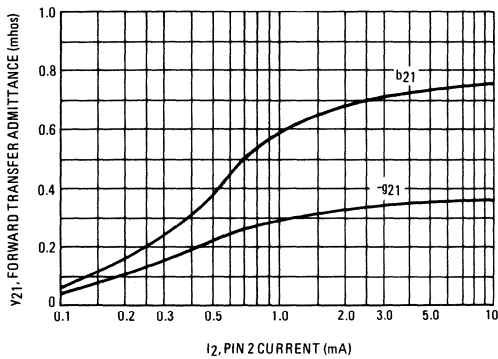
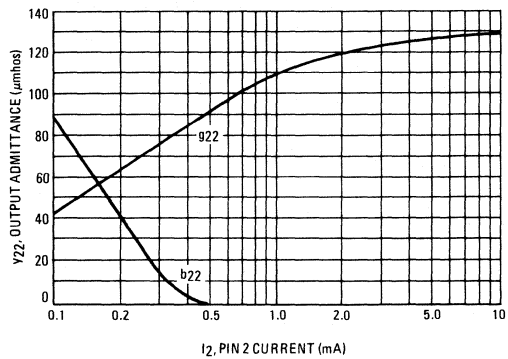


FIGURE 12 – OUTPUT ADMITTANCE



10.7 MHz PERFORMANCE
(Circuit of Figure 1)

FIGURE 13 – POWER GAIN versus SUPPLY VOLTAGE

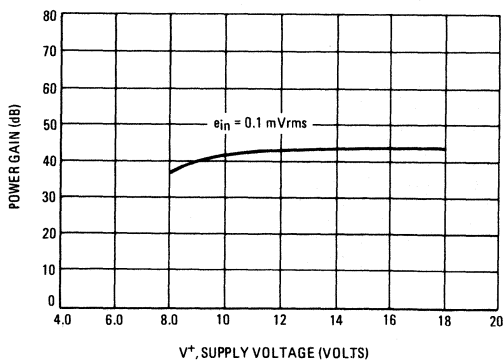
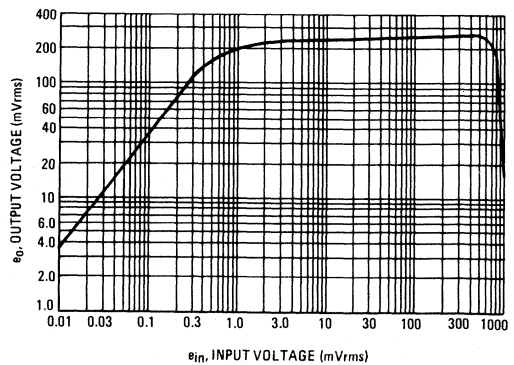


FIGURE 14 – VOLTAGE TRANSFER CHARACTERISTIC



MFC4040

SINGLE TOGGLE FLIP-FLOP

SINGLE TOGGLE FLIP-FLOP

- Wide Operating Voltage Range – 4.0 to 16 Volts
- Regulated Supply Not Required
- Compatible with TTL and DTL
- Economical 4-Lead Plastic Package

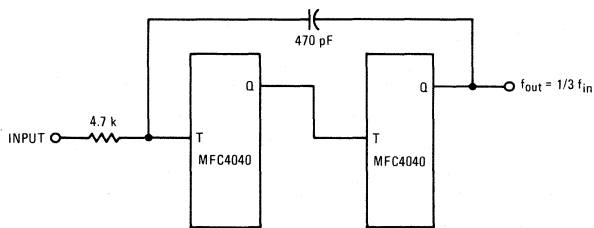
SINGLE TOGGLE FLIP-FLOP

Single Monolithic
Functional Circuit

MAXIMUM RATINGS

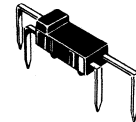
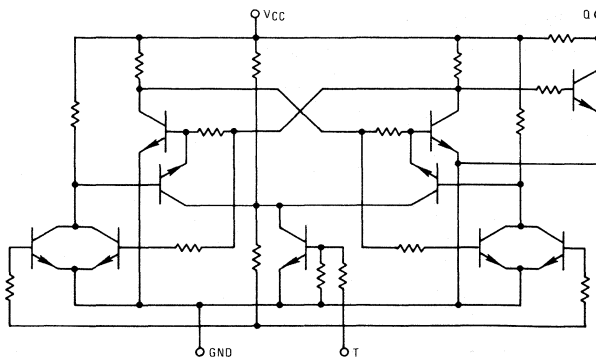
| Rating | Symbol | Value | Volts |
|---|--------------------------|------------|------------------------|
| Power Supply Voltage | V_{CC} | 19 | Vdc |
| Output Sinking Current | I_{sink} | 10 | mA |
| Negative Input Voltage | V_{in} | 0.5 | Vdc |
| Power Dissipation @ $T_A = 25^\circ C$ Derate above $25^\circ C$ | P_D $1/\theta_{JA}$ | 1.0 10 | Watt mW/ $^\circ C$ |
| Operating Temperature Range | T_A | -10 to +75 | $^\circ C$ |

TYPICAL APPLICATION



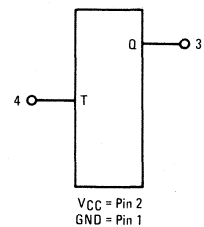
Divide-by-3 Circuit

FIGURE 1 – CIRCUIT SCHEMATIC



CASE 206A
PLASTIC

BLOCK DIAGRAM



See Packaging Information Section for outline dimensions.

MFC4040 (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = 12$ Vdc, $V_{in} = 4.0$ Vp-p Square Pulse, $f = 10$ kHz, 50% Duty Cycle, $t_f = 1.0$ V/ μ s (Min), $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------|-------------|--------|------------|-----------|
| Operating Power Supply Voltage | V_{CC} | 4.0 | — | 16 | Vdc |
| Toggle Frequency | f_{Tog} | — | 3.0 | — | MHz |
| Output Voltage (High) ($V_{CC} = 4.0$ Vdc) ($V_{CC} = 16$ Vdc) | V_{OH} | 3.5 15.5 | — — | — — | Vdc |
| Output Voltage (Low) ($V_{CC} = 4.0$ Vdc) ($V_{CC} = 16$ Vdc) | V_{OL} | — — | — — | 0.5 1.0 | Vdc |
| Operating Drain Current | I_D | — | — | 32 | mAdc |
| Output Sinking Current ($V_O \leq 1.0$ Vdc) | I_{sink} | — | 2.0 | — | mAdc |
| Rise Time | t_r | — | 250 | — | ns |
| Storage Time | t_s | — | 350 | — | ns |
| Fall Time | t_f | — | 60 | — | ns |
| Input Resistance | R_{in} | 10 | — | — | $k\Omega$ |
| Output Resistance (Output High) | R_{OH} | — | — | 2.8 | $k\Omega$ |

INPUT PULSE REQUIREMENTS

| Characteristic | Symbol | Min | Max | Unit |
|-----------------|-----------------|------|------|------------------------------------|
| Pulse Magnitude | V_H | +4.0 | — | Volts |
| Zero Level | V_L | — | +1.0 | Volts |
| Leading Edge | No Requirement | | | |
| Trailing Edge | $\frac{dv}{dt}$ | -1.0 | — | $\frac{\text{Volts}}{\mu\text{s}}$ |

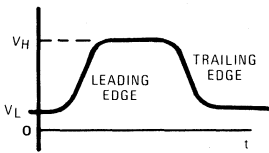
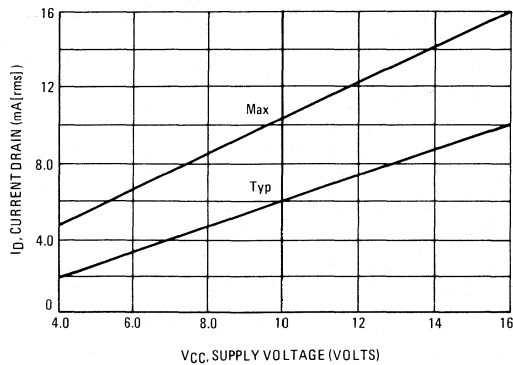


FIGURE 2 – RMS CURRENT DRAIN



MFC4050

AUDIO DRIVER

Advance Information

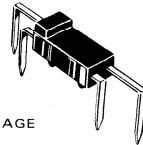
CLASS "A" AUDIO DRIVER

... designed for driving Class "A" PNP power output transistor stage applications.

- Drives to 4 Watts of Output Power
- Ideal for 12 Volt Automotive Equipment
- No Gain Selection of Power Transistors Necessary
- Economical 4-Lead Package

CLASS "A" AUDIO DRIVER

Silicon Monolithic
Functional Circuit

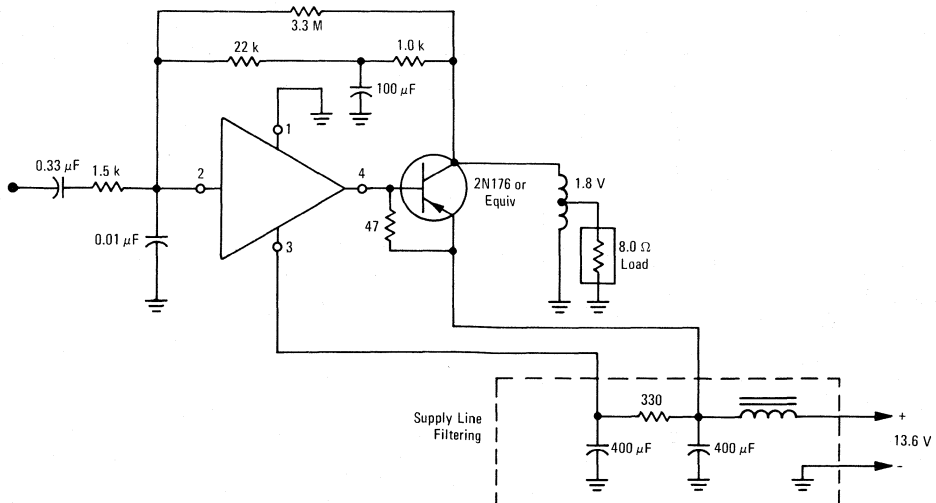


CASE 206A
PLASTIC PACKAGE

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|--------------------------|------------|------------------------------|
| Power Supply Voltage | V^+ | 18 | Vdc |
| Power Dissipation @ $T_A = 25^\circ\text{C}$ (Package Dissipation) Derate above 25°C | P_D $1/\theta_{JA}$ | 1.0 10 | Watt mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -10 to +75 | $^\circ\text{C}$ |

FIGURE 1 - TYPICAL 4-WATT AMPLIFIER CIRCUIT APPLICATION



See Packaging Information Section for outline dimensions.

MFC4050 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

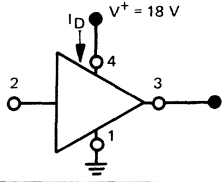
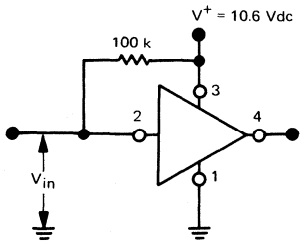
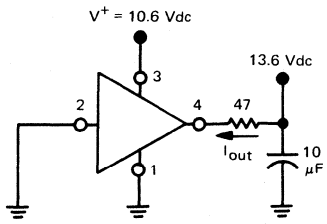
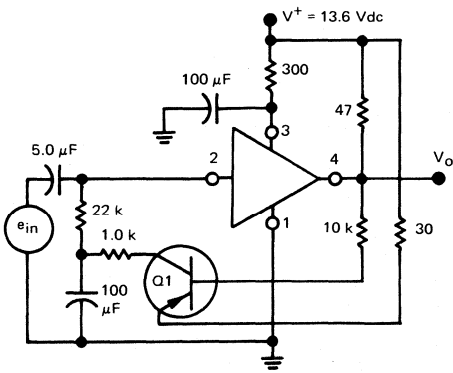
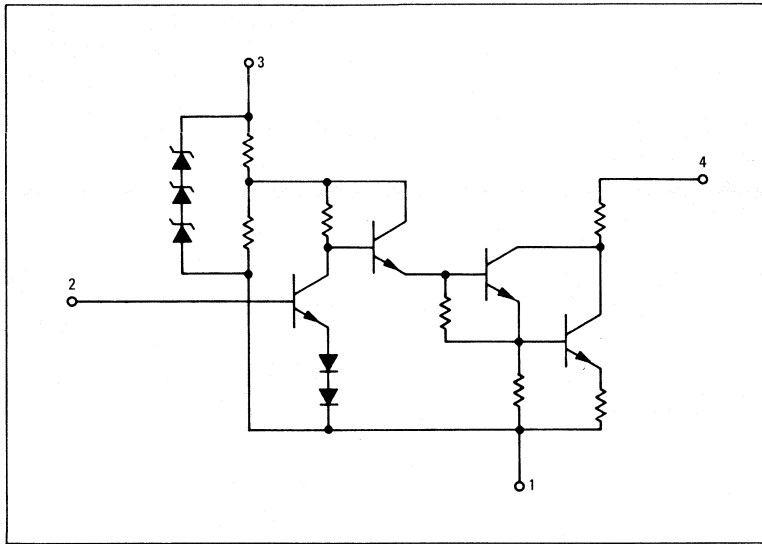
| Circuit | Characteristic | Symbol | Min | Max | Unit |
|---|--|-----------|-----|-----|-------|
|  | Current Drain No Load | I_D | — | 10 | mA |
|  | Input Voltage | V_{in} | 1.9 | 2.5 | Vdc |
|  | Output Current ($e_{in} = 1.0 \text{ mV (rms) @ 1.0 kHz}$) | I_{out} | 30 | — | mA dc |
|  | Open Loop Voltage Gain ($e_{in} = 1.0 \text{ mV (rms) @ 1.0 kHz}$) Q1: MPS6514 or equiv. | A_{VOL} | 130 | — | V/V |

FIGURE 2 – CIRCUIT SCHEMATIC



VOLTAGE REGULATORS

MFC4060A MFC4062A MFC4063A MFC4064A

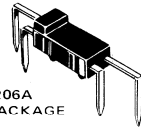
MONOLITHIC VOLTAGE REGULATORS

This series of voltage regulators is designed to deliver load currents to 200 mA dc. Output current capability can be increased to several amperes through the use of external pass transistors. These devices are industrial quality regulators designed for consumer applications requiring high volume and low cost.

- Excellent Line and Load Regulation
- Economical Four-Lead Package

VOLTAGE REGULATORS

Silicon Monolithic
Functional Circuit



CASE 206A
PLASTIC PACKAGE

FIGURE 1 – TYPICAL CIRCUIT CONNECTION AND TEST CIRCUIT

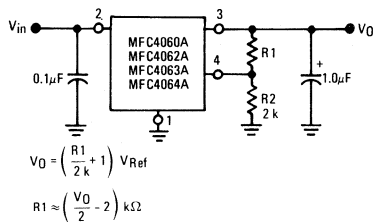


FIGURE 2 – 5-VOLT, 5-AMPERE REGULATOR WITH REMOTE SENSING PNP CURRENT BOOST

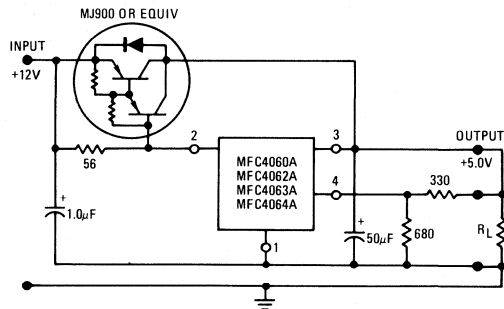
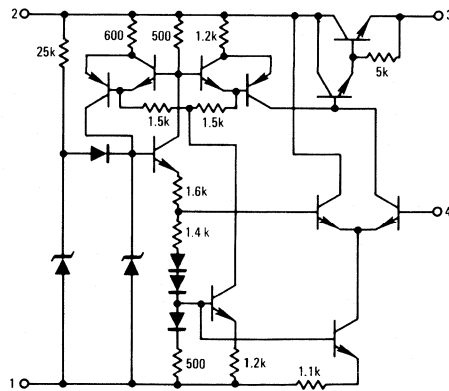


FIGURE 3 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MFC4060A, MFC4062A, MFC4063A, MFC4064A (continued)

MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|--|-----------|-------------|------------------------|
| Input Voltage | V_{in} | 38 | Vdc |
| | | 22 | Vdc |
| Maximum Load Current | I_L | 200 | mAdc |
| Power Dissipation (Package Limitation) Derate above $T_A = +25^{\circ}\text{C}$ | P_D | 1.0 | Watt |
| | | 10 | mW/ $^{\circ}\text{C}$ |
| Operating Temperature Range (Ambient) | T_A | -10 to +75 | $^{\circ}\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^{\circ}\text{C}$ |

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: $T_A = +25^{\circ}\text{C}$, $V_{in} = 12\text{ Vdc}$, $V_O = 5.0\text{ Vdc}$, $I_L = 10\text{ mAdc}$, See Figure 1.)

| Characteristic | Symbol | MFC4060A | | | MFC4062A | | | MFC4063A | | | MFC4064A | | | Unit |
|---|----------------|-----------|-------|------|-----------|-------|------|-----------|-------|------|-----------|-------|------|-----------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage Range | V_{in} | 9.0 | — | 38 | 9.0 | — | 38 | 9.0 | — | 22 | 9.0 | — | 22 | Vdc |
| Output Voltage Range | V_O | V_{ref} | — | 35 | V_{ref} | — | 35 | V_{ref} | — | 19 | V_{ref} | — | 19 | Vdc |
| Input-Output Voltage Differential | $V_{in} - V_O$ | 3.0 | — | — | 3.0 | — | — | 3.0 | — | — | 3.0 | — | — | Vdc |
| Reference Voltage | V_{ref} | 3.75 | 4.1 | 4.35 | 3.6 | 4.1 | 4.6 | 3.75 | 4.1 | 4.35 | 3.6 | 4.1 | 4.6 | Vdc |
| Standby Current Drain ($I_L = 0$, $V_{in} = 20\text{ V}$) | I_{IB} | — | 3.7 | 6.0 | — | 3.7 | 7.0 | — | 3.7 | 6.0 | — | 3.7 | 7.0 | mAdc |
| Average Temperature Coefficient of Output Voltage ($T_A = -10$ to $+75^{\circ}\text{C}$) | TC_{VO} | — | 0.003 | 0.03 | — | 0.003 | 0.03 | — | 0.003 | 0.03 | — | 0.003 | 0.03 | %/ $^{\circ}\text{C}$ |
| Line Regulation ($V_O = 7.5\text{ V}$) $12\text{ V} < V_{in} < 18$ $12\text{ V} < V_{in} < 30$ | Reg_{in} | — | — | — | — | — | — | — | 0.01 | 0.03 | — | — | 0.06 | %/ V_{in} |
| | | — | 0.01 | 0.03 | — | — | 0.06 | — | — | — | — | — | — | — |
| Load Regulation (1.0 mA $I_L < 50\text{ mA}$) | Reg_L | — | 0.03 | 0.2 | — | — | 0.4 | — | 0.03 | 0.2 | — | — | 0.4 | % |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

LINE REGULATION

$$\% / V_{in} = \frac{\Delta V_O \times 100}{\Delta V_{in} \times V_O}$$

LOAD REGULATION

$$\% = \frac{\Delta V_O}{V_O} \times 100$$

TYPICAL CHARACTERISTICS

($V_{in} = 12\text{ Vdc}$, $V_O = 5.0\text{ Vdc}$, $I_L = 1.0\text{ mAdc}$, $T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT versus INPUT-OUTPUT VOLTAGE

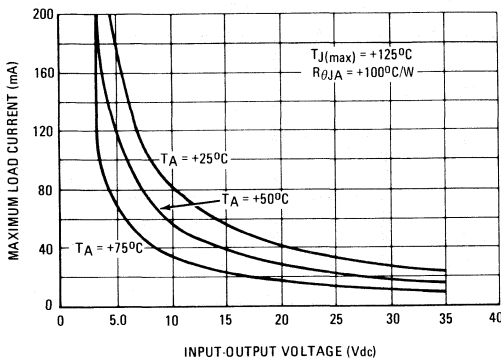
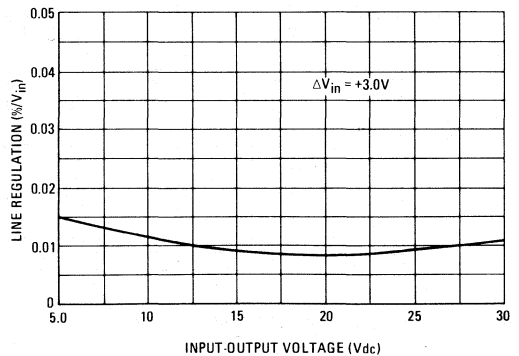


FIGURE 5 – LINE REGULATION versus INPUT-OUTPUT VOLTAGE



MFC6010

FM IF AMPLIFIER

FM LIMITING IF AMPLIFIER

... a monolithic silicon integrated circuit designed especially for 10.7 MHz IF applications.

Highlights Include:

- High Stable Gain @ 10.7 MHz (40 dB typ)
- Low Feedback Capacitance ($|y_{12}| = 0.01$ mmho typ)
- Non-Saturating Limiting (With Suitable Load)
- Compatible With CA3053 and $\mu A703$ (See Figures 7 and 8)

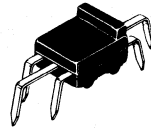
MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|--|-----------------|------------|----------------------------|
| Power Supply Voltage | V^+ | 20 | Vdc |
| Output Collector Voltage | V_4 | 20 | Vdc |
| Input Voltage* | V_2, V_5 | ± 5.0 | Volts |
| Power Dissipation @ $T_A = 25^\circ\text{C}$ (Package Limitation) | P_D | 1.0 | Watt |
| Derate above 25°C | $1/\theta_{JA}$ | 10 | $\text{mW}/^\circ\text{C}$ |
| Operating Temperature Range | T_A | -10 to +75 | $^\circ\text{C}$ |

* Differential Voltage Swing.

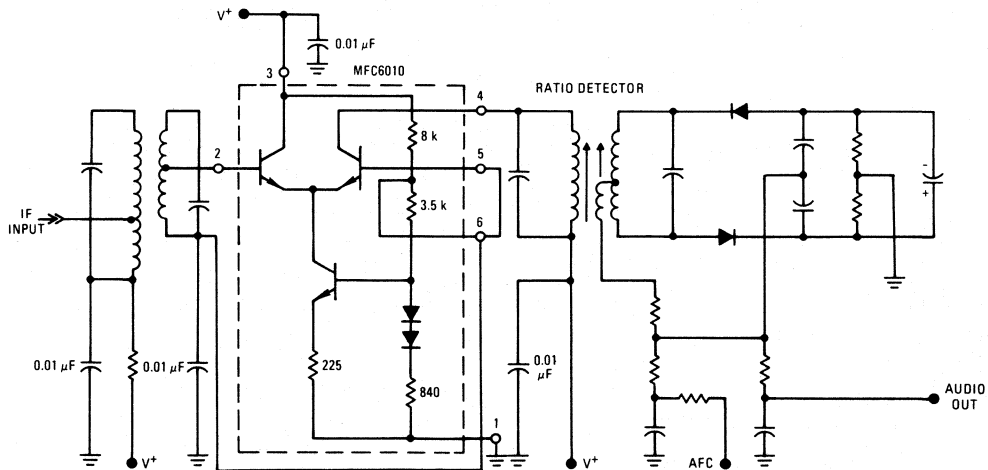
FM IF AMPLIFIER

Silicon Monolithic
Functional Circuit



CASE 643A
PLASTIC PACKAGE

FIGURE 1 - Typical Application (10.7 MHz Limiting Amplifier)



See Packaging Information Section for outline dimensions.

MFC6010 (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = 12$ Volts, $f = 10.7$ MHz, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

| Circuit for I_D | Characteristic | Symbol | Min | Typ | Max | Unit |
|-------------------|--|-----------------|------|------|-----|------------------|
| | Total Current Drain | I_D | — | — | 10 | mA |
| | Output Quiescent Current | I_Q | 1.75 | 3.2 | 5.0 | mA |
| | Output Saturation Voltage | $V(\text{sat})$ | — | 3.5 | — | Volts |
| | Forward Transadmittance | $ y_{21} $ | 25 | — | — | mmhos |
| | Reverse Transadmittance | $ y_{12} $ | — | 0.01 | — | mmho |
| | Input Capacitance | C_{in} | — | 6.0 | — | pF |
| | Input Conductance | G_{in} | — | 0.4 | — | mmho |
| | Output Capacitance | C_{out} | — | 2.5 | — | pF |
| | Output Conductance | G_{out} | — | 35 | — | μmhos |
| | Noise Figure ($R_S = 750 \Omega$) | N_F | — | 7.0 | — | dB |
| | Maximum Stable Gain (Stern Factor = 3) | A_V | — | 40 | — | dB |
| | Input Voltage (3.0 dB Limiting) | e_{in} | — | 60 | — | mV |

FIGURE 2 – LIMITING CHARACTERISTICS

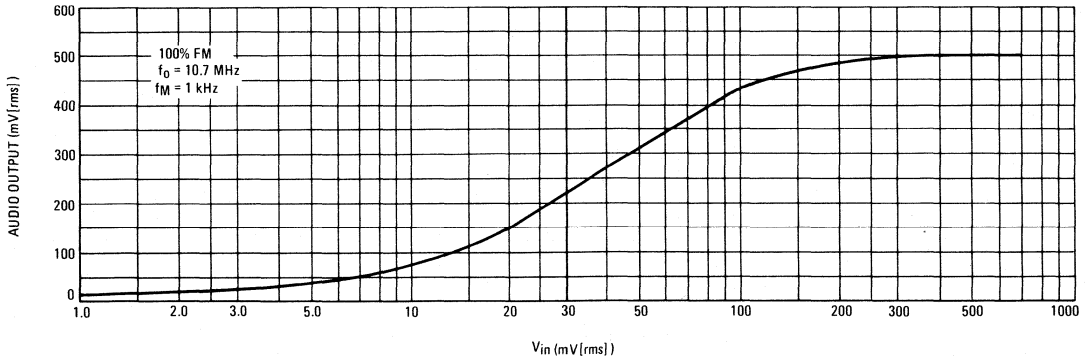


FIGURE 3 – AM REJECTION

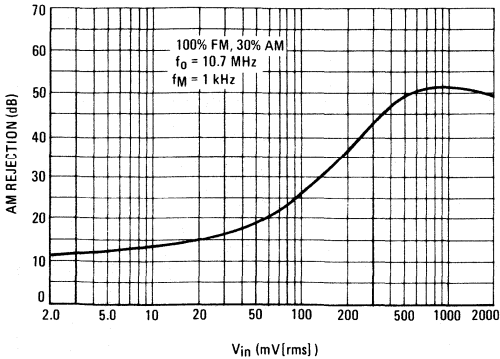
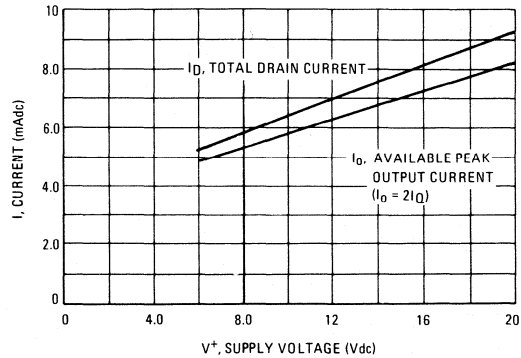
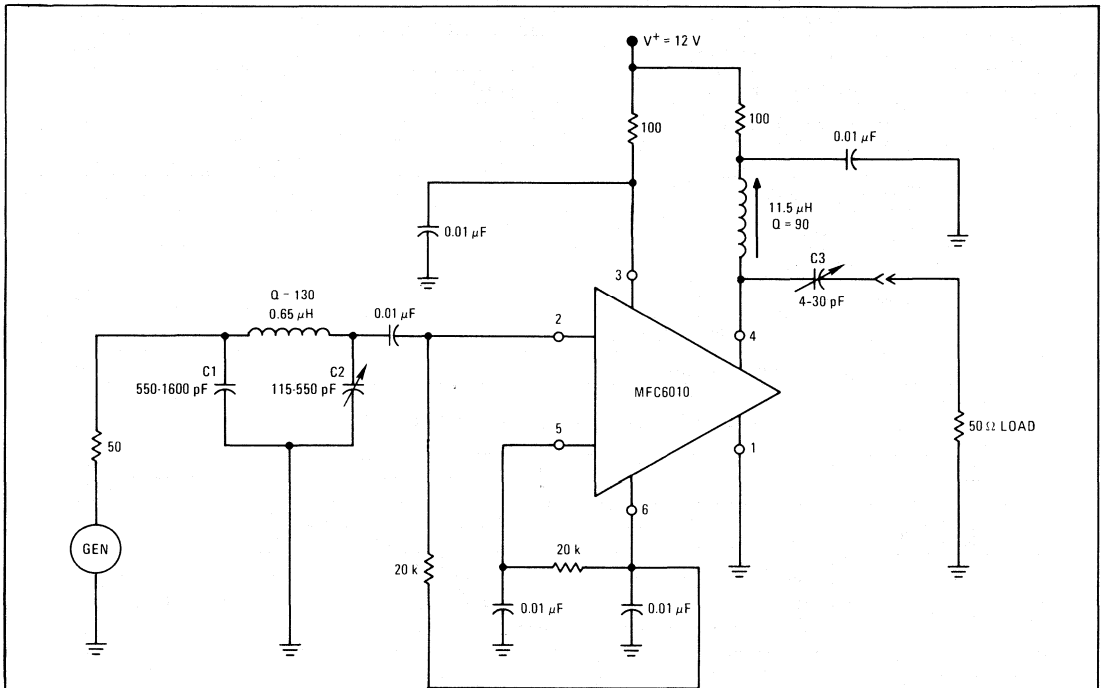


FIGURE 4 – CURRENT DRAIN AND OUTPUT CURRENT



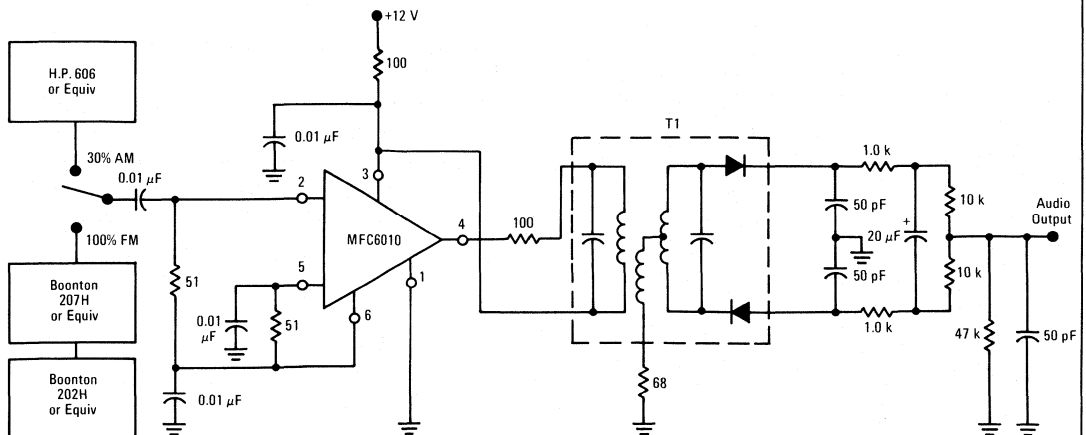
TEST CIRCUITS

FIGURE 5 – POWER-GAIN TEST CIRCUIT



Note: C1 (1000 pF nom), C2 (420 pF nom), C3 (20 pF nom) adjusted for maximum power gain.

FIGURE 6 – LIMITING AND AM REJECTION TEST CIRCUIT



T1 – Ratio Detector Primary Impedance $\approx 1.5 \text{ k}\Omega$

7

MFC6010 (continued)

APPLICATIONS INFORMATION

Because of the low reverse transfer admittance of the MFC6010, stability will be dependent mainly upon circuit layout. With careful design, very high gain (in the order of 40 dB) may be achieved at 10.7 MHz. The bias and supply currents may be varied from their normal values (shown in Figure 4) by shunting additional resistance from pin 6 to ground or to the supply line.

Although less gain may be realized when using the MFC6010 as a limiter, it is recommended that it be operated in a non-saturated mode. This mode of operation results in a high output impedance at limiting. Therefore the operation of the demodulator circuit is not subject to variable loading of the limiter output.

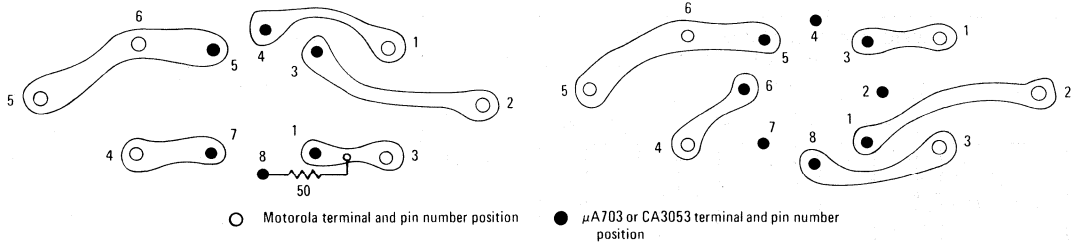
In order to avoid driving the amplifier transistor components of the MFC6010 into saturation, the load resistance must be

chosen to ensure that current limiting occurs before the collector voltage drops to a value low enough to forward bias the collector-base junction. In a transformer coupled circuit, the maximum allowable load can be derived from

$$R_L = \frac{2(V^+ - V_5)}{I_0}$$

where values for I_0 may be determined from Figure 4 (providing the bias currents have not been altered from their normal values).

In order to avoid degradation of AM rejection, the input signal should not exceed one volt (rms).



*Foil patterns shown are intended to show pin-for-pin interconnection. Any change in the number of components is dictated by the requirements of the individual design.

MFC6020

DUAL TOGGLE FLIP-FLOP

DUAL TOGGLE FLIP-FLOP

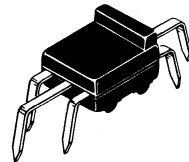
- Wide Operating Voltage Range — 4.0 to 16 Volts
- Regulated Supply Not Required
- Compatible with TTL and DTL
- Economical 6-Lead Plastic Package

DUAL TOGGLE FLIP-FLOP

Silicon Monolithic Functional Circuit

MAXIMUM RATINGS

| Rating | Symbol | Value | Volts |
|---|--------------------------|-------------|---------------|
| Power Supply Voltage | V_{CC} | 19 | Vdc |
| Output Sinking Current | I_{sink} | 10 | mA |
| Negative Input Voltage | V_{in} | 0.5 | Vdc |
| Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D $1/\theta_{JA}$ | 1.0 10 | Watt mW/°C |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -40 to +125 | °C |
| Operating Temperature Range | T_A | -10 to +75 | °C |



CASE 643A
PLASTIC PACKAGE

TYPICAL APPLICATION — ELECTRONIC ORGAN DIVIDER

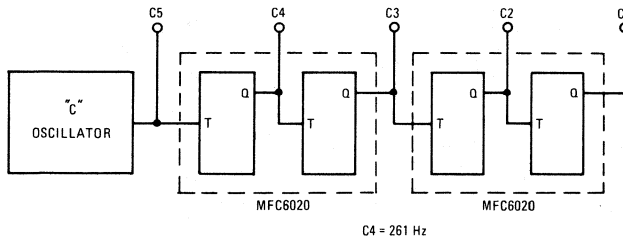
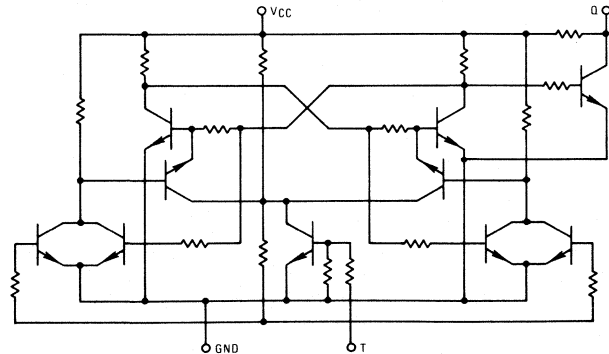
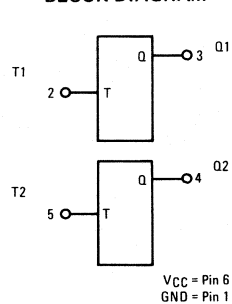


FIGURE 1 — CIRCUIT SCHEMATIC (One Half of Circuit Shown)



BLOCK DIAGRAM



See Packaging Information Section for outline dimensions.

MFC6020 (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = 12$ Vdc, $V_{in} = 4.0$ V, Square Pulse, $f = 10$ kHz, 50% Duty Cycle, $t_f = 1.0$ V/ μ s (Min), $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------|-------------|--------|------------|-----------|
| Operating Power Supply Voltage | V_{CC} | 4.0 | — | 16 | Vdc |
| Toggle Frequency | f_{Tog} | — | 3.0 | — | MHz |
| Output Voltage (High) ($V_{CC} = 4.0$ Vdc) ($V_{CC} = 16$ Vdc) | V_{OH} | 3.5 15.5 | — — | — — | Vdc |
| Output Voltage (Low) ($V_{CC} = 4.0$ Vdc) ($V_{CC} = 16$ Vdc) | V_{OL} | — — | — — | 0.5 1.0 | Vdc |
| Operating Drain Current | I_D | — | — | 32 | mAdc |
| Output Sinking Current ($V_o \leq 1.0$ Vdc) | I_{sink} | — | 2.0 | — | mAdc |
| Rise Time | t_r | — | 250 | — | ns |
| Storage Time | t_s | — | 350 | — | ns |
| Fall Time | t_f | — | 60 | — | ns |
| Cross Talk ($V_{in} = 15$ V, Square Pulse, $V_{CC} = 16$ Vdc) T1 to Q2 T2 to Q1 | V_o | — — | — — | 15 15 | mV |
| Input Resistance | R_{in} | 10 | — | — | $k\Omega$ |
| Output Resistance (Output High) | R_{OH} | — | — | 2.8 | $k\Omega$ |

INPUT PULSE REQUIREMENTS

| Characteristic | Symbol | Min | Max | Unit |
|-----------------|-----------------|------|------|------------------------------------|
| Pulse Magnitude | V_H | +4.0 | — | Volts |
| Zero Level | V_L | — | +1.0 | Volts |
| Leading Edge | No Requirement | | | |
| Trailing Edge | $\frac{dv}{dt}$ | -1.0 | — | $\frac{\text{Volts}}{\mu\text{s}}$ |

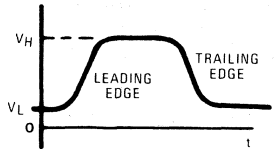
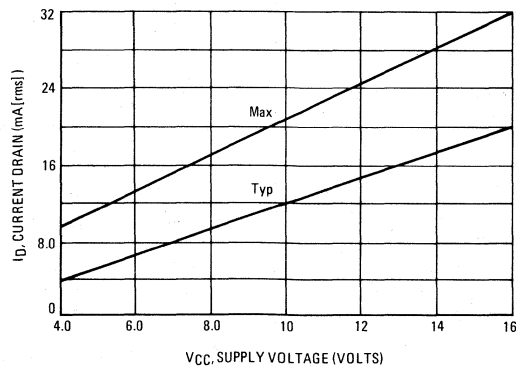


FIGURE 2 – RMS CURRENT DRAIN versus SUPPLY VOLTAGE



VOLTAGE REGULATORS

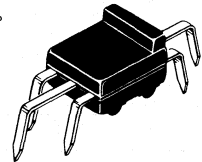
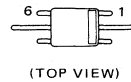
MFC6030A MFC6032A MFC6033A MFC6034A

MONOLITHIC VOLTAGE REGULATORS

This series of voltage regulators is designed to deliver load currents to 200 mAdc. Output current capability can be increased to several amperes through the use of external pass transistors. These devices are industrial quality regulators intended for consumer applications requiring high volume and low cost.

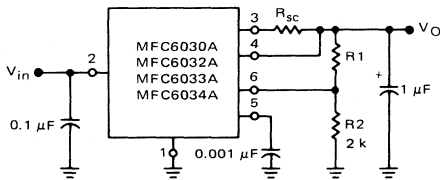
- Excellent Line and Load Regulation
- Current-Limit Feature Available
- Economical Six-Lead Package

VOLTAGE REGULATORS MONOLITHIC SILICON FUNCTIONAL CIRCUITS



PLASTIC PACKAGE
CASE 643A

FIGURE 1 – TYPICAL CIRCUIT CONNECTION AND TEST CIRCUIT



$$V_O = \left(\frac{R_1}{2k} + 1 \right) V_{ref}$$

$$R_1 \approx \left(\frac{V_O}{2} - 2 \right) k\Omega$$

FIGURE 3 – CIRCUIT SCHEMATIC

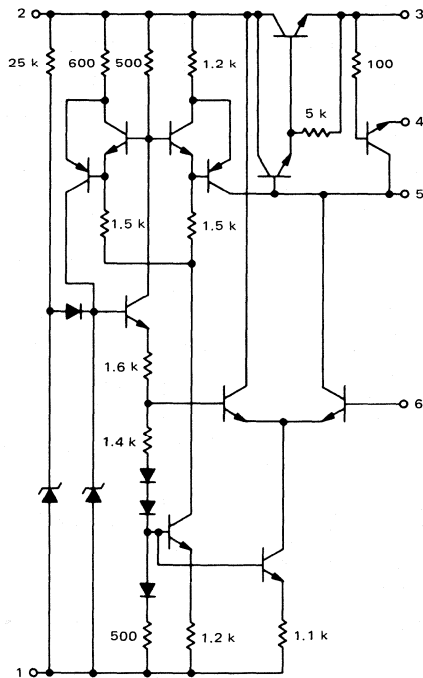
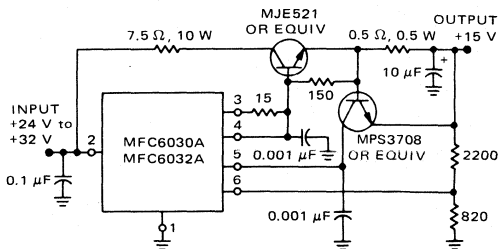


FIGURE 2 – 15-VOLT, 1.0-AMPERE REGULATOR
(with short-circuit protection)



MFC6030A, MFC6032A, MFC6033A, MFC6034A (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

| Rating | Symbol | Value | Unit |
|---|------------------|-------------|---------------|
| Input Voltage MFC6030A, MFC6032A MFC6033A, MFC6034A | V _{in} | 38 22 | Vdc |
| Maximum Load Current | I _L | 200 | mAdc |
| Power Dissipation (Package Limitation) Derate above T _A = +25°C | P _D | 1.0 10 | Watt mW/°C |
| Operating Temperature Range (Ambient) | T _A | -10 to +75 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS (V_{in} = +12 Vdc, V_O = +5.0 Vdc, I_L = 1.0 mAdc, R_{sc} = 0, T_A = +25°C unless otherwise noted.) (See Figure 1)

| Characteristic | Symbol | MFC6030A | | | MFC6032A | | | MFC6033A | | | MFC6034A | | | Unit |
|--|---------------------------------|------------------|-------|------|------------------|-------|------|------------------|-------|------|------------------|-------|------|-------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage Range | V _{in} | 9.0 | — | 38 | 9.0 | — | 38 | 9.0 | — | 22 | 9.0 | — | 22 | Vdc |
| Output Voltage Range | V _O | V _{Ref} | — | 35 | V _{Ref} | — | 35 | V _{Ref} | — | 19 | V _{Ref} | — | 19 | Vdc |
| Input-Output Voltage Differential | V _{in} -V _O | 3.0 | — | — | 3.0 | — | — | 3.0 | — | — | 3.0 | — | — | Vdc |
| Reference Voltage (R ₁ = 0) | V _{ref} | 3.75 | 4.1 | 4.35 | 3.6 | 4.1 | 4.6 | 3.75 | 4.1 | 4.35 | 3.6 | 4.1 | 4.6 | Vdc |
| Standby Current Drain (I _L = 0, V _{in} = 20 V) | I _{IB} | — | 3.7 | 6.0 | — | 3.7 | 7.0 | — | 3.7 | 6.0 | — | 3.7 | 7.0 | mAdc |
| Average Temperature Coefficient of Output Voltage (T _A = -10 to +75°C) | TCV _O | — | 0.003 | 0.03 | — | 0.003 | 0.03 | — | 0.003 | 0.03 | — | 0.003 | 0.03 | %/°C |
| Line Reg. (V _O = 7.5 V) (12 V < V _{in} < 18) (12 V < V _{in} < 30) | Reg _{in} | — | — | — | — | — | — | — | 0.01 | 0.03 | — | — | 0.06 | %/V _{in} |
| Load Regulation (1.0 mA < I _L < 50 mA) | Reg _L | — | 0.03 | 0.2 | — | — | 0.4 | — | 0.03 | 0.2 | — | — | 0.4 | %/V _O |
| Short-Circuit Current Limit (R _{sc} = 100 ohms, V _O = 0) | I _{sc} | — | 6.5 | — | — | 6.5 | — | — | 6.5 | — | — | 6.5 | — | mAdc |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

$$\text{LINE REGULATION} \\ \%/V_{in} = \frac{\Delta V_O \times 100}{\Delta V_{in} \times V_O}$$

$$\text{LOAD REGULATION} \\ \% = \frac{\Delta V_O}{V_O} \times 100$$

$$\text{SHORT-CIRCUIT CURRENT} \\ I_{SC} = \frac{V_{BE} \approx 0.65 \text{ (at } T_J = +25^\circ\text{C)}}{R_{sc} = 100 \text{ ohms}}$$

TYPICAL CHARACTERISTICS

(V_{in} = 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{sc} = 0, T_A = +25°C unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT versus INPUT-OUTPUT VOLTAGE

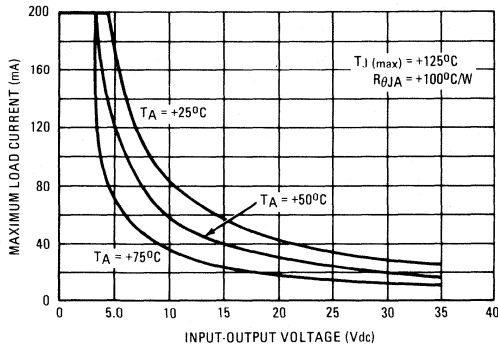
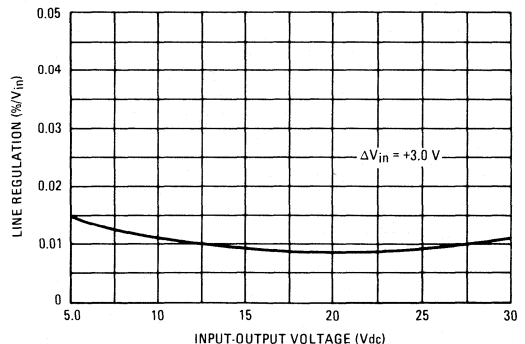


FIGURE 5 – LINE REGULATION versus INPUT-OUTPUT VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – LOAD REGULATION versus INPUT-OUTPUT VOLTAGE

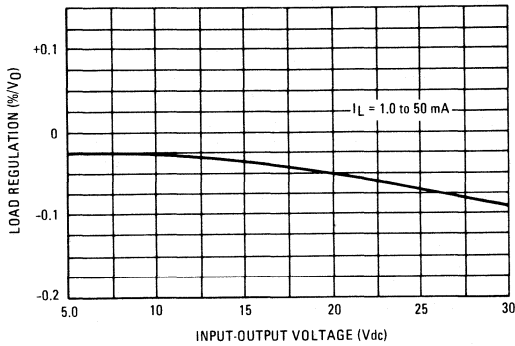


FIGURE 7 – LOAD REGULATION WITH CURRENT LIMITING

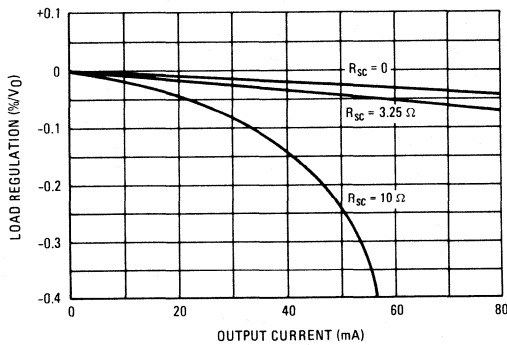
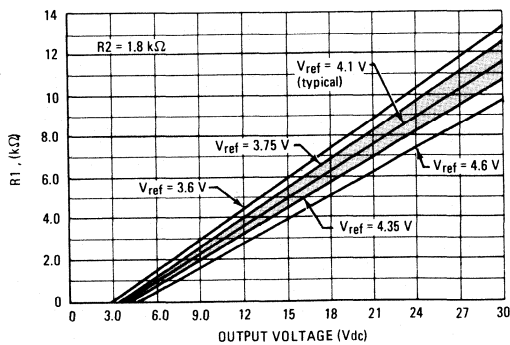
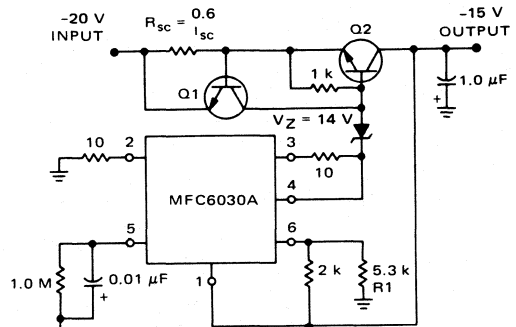


FIGURE 8 – OUTPUT VOLTAGE versus R1



TYPICAL APPLICATIONS

FIGURE 9 – MFC6030A -15 VOLT REGULATOR with CURRENT LIMIT

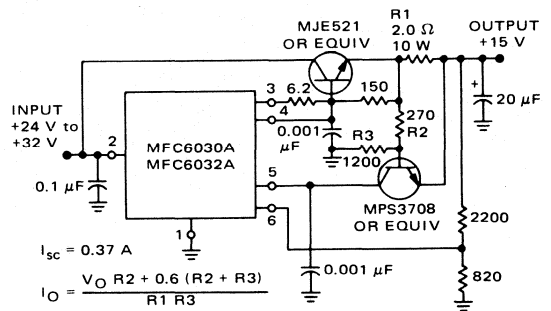


NOTE: For other output voltages:
 $(-9 \text{ V} \leq V_O \leq -35 \text{ V})$

$$R1 \text{ (k}\Omega\text{)} = \frac{2 |V_O|}{V_{ref}} - 2$$

$$V_z = |V_{in}| - \frac{|V_O|}{2} + 1$$

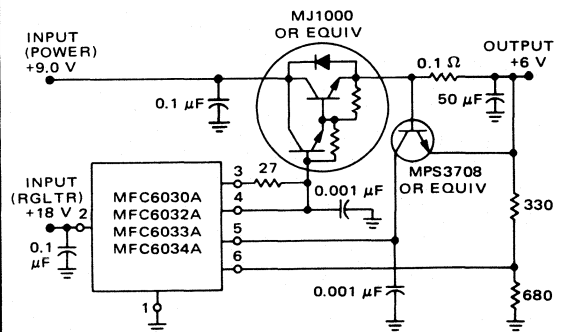
FIGURE 10 – -15-VOLT, 2.0-AMPERE REGULATOR (with current foldback)



$$I_{sc} = 0.37 \text{ A}$$

$$I_O = \frac{V_O R2 + 0.6 (R2 + R3)}{R1 R3}$$

FIGURE 11 – 6.0-VOLT, 5.0-AMPERE HIGH EFFICIENCY REGULATOR



7

MFC6030A, MFC6032A, MFC6033A, MFC6034A (continued)

TYPICAL APPLICATIONS (continued)

FIGURE 12 – CURRENT BYPASS
(Load current range, 400-to-500 mA)

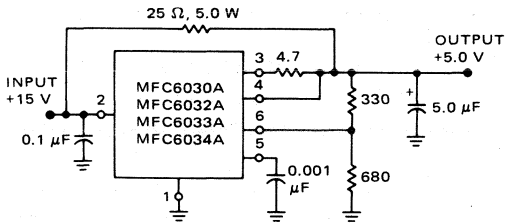


FIGURE 13 – 100 mA CONSTANT CURRENT SOURCE

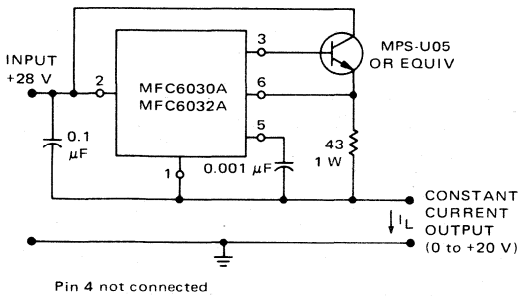


FIGURE 15 – VOLTAGE BOOSTED 40-VOLT,
100 mA REGULATOR
(with short-circuit current limiting)

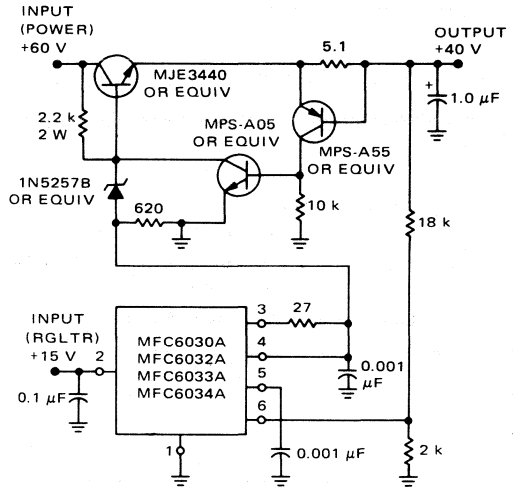
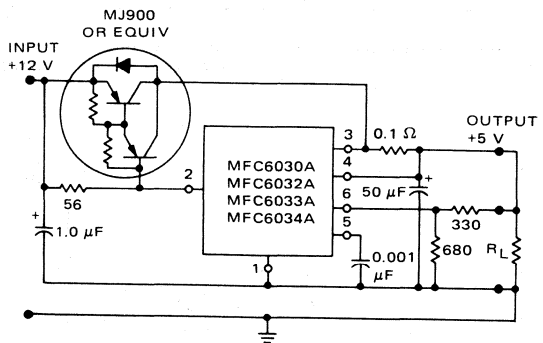


FIGURE 14 – 5.0-VOLT, 5.0-AMPERE REGULATOR with
REMOTE SENSING, PNP CURRENT BOOST



MFC6040

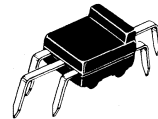
ELECTRONIC ATTENUATOR

ELECTRONIC ATTENUATOR

- Designed for use in:
 - DC Operated Volume Control
 - Compression and Expansion Amplifier Applications
- Controlled by DC Voltage or External Variable Resistor
- Economical 6-Lead Plastic Package

ELECTRONIC ATTENUATOR

Silicon Monolithic
Functional Circuit

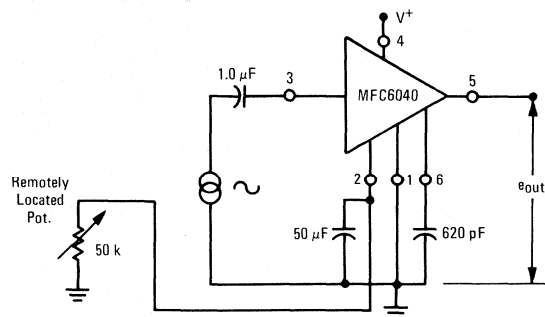


CASE 643A
PLASTIC PACKAGE

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

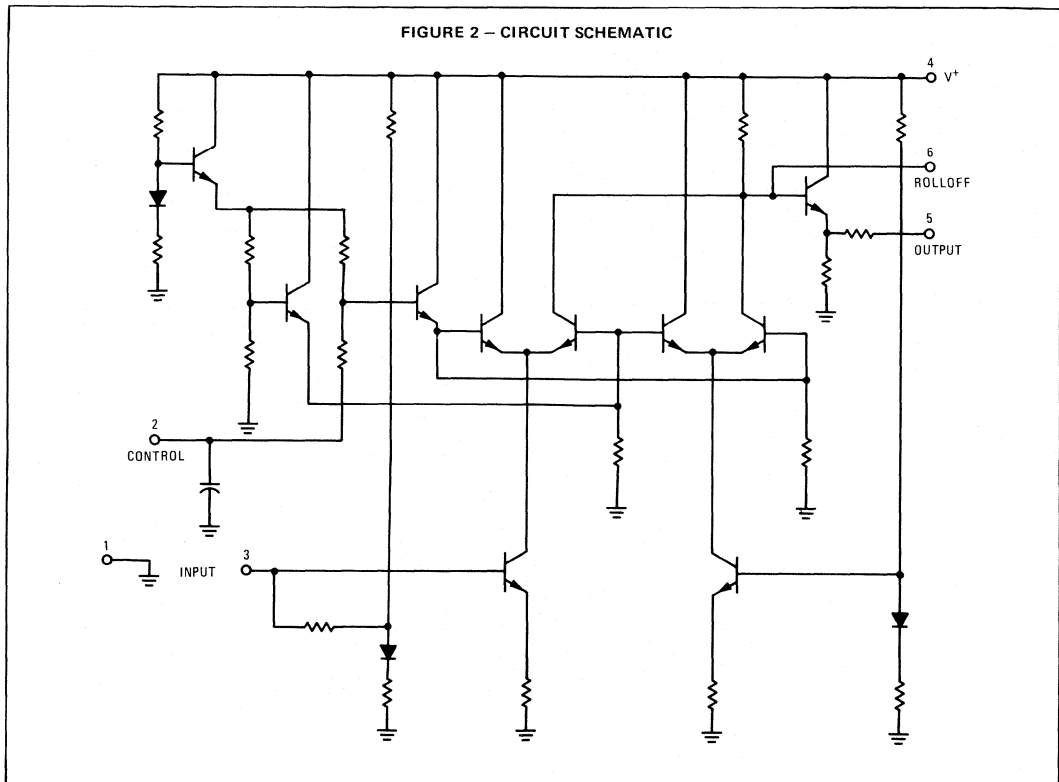
| Rating | Symbol | Value | Unit |
|---|-----------------|------------|----------------------|
| Power Supply Voltage | V^+ | 21 | Vdc |
| Power Dissipation @ $T_A = 25^\circ\text{C}$ (Package Limitation) Derate above $T_A = 25^\circ\text{C}$ | P_D | 1.0 | Watt |
| | $1/\theta_{JA}$ | 10 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -10 to +75 | $^\circ\text{C}$ |

FIGURE 1 – TYPICAL DC "REMOTE" VOLUME CONTROL



ELECTRICAL CHARACTERISTICS ($e_{in} = 100 \text{ mV}$, $f = 1.0 \text{ kHz}$, $R_1 = 0$, $V^+ = 16 \text{ Vdc}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Circuit | Characteristic | Symbol | Min | Typ | Max | Unit | |
|---------|--|----------|-----|-----|-----|--------|----|
| | Operating Power Supply Voltage | V^+ | 9.0 | — | 18 | Vdc | |
| | Control Terminal Sink Current ($e_{in} = 0$) | I_{cs} | — | — | 2.0 | mAdc | |
| | Maximum Input Voltage | e_{in} | — | — | 0.5 | V(rms) | |
| | Voltage Gain | A_V | 11 | 13 | — | dB | |
| | Attenuation Range ($R_C = 33 \text{ k ohms}$) | | | 70 | 90 | — | dB |
| | Total Harmonic Distortion ($e_{in} = 100 \text{ mV}$, $e_o = 100 \text{ mV}$) | THD | — | 0.6 | 1.0 | % | |



TYPICAL ELECTRICAL CHARACTERISTICS
 ($V^+ = 16 \text{ Vdc}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

FIGURE 3 – ATTENUATION versus DC CONTROL VOLTAGE

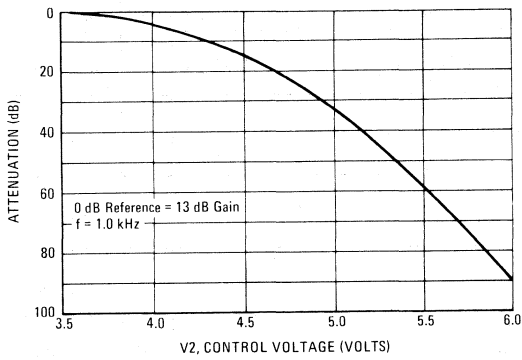


FIGURE 4 – ATTENUATION versus CONTROL RESISTOR

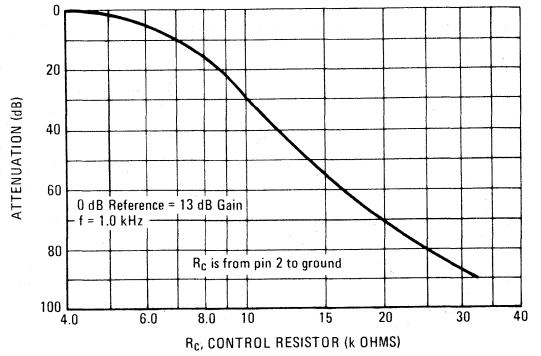


FIGURE 5 – FREQUENCY RESPONSE

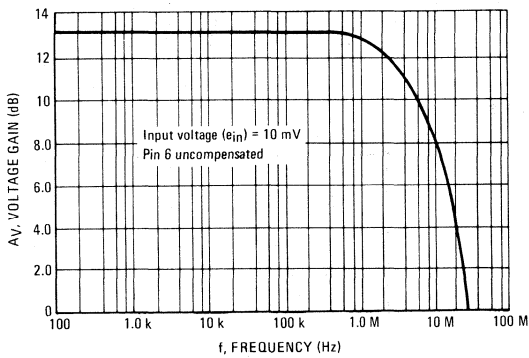


FIGURE 6 – OUTPUT VOLTAGE SWING

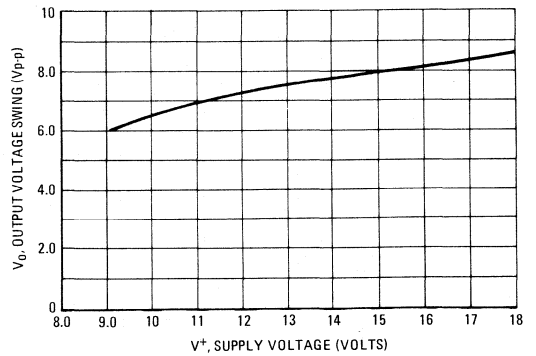
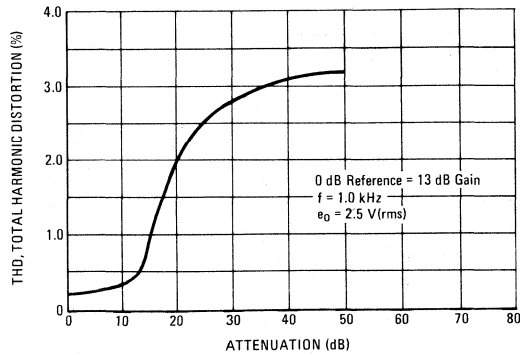


FIGURE 7 – TOTAL HARMONIC DISTORTION



MFC6050

DUAL TOGGLE FLIP-FLOP

DUAL TOGGLE FLIP-FLOP WITH RESET

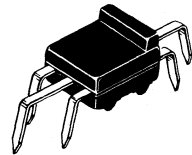
- Wide Operating Voltage Range – 4.0 to 16 Volts
- Regulated Supply Not Required
- Compatible with TTL and DTL
- Economical 6-Lead Plastic Package
- Reset (R) Available to Set Output to 0 Regardless of Previous History

DUAL TOGGLE FLIP-FLOP WITH RESET

Silicon Monolithic Functional Circuit

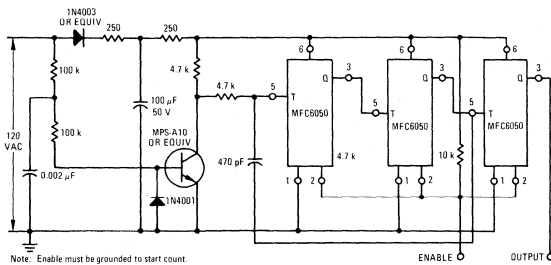
MAXIMUM RATINGS

| Rating | Symbol | Value | Volts |
|---|--------------------------|------------|------------------------|
| Power Supply Voltage | V_{CC} | 19 | Vdc |
| Output Sinking Current | I_{sink} | 15 | mA |
| Negative Input Voltage | V_{in} | 0.5 | Vdc |
| Power Dissipation @ $T_A = 25^\circ C$ Derate above $25^\circ C$ | P_D $1/\theta_{JA}$ | 1.0 10 | Watt mW/ $^\circ C$ |
| Operating Temperature Range | T_A | -10 to +75 | $^\circ C$ |

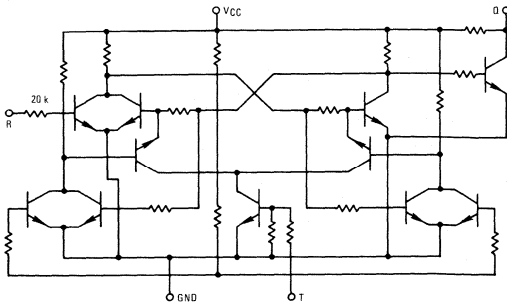


CASE 643A

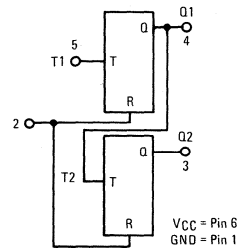
TYPICAL APPLICATION – DIVIDE BY 60 COUNTER



SIMPLIFIED CIRCUIT SCHEMATIC (One-Half of Circuit Shown)



BLOCK DIAGRAM



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 12$ Vdc, $V_{in} = 4.0$ V, Square Pulse, $f = 10$ kHz, 50% Duty Cycle, $t_f = 1.0$ V/ μ s (Min), $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------|-------------|--------|------------|-----------|
| Operating Power Supply Voltage | V_{CC} | 4.0 | — | 16 | Vdc |
| Toggle Frequency | f_{Tog} | — | 3.0 | — | MHz |
| Output Voltage (High) ($V_{CC} = 4.0$ Vdc) ($V_{CC} = 16$ Vdc) | V_{OH} | 3.5 15.5 | — — | — — | Vdc |
| Output Voltage (Low) ($V_{CC} = 4.0$ Vdc) ($V_{CC} = 16$ Vdc) | V_{OL} | — — | — — | 0.5 1.0 | Vdc |
| Operating Drain Current | I_D | — | — | 32 | mAdc |
| Output Sinking Current ($V_o = 1.0$ Vdc) | I_{sink} | — | 8.0 | — | mAdc |
| Rise Time | t_r | — | 250 | — | ns |
| Storage Time | t_s | — | 350 | — | ns |
| Fall Time | t_f | — | 60 | — | ns |
| Cross Talk ($V_{in} = 15$ V, Square Pulse, $V_{CC} = 16$ Vdc) T1 to Q2 T2 to Q1 | V_o | — — | — — | 15 15 | mV |
| Max V_{in} at R for no effect @ 75°C | | — | 1.0 | — | Vdc |
| Input Resistance | R_{in} | 10 | — | — | $k\Omega$ |
| Output Resistance (Output High) | R_{OH} | — | — | 2.8 | $k\Omega$ |

INPUT PULSE REQUIREMENTS

| Characteristic | Symbol | Min | Max | Unit |
|-----------------|-----------------|----------------|------|------------------------------------|
| | | | | |
| Pulse Magnitude | V_H | +4.0 | — | Volts |
| Zero Level | V_L | — | +1.0 | Volts |
| Leading Edge | | No Requirement | | |
| Trailing Edge | $\frac{dv}{dt}$ | -1.0 | — | $\frac{\text{Volts}}{\mu\text{s}}$ |

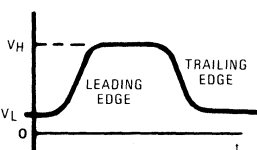
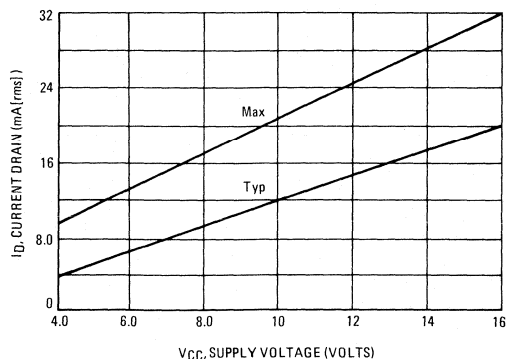


FIGURE 2 – RMS CURRENT DRAIN versus SUPPLY VOLTAGE



MFC6060

3-INPUT "AND" GATE

3-INPUT "AND" GATE

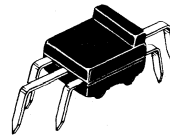
- Wide Operating Voltage – to 16 Volts
- Compatible with TTL and DTL
- Economical 6-Lead Plastic Package
- Regulated Supply Not Required

3-INPUT "AND" GATE

Silicon Monolithic
Functional Circuit

MAXIMUM RATINGS

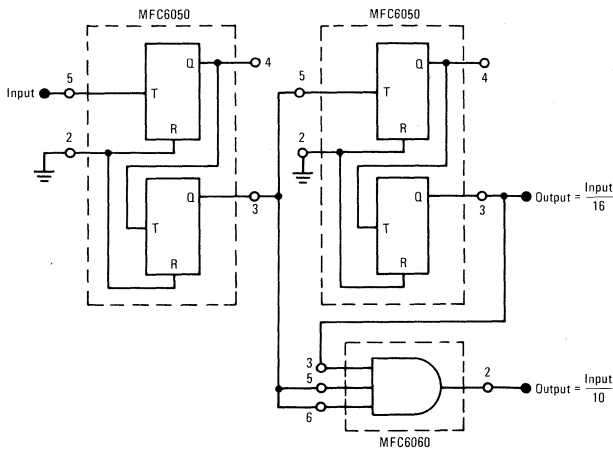
| Rating | Symbol | Value | Unit |
|---|-----------------|-------------|----------------------|
| Power Supply Voltage | V_{CC} | 19 | Vdc |
| Power Dissipation @ $T_A = 25^\circ\text{C}$ (Package Limitation) Derate above 25°C | P_D | 1.0 | Watt |
| | $1/\theta_{JA}$ | 10 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | 0 to +75 | $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -40 to +125 | $^\circ\text{C}$ |



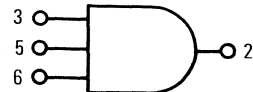
CASE 643A
PLASTIC PACKAGE

TYPICAL APPLICATION

FIGURE 1 – DIVIDE-BY-10



BLOCK DIAGRAM



$V_{CC} = \text{Pin 4}$
 $GND = \text{Pin 1}$

See Packaging Information Section for outline dimensions.

MFC6060 (continued)

ELECTRICAL CHARACTERISTICS ($V_{CC} = 16 \text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Figure | Symbol | Min | Max | Unit |
|---|--------|----------|-----|-----|------|
| Output Voltage – Low Pin 3 = V_{CC} ; Pin 5 = V_{CC} ; Pin 6 = GND Pin 5 = GND; Pin 6 = V_{CC} ; Pin 3 = V_{CC} Pin 3 = GND; Pin 5 = V_{CC} ; Pin 6 = V_{CC} | 2 | V_{OL} | – | 0.6 | Vdc |
| Output Voltage – High | 3 | V_{OH} | 15 | – | Vdc |
| Drain Current | 3 | I_D | – | 10 | mAdc |

FIGURE 2 – OUTPUT VOLTAGE (LOW) TEST CIRCUIT

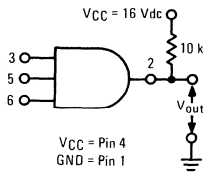


FIGURE 3 – OUTPUT VOLTAGE (HIGH) TEST CIRCUIT

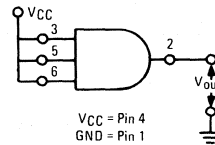
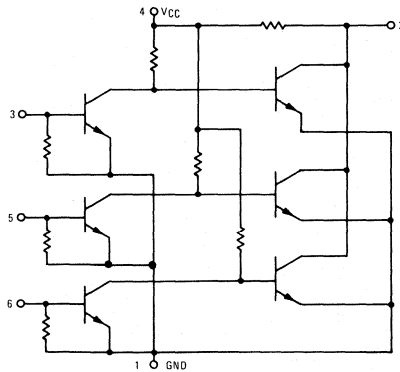


FIGURE 4 – CIRCUIT SCHEMATIC



7

MFC6070

AUDIO POWER AMPLIFIER

1-WATT AUDIO POWER AMPLIFIER

... designed primarily for low-cost audio amplifiers in phonograph, TV and radio applications.

- 100 mV Sensitivity for 1-Watt*
- Low Distortion – 1% @ 1-Watt typ*
- Short-Circuit Proof – Short Term (10 seconds typ)
- No Heatsink Required for 1-Watt Output at $T_A = 55^\circ\text{C}^{**}$
- Excellent Hum Rejection

*Circuit Dependent
**Voltage Dependent

1-WATT AUDIO POWER AMPLIFIER

Silicon Monolithic
Functional Circuit

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

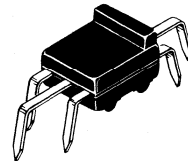
| Rating | Symbol | Value | Unit |
|--|-----------------|-------------|----------------------|
| Power Supply Voltage | V^+ | 20 | Vdc |
| Power Dissipation | P_D | 1.0 | Watt |
| Derate above $T_A = +25^\circ\text{C}$ | $1/\theta_{JA}$ | 8.0 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -10 to +55 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -40 to +150 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|-----------------|-----|---------------------------|
| Thermal Resistance, Junction to Ambient | θ_{JA}^* | 125 | $^\circ\text{C}/\text{W}$ |

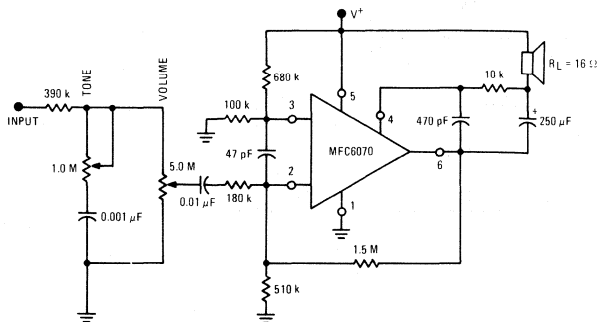
*Thermal resistance is measured in still air with fine wires connected to the leads, representing the "worst case" situation.

For a larger power requirement, pin 1 must be soldered to at least one sq. in. of copper foil on the printed circuit board. The θ_{JA} will be no greater than $+90^\circ\text{C}/\text{W}$. Thus, 1.39 Watts could be dissipated at $+25^\circ\text{C}$, which must be linearly derated at $11.1 \text{ mW}/^\circ\text{C}$ from $+25^\circ\text{C}$ to $+150^\circ\text{C}$.



CASE 643A
PLASTIC PACKAGE

FIGURE 1 – TYPICAL 1-WATT PHONOGRAPH AMPLIFIER
(Ceramic cartridge input)



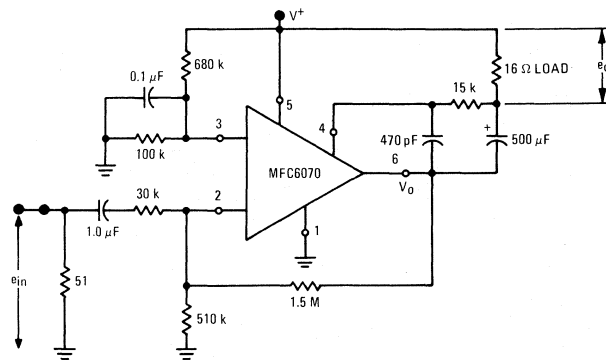
See Packaging Information Section for outline dimensions.

MFC6070 (continued)

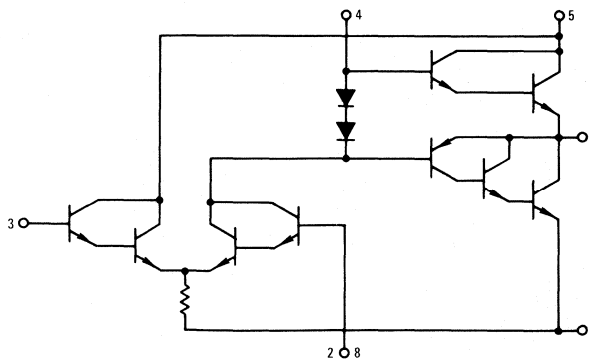
ELECTRICAL CHARACTERISTICS ($V^+ = 16$ Vdc, See Figure 2 for test circuit, $T_A = +25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|----------|-----|-----|-----|------|
| Quiescent Output Voltage | V_o | — | 8.0 | — | Vdc |
| Quiescent Drain Current ($e_{in} = 0$) | I_D | — | 5.0 | 18 | mA |
| Sensitivity, Input Voltage (e_{in} adjusted for $e_o = 4.0$ V(rms) @ 1.0 kHz, Power Output = 1.0 Watt) | e_{in} | — | 100 | 150 | mV |
| Total Harmonic Distortion ($e_o = 4.0$ V(rms) @ 1.0 kHz, Power Output = 1.0 Watt) (e_{in} adjusted for $e_o = 1.26$ V(rms) @ 1.0 kHz, Power Output = 100 mW) | THD | — | 1.0 | 10 | % |
| Hum and Noise (IHF Standard A201, 1966) | — | — | -40 | — | dB |

FIGURE 2 — 1-WATT AUDIO POWER AMPLIFIER TEST CIRCUIT



Circuit Schematic



7

TYPICAL CHARACTERISTICS

($V^+ = 16$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 3 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER

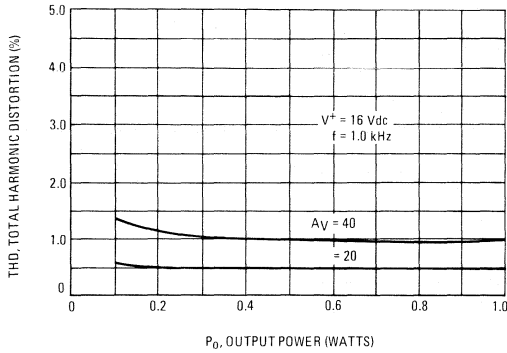


FIGURE 4 – POWER DISSIPATION versus OUTPUT POWER

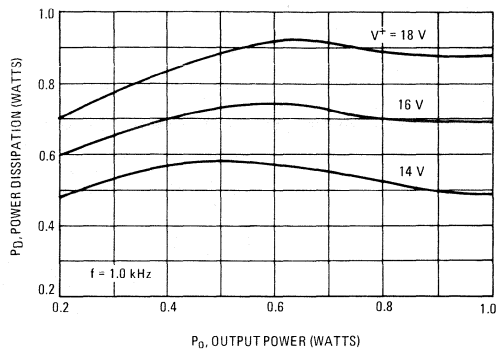
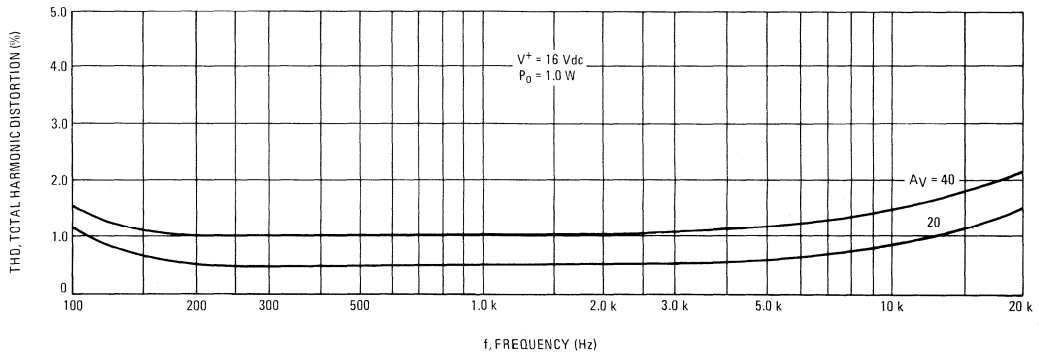


FIGURE 5 – TOTAL HARMONIC DISTORTION versus FREQUENCY



APPLICATIONS INFORMATION

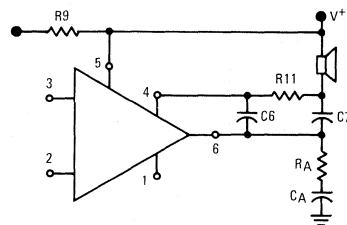
Shown in Figures 7 and 11 are low cost 1 W phono amplifiers with a sensitivity (@ 1 kHz) of approximately 450 mV. The input impedance of both amplifiers is approximately equal to R_4 and the gain is determined by $(R_7 + R_{10})/R_5$. To change the gain of the amplifier, change the value of R_5 and hold $(R_7 + R_{10})$ between 1 M and 2.2 M. This allows the use of a small and less expensive capacitor for C_2 .

The bass boost effect shown in the frequency response curves (Figures 10 and 14) is provided by the parallel combination of C_4 and R_{10} and can be eliminated by removing C_4 and replacing $(R_7 + R_{10})$ with a 2.2 Megohm resistor. High frequency compensation is provided by C_6 and the low frequency roll-off is determined by the impedance network of C_2 and R_5 , C_3 and R_4 , and C_8 and the speaker. The series combination of R_A and C_A from pin 6 to ground may be required for stability, depending on printed circuit board layout, speaker reactance, and lead lengths.

Device ac short-circuit capability was tested in both the 8-ohm and 16-ohm amplifiers by shorting pin 6 thru a 500 microfarad capacitor to ground for a period of ten seconds with the amplifier operating at full rated output.

The speaker can be connected to V^+ (alternate connection shown below) or ground (Figures 7 and 11). Printed circuit board art work (1:1 pattern) is shown for both systems in Figures 16 and 18. A picture of the completed board for the grounded speaker system is shown in Figure 21.

ALTERNATE CONNECTION FOR SPEAKER TO V^+
(See Figure 20 for Parts List)



APPLICATIONS INFORMATION (continued)

($R_L = 8.0$ ohms, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 6 - POWER SUPPLY

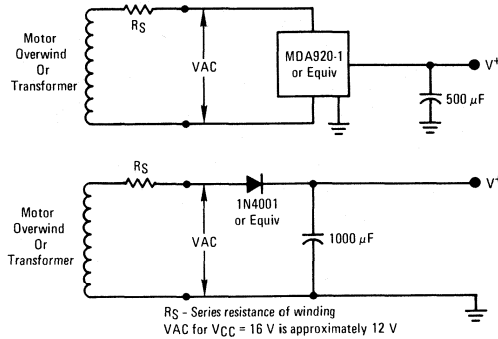


FIGURE 7 - PHONOGRAPH AMPLIFIER 1 WATT - 8 OHM
(See Figure 15 for Parts List)

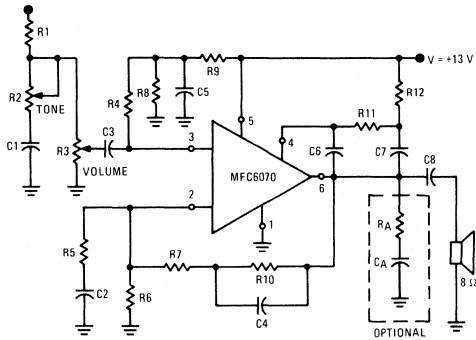


FIGURE 8 - TOTAL HARMONIC DISTORTION
versus OUTPUT POWER FOR FIGURE 7

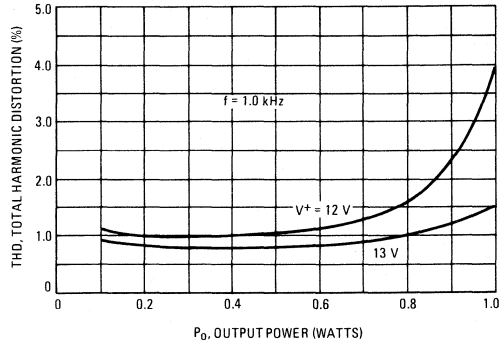


FIGURE 9 - TOTAL HARMONIC DISTORTION
versus FREQUENCY FOR FIGURE 7

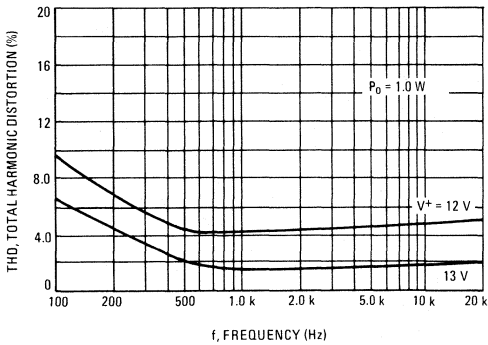
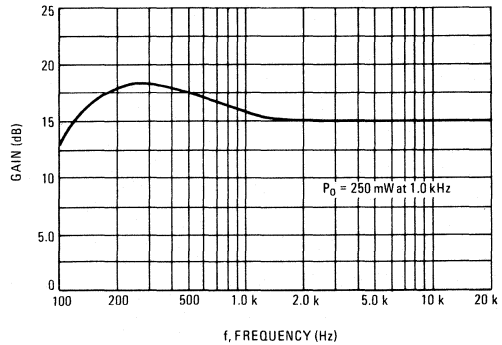


FIGURE 10 - FREQUENCY RESPONSE FOR FIGURE 7



APPLICATIONS INFORMATION (continued)

($R_L = 16$ ohms, $T_A = +25^\circ\text{C}$ unless otherwise noted)

FIGURE 11 – 1.0 WATT, 16 OHM LOAD PHONOGRAPH AMPLIFIER
(See Figure 15 for Parts List)

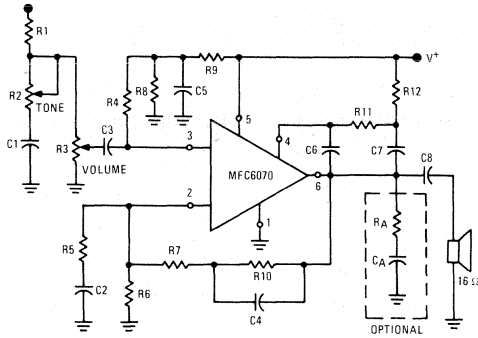


FIGURE 12 – TOTAL HARMONIC DISTORTION
versus OUTPUT POWER FOR FIGURE 11

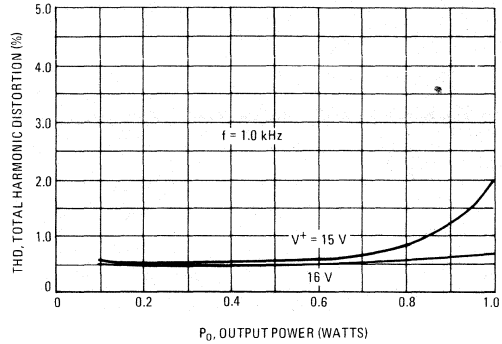


FIGURE 13 – TOTAL HARMONIC DISTORTION
versus FREQUENCY FOR FIGURE 11

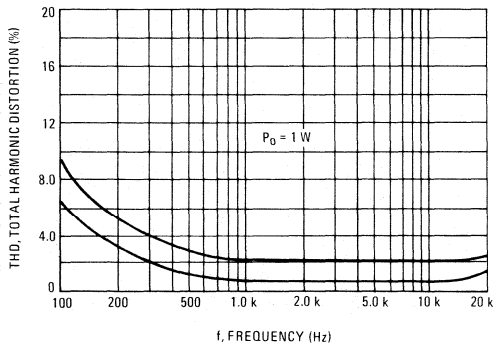


FIGURE 14 – FREQUENCY RESPONSE FOR FIGURE 11

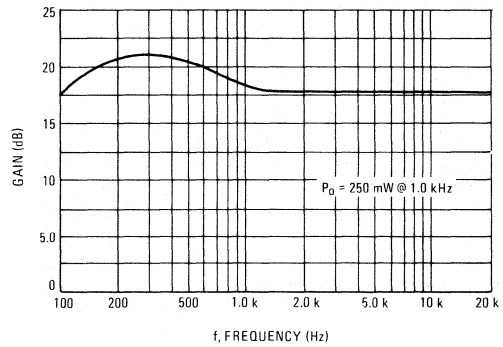


FIGURE 15 – PARTS LIST FOR FIGURES 7 AND 11

| | | |
|------------------|------------------------|---------------------------|
| R1 = 180 k ohms | R9 = 1.0 Megohm | C3 = 0.05 μF |
| R2 = 5.0 Megohms | R10 = 1.5 Megohms | C4 = 470 pF |
| R3 = 5.0 Megohms | R11 = 6.8 kilohms | C5 = 0.1 μF |
| R4 = 1.0 Megohm | R12 = 6.8 kilohms | C6 = 470 pF |
| R5 = 150 k ohms* | RA = 10 ohms** | C7 = 0.1 μF |
| R6 = 910 k ohms* | C1 = 470 pF | C8 = 500 μF * |
| R7 = 680 k ohms | C2 = 0.1 μF | CA = 0.1 μF ** |
| R8 = 180 k ohms | | |

*For Figure 11 (16-ohm load) change R5 to 100 k ohms, R6 to 820 k ohms and C8 to 250 μF .

**Optional – Not included on board. (See Applications Information Note)

APPLICATIONS INFORMATION (continued)

FIGURE 16 – PRINTED CIRCUIT BOARD (Foil Side)
(Speaker Grounded)

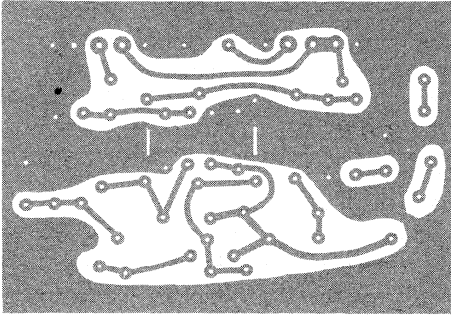


FIGURE 17 – COMPONENT DIAGRAM FOR FIGURE 16

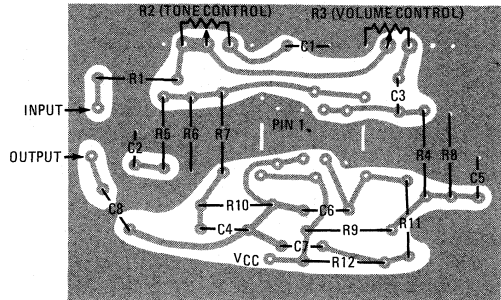


FIGURE 18 – PRINTED CIRCUIT BOARD (Foil Side)
(Speaker to V⁺)

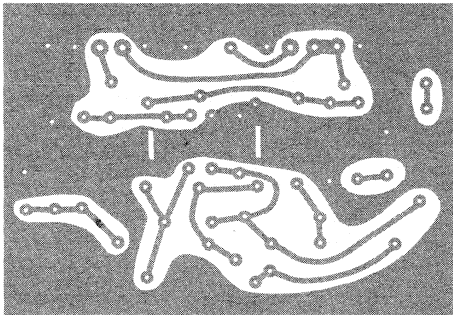


FIGURE 19 – COMPONENT DIAGRAM FOR FIGURE 18

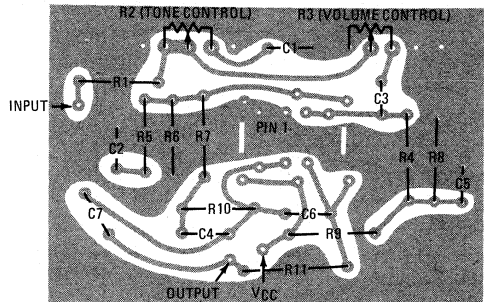
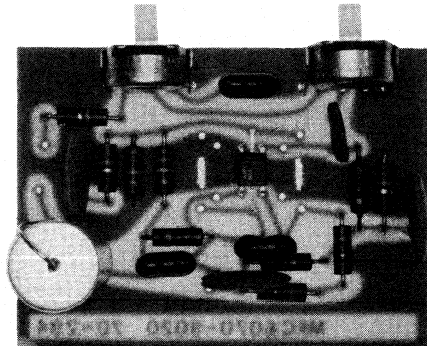


FIGURE 20 – PARTS LIST FOR FIGURE 19
(See Applications Information Note)

| | |
|---------------------------|--------------------------|
| R1 = 180 k ohms | C1,C4,C6 = 470 pF |
| R2,R3 = 5.0 Megohms | C2,C5 = 0.1 μF |
| R4,R9 = 1.0 Megohm | C3 = 0.05 μF |
| R5 = 82 k ohms | C7 = 250 μF |
| R6 = 820 k ohms | C _A = 0.1 μF* |
| R7 = 680 k ohms | |
| R8 = 180 k ohms | |
| R10 = 1.5 Megohms | |
| R11 = 15 k ohms | |
| R _A = 10 ohms* | |

*Optional - Not included on board. (See Applications Information Note)

FIGURE 21 – COMPLETED BOARD
(Speaker Grounded)



MFC6080

RS FLIP-FLOP

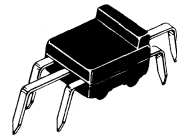
... designed for use in high-level, low-speed logic and timing systems.

- Wide Operating Voltage Range – 4.0 to 16 Volts
- High Current Buffered Outputs Allows Direct Drive of Medium Current Lamps and Relays
- Compatible with TTL and DTL
- Regulated Supply Not Required

RS FLIP-FLOP Silicon Monolithic Functional Circuit

MAXIMUM RATINGS

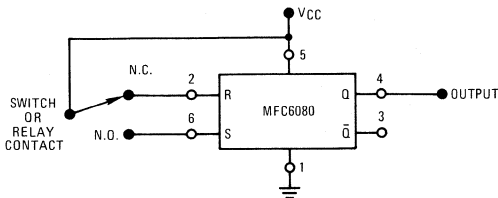
| Rating | Symbol | Value | Unit |
|---|-----------------|-------------|----------------------|
| Power Supply Voltage | V_{CC} | 19 | Vdc |
| Power Dissipation @ $T_A = 25^\circ\text{C}$ (Package Limitation) Derate above 25°C | P_D | 1.0 | Watt |
| | $1/\theta_{JA}$ | 10 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | 0 to +75 | $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -40 to +125 | $^\circ\text{C}$ |



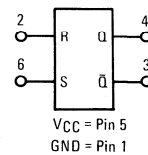
CASE 643A
PLASTIC PACKAGE

TYPICAL APPLICATION

FIGURE 1 – BOUNCELESS SWITCH



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS ($V_{CC} = 16 \text{ Vdc}$, $V_{in} = 4.0 \text{ to } 16 \text{ Vdc}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Figure | Min | Typ | Max | Unit |
|---|------------|--------|-----|-----|-----|--------------------|
| Output Voltage R Input Pin 2 = V_{in} , Pin 3 = V_{out} , Pin 6 = GND S Input Pin 2 = GND, Pin 4 = V_{out} , Pin 6 = V_{in} R S Input Pin 2 = V_{in} , Pin 4 = V_{out} , Pin 6 = V_{in} | V_{out} | 1 | 14 | — | — | Vdc |
| Saturation Voltage R Input Pin 2 = V_{in} , Pin 4 = V_{sat} , Pin 6 = GND S Input Pin 2 = GND, Pin 3 = V_{sat} , Pin 6 = V_{in} R S Input Pin 2 = V_{in} , Pin 3 = V_{sat} , Pin 6 = V_{in} | V_{sat} | 1 | — | — | 1.0 | Vdc |
| Input Current R Input I_{in} measured at Pin 2 with 4.0 Vdc applied to Pin 2 and Pin 6 grounded S Input I_{in} measured at Pin 6 with 4.0 Vdc applied to Pin 6 and Pin 2 grounded | I_{in} | 2 | — | 170 | — | μA_{dc} |
| Output Sinking Current Current into Pin 3 or Pin 4 with Q or \bar{Q} in low state | I_{sink} | — | — | — | 120 | mA_{dc} |
| Drain Current Pin 2 and 6 = GND | I_D | 2 | — | — | 20 | mA_{dc} |

FIGURE 2 – VOLTAGE TEST CIRCUIT

FIGURE 3 – CURRENT TEST CIRCUIT

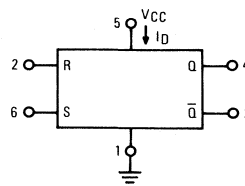
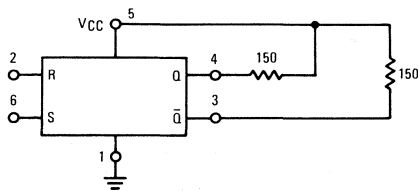
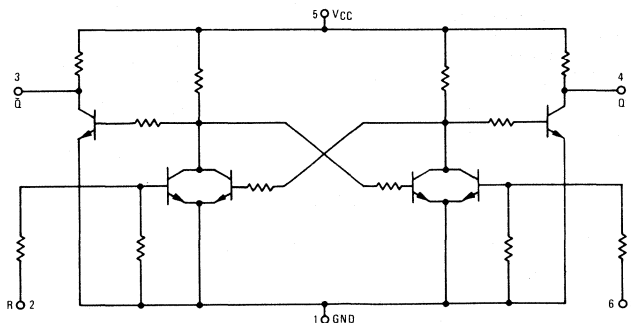


FIGURE 4 – CIRCUIT SCHEMATIC



TRUTH TABLE

| R | S | Q |
|---|---|---|
| 0 | 0 | x |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

x - the state of Q is undetermined

**MFC8000
thru
MFC8002**

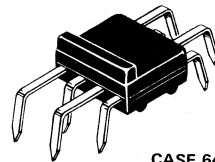
MONOLITHIC DUAL STEREO AMPLIFIER

... designed for the input stage of stereo power amplifiers.

- Excellent Channel Separation – 60 dB minimum
- High Gain – $h_{FE} = 75$ minimum
- Satisfies Both Channel Requirements with One Compact Package
- Selection of Breakdown Voltages to Meet the Particular Applications

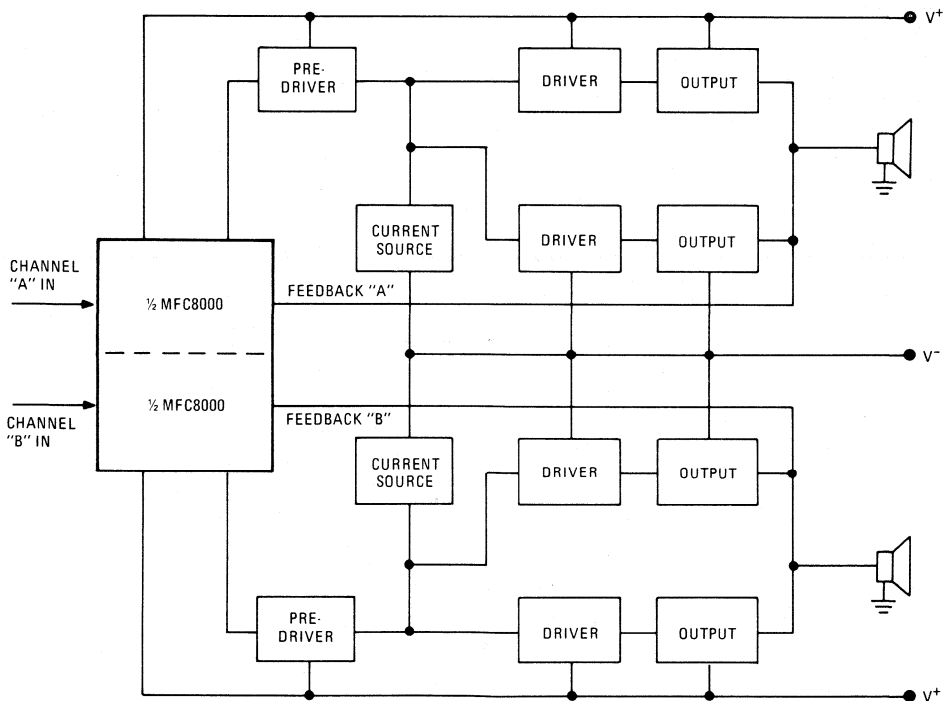
**DUAL DIFFERENTIAL AMPLIFIER
(Stereo Input Amplifier)**

**SILICON MONOLITHIC
CONSUMER CIRCUIT**



**CASE 644A
PLASTIC PACKAGE**

TYPICAL APPLICATION



See Packaging Information Section for outline dimensions.

MFC8000, MFC8001, MFC8002 (continued)

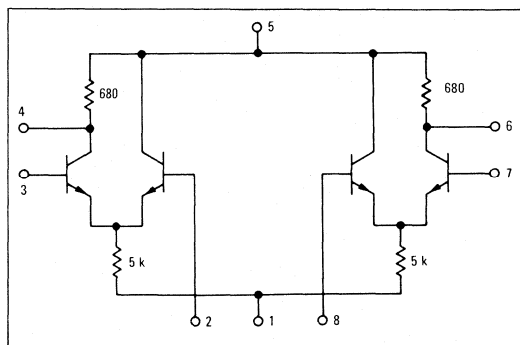
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|--------|----------------|------------------------------|
| Maximum Supply Voltage – MFC8000 MFC8001 MFC8002 | V^+ | 40 50 60 | Vdc |
| Power Dissipation (Package Limitation) (Soldered on a circuit board) Derate above $T_A = 25^\circ\text{C}$ | P_D | 1.0 10 | Watt mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -10 to +75 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|--|----------------|-------------|-------------|-----------------|
| Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}$, $I_B = 0$) | BV_{CEO} | 40 50 60 | – – – | – – – | Vdc |
| DC Current Gain ($V_{CE} = 20 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$) | h_{FE} | 75 | 100 | – | – |
| Base Differential Voltage ($V_{CE} = 20 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$) | $ \Delta V_{BE3} - \Delta V_{BE2} $ $ \Delta V_{BE8} - \Delta V_{BE7} $ | – | – | 15 | mVdc |
| Base Differential Current ($V_{CE} = 20 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$) | $ \Delta I_{B3} - \Delta I_{B2} $ $ \Delta I_{B8} - \Delta I_{B7} $ | – | – | 1.0 | μAdc |
| Channel Separation (Pins 2,3,8 grounded, signal at pin 7, e_{out1} at pin 6, e_{out2} at pin 4) | e_{out1} e_{out2} | 60 | – | – | dB |

CIRCUIT SCHEMATIC



7

MFC8010

AUDIO POWER AMPLIFIER

1-WATT AUDIO POWER AMPLIFIER

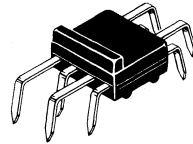
... designed to provide the complete audio system in television, radio and phonograph equipment.

- One Watt Continuous Sine Wave Power at +55°C
- High Gain – 10 mV (Max) for 1 Watt*
- Extremely Low Distortion – 1% @ 1 Watt (Typ)*
- Economical 8-Lead Plastic Package
- Short-Circuit Proof (Short Term)
- No Special Heat-Sinking Required

*Circuit Dependent.

1-WATT AUDIO POWER AMPLIFIER

Silicon Monolithic Functional Circuit

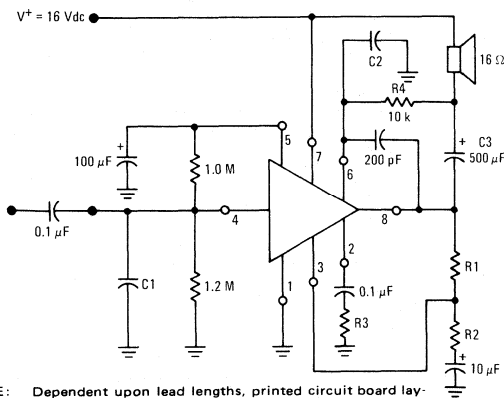


CASE 644A
PLASTIC PACKAGE

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|-----------------|------------|-------|
| Power Supply Voltage | V^+ | 22 | Vdc |
| Power Dissipation @ $T_A = 25^\circ\text{C}$ (Package Limitation) | P_D | 1.2 | Watt |
| Derate above $T_A = 25^\circ\text{C}$ | $1/\theta_{JA}$ | 10 | mW/°C |
| Operating Temperature Range | T_A | -10 to +55 | °C |

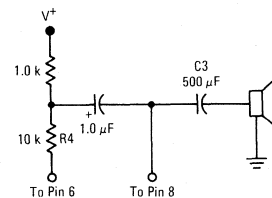
FIGURE 1 – TYPICAL 1-WATT AUDIO POWER AMPLIFIER CIRCUIT



NOTE: Dependent upon lead lengths, printed circuit board layout and output loading, a stabilization network consisting of a 0.1 µF capacitor in series with a 10 ohm resistor may be required from pin 8 to ground.

| Sensitivity For 1 Watt mV | C1 pF | C2 pF | R1 k ohms | R2 ohms | R3 ohms |
|---------------------------|-------|-------|-----------|---------|---------|
| 400 | 0 | 0 | 10 | 1.0 k | 82 |
| 10 | 100 | 100 | 51 | 100 | 2.2 k |

Alternate connection to permit connecting speaker to ground instead of to V^+ :



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Circuit | Characteristic | Symbol | Min | Typ | Max | Unit |
|---------|--|--------------|-----|-----|-----|------|
| | Quiescent Output Voltage | V_O | 7.0 | 8.0 | 9.0 | Vdc |
| | Quiescent Drain Current | I_D | — | 10 | 18 | mAdc |
| | Sensitivity, Input Voltage (e_{in} adjusted for $v_{out} = 4.0$ V(rms) @ 1.0 kHz, Power Output = 1.0 Watt) | e_{in} | — | — | 10 | mV |
| | Total Harmonic Distortion ($v_{out} = 4.0$ Vrms @ 1.0 kHz, Power Output = 1.0 Watt) (v_{in} adjusted for $v_{out} = 2.8$ V(rms) @ 1.0 kHz, Power Output = 500 mW) | THD | — | 1.5 | 5.0 | % |
| | Output Noise ($e_{in} = 0$) | $e_{n(out)}$ | — | 5.0 | — | mV |

FIGURE 2 – CIRCUIT SCHEMATIC

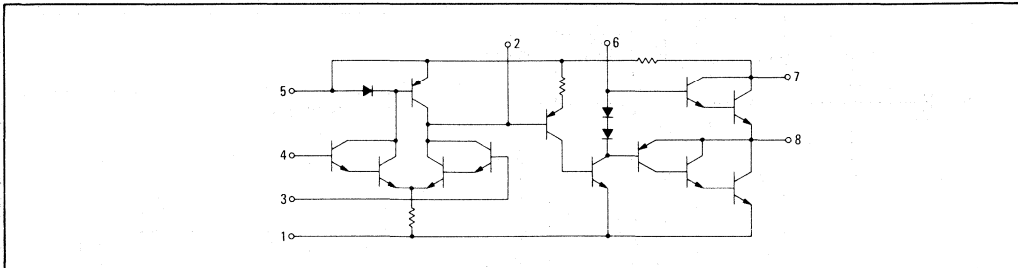


FIGURE 3 – DISTORTION

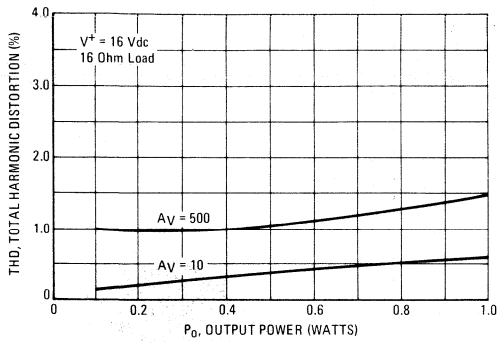


FIGURE 4 – DISTORTION

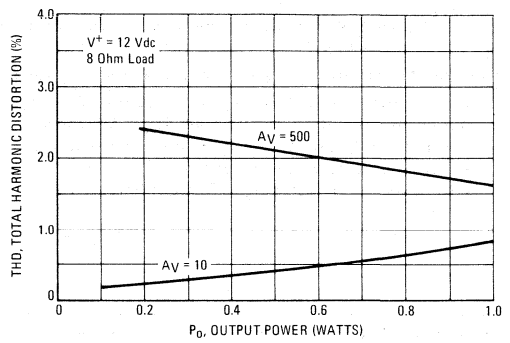


FIGURE 5 – EFFICIENCY

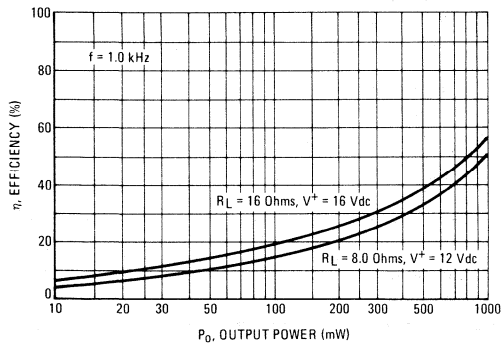
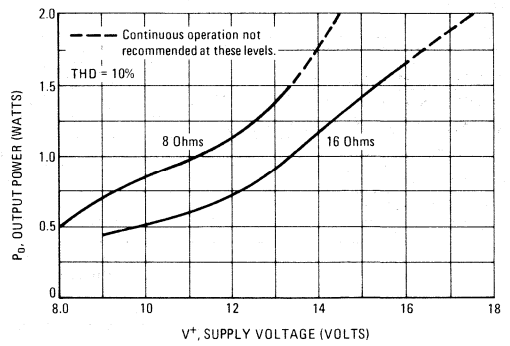


FIGURE 6 – POWER OUTPUT



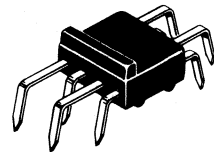
MFC8020A
MFC8021A
MFC8022A

CLASS B AUDIO DRIVERS

... designed as preamplifiers and driver circuits for complementary output transistors.

- Driver for Auto Radios – and up to 20-Watt Amplifiers
- High Gain – 7.0 mV for 1.0 Watt, $R_L = 3.2$ Ohms
- High Input Impedance – 500-Kilohm Capability
- Output Biasing Diodes Included
- No Special h_{FE} Matching of Outputs Required

CLASS B AUDIO DRIVERS
SILICON MONOLITHIC
FUNCTIONAL CIRCUITS



CASE 644A
 PLASTIC PACKAGE

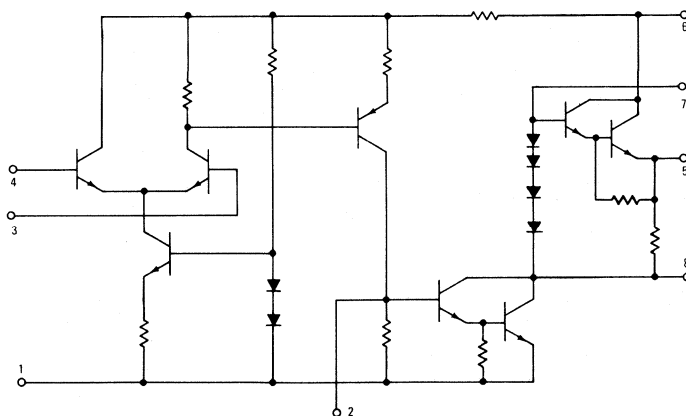
MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

| Rating | Value | | | Unit |
|--|-------------|-------------|-------------|----------------------|
| | MFC8020A | MFC8021A | MFC8022A | |
| Power Supply Voltage | 35 | 20 | 45 | Vdc |
| Power Dissipation | 1.0 | 1.0 | 1.0 | Watt |
| Derate above $T_A = +25^\circ\text{C}$ | 10 | 10 | 10 | mW/ $^\circ\text{C}$ |
| Peak Output Current (pins 5 & 8) | 150 | 150 | 150 | mA |
| Operating Temperature Range | -10 to +75 | -10 to +75 | -10 to +75 | $^\circ\text{C}$ |
| Storage Temperature Range | -55 to +125 | -55 to +125 | -55 to +125 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Value | Unit |
|----------------------|-------|---------------------------|
| Thermal Resistance | 100 | $^\circ\text{C}/\text{W}$ |
| Junction Temperature | 125 | $^\circ\text{C}$ |

FIGURE 1 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

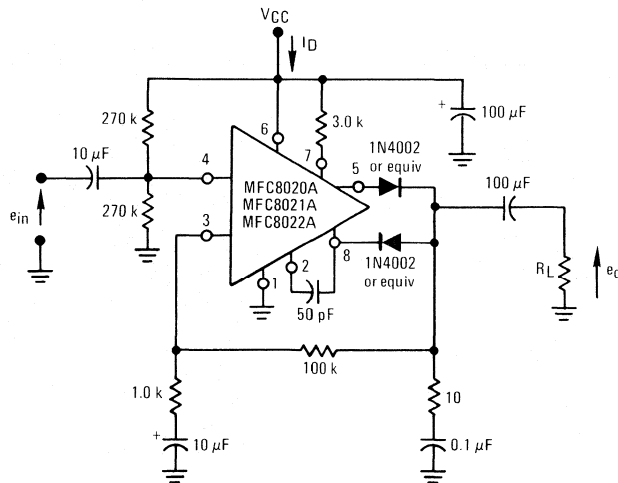
MFC8020A, MFC8021A, MFC8022A (continued)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted) (See Figure 2)

| Characteristic | | Min | Typ | Max | Unit |
|--|----------|-----|-----|-----|------|
| Drain Current (e _{in} = 0) | | | | | mA |
| V _{CC} = 30 Vdc | MFC8020A | — | 10 | 30 | |
| V _{CC} = 14 Vdc | MFC8021A | — | 7.0 | 30 | |
| V _{CC} = 40 Vdc | MFC8022A | — | 12 | 30 | |
| Sensitivity (P _O = 1.0 Watt, f = 1.0 kHz) | | | | | mV |
| e _o = 8.95 V(RMS), R _L = 165 Ω | MFC8020A | — | 89 | 112 | |
| e _o = 3.2 V(RMS), R _L = 65 Ω | MFC8021A | — | 32 | 40 | |
| e _o = 12.65 V(RMS), R _L = 165 Ω | MFC8022A | — | 126 | 160 | |
| Total Harmonic Distortion (f = 1.0 kHz) | | | | | % |
| V _{CC} = 30 V, e _o = 8.95 V(RMS), R _L = 165 Ω | MFC8020A | — | 0.7 | 5.0 | |
| V _{CC} = 14 V, e _o = 3.2 V(RMS), R _L = 65 Ω | MFC8021A | — | 1.0 | 5.0 | |
| V _{CC} = 40 V, e _o = 12.65 V(RMS), R _L = 165 Ω | MFC8022A | — | 1.5 | 5.0 | |
| Open-Loop Gain | | | | | dB |
| V _{CC} = 30 V, R _L = 165 Ω | MFC8020A | — | 89 | — | |
| V _{CC} = 14 V, R _L = 65 Ω | MFC8021A | — | 87 | — | |
| V _{CC} = 40 V, R _L = 165 Ω | MFC8022A | — | 90 | — | |
| Ripple Rejection | | | | | dB |
| f = 60 Hz, A _v = 100, e _{in} = 0, Power Supply Ripple = 1.0 V(RMS) | | — | 27 | — | |
| Equivalent Input Noise | | | | | μV |
| e _{in} = 0, R _S = 1.0 k Ω, BW = 100 Hz – 10 kHz | | — | 18 | — | |
| Quiescent Output Voltage (e _{in} = 0) | | | | | Vdc |
| V _{CC} = 30 V | MFC8020A | — | 15 | — | |
| V _{CC} = 14 V | MFC8021A | — | 7.0 | — | |
| V _{CC} = 40 V | MFC8022A | — | 20 | — | |

Symbols conform to JEDEC Bulletin No. 1 where applicable.

FIGURE 2 – TEST CIRCUIT



MFC8020A, MFC8021A, MFC8022A (continued)

TYPICAL AUTO RADIO AUDIO APPLICATION and CHARACTERISTICS
($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 3 – APPLICATION CIRCUIT FOR MFC8021A

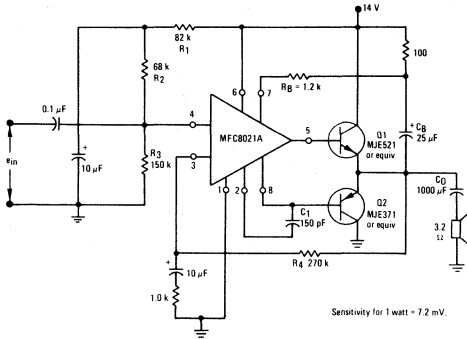


FIGURE 4 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER

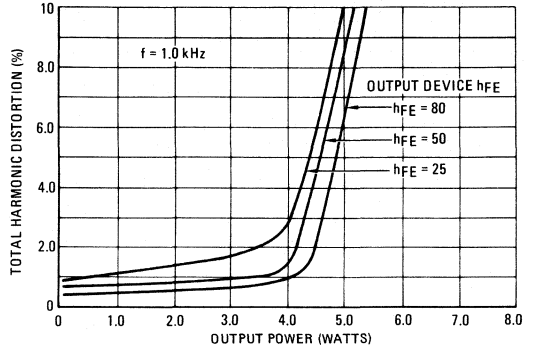


FIGURE 5 – TOTAL HARMONIC DISTORTION versus FREQUENCY

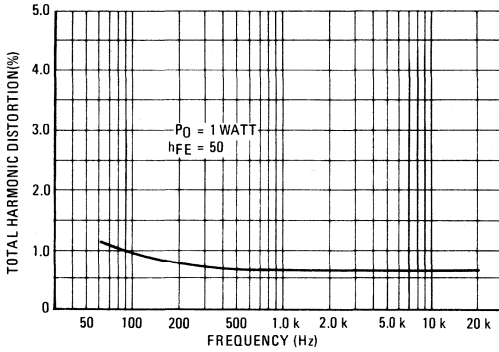
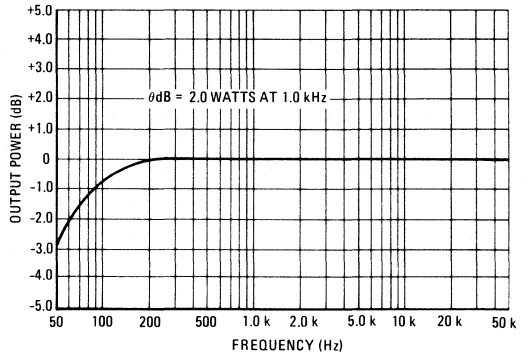


FIGURE 6 – FREQUENCY RESPONSE

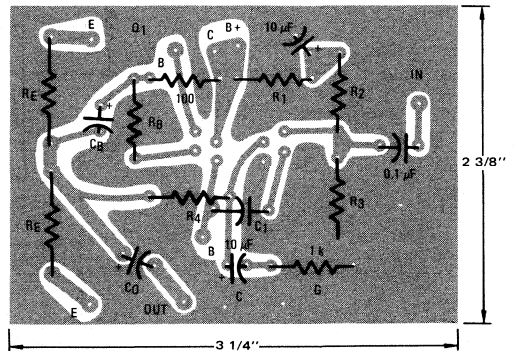


APPLICATIONS INFORMATION for MFC8021A
(AUTO RADIO AUDIO)

The MFC8021A combines all the voltage gain required for an automotive radio audio amplifier into one package reducing the circuit-board area requirement. The circuit shown in Figure 3 has an input sensitivity of approximately 7.2 millivolts for a one-watt output. Sensitivity can be adjusted by changing the value of R4. The circuit performance is a function of the output device h_{FE} , as shown in Figure 4. Figure 4 can be used to determine the minimum h_{FE} of the output transistors. The bandwidth of the amplifier is determined by the capacitor, C1. If C1 is increased to 390 pF the high frequency 3.0 dB point is typically 20 kHz.

An illustration of the copper side of the printed-circuit board layout is shown in Figure 7. The output transistors are mounted on the heatsink which for auto radio audio applications should have a maximum thermal resistance of 18°C/W for each device or 9.0°C/W when both output transistors are mounted on the same heatsink.

FIGURE 7 – PRINTED CIRCUIT BOARD for AUTOMOTIVE RADIO AUDIO 10-and-20 WATT AMPLIFIERS (COPPER SIDE)



MFC8020A, MFC8021A, MFC8022A (continued)

TYPICAL 10-and-20 WATT AMPLIFIER APPLICATION AND CHARACTERISTICS

($T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

FIGURE 8 – APPLICATION CIRCUIT for MFC8020A/and MFC8022A

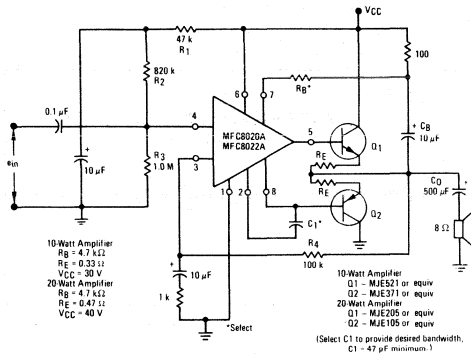


FIGURE 9 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER

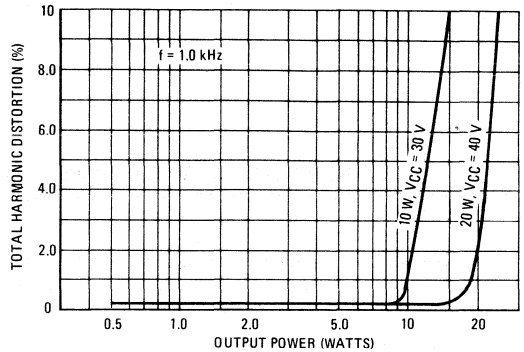


FIGURE 10 – TOTAL HARMONIC DISTORTION versus FREQUENCY

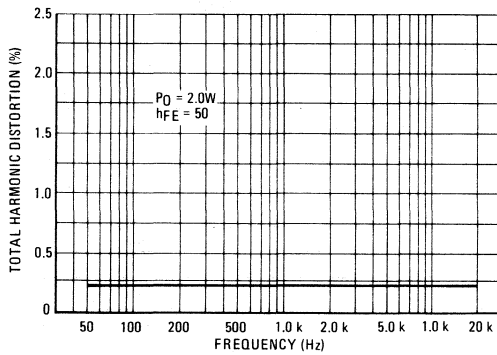
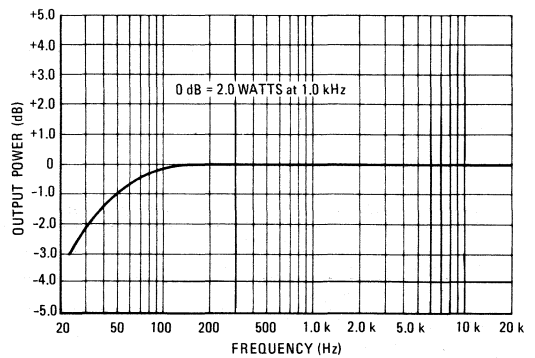


FIGURE 11 – FREQUENCY RESPONSE



APPLICATIONS INFORMATION for MFC8020A and MFC8022A (10-Watt and 20-Watt Amplifiers)

The MFC8020A and MFC8022A are high-voltage parts capable of driving 10-to-20 watt audio amplifiers. The gain of the circuit shown in Figure 8 changes when the value of R_4 is varied and the bandwidth is determined by C_1 . Emitter resistors are required at the higher voltages used for 10-to-20 watt audio amplifiers to provide thermal stability. The value of R_E is a function of the heatsink thermal resistance and supply voltage. The heatsink requirements for operation at $+65^{\circ}\text{C}$ (with both devices mounted on the same heatsink) is about $14^{\circ}\text{C}/\text{W}$ for the 10-watt amplifier and $8.0^{\circ}\text{C}/\text{W}$ for the 20-watt amplifier. If the maximum ambient operating temperature is reduced then the heatsink can be reduced in size as calculated by

$$\theta_{SA} = \frac{T_J - (\theta_{JS}) P_D - T_A}{P_D}$$

where

θ_{SA} = Heatsink thermal resistance

T_J = Maximum junction operating temperature

θ_{JS} = Junction to heatsink thermal resistance (includes all surface interface components for thermal resistance such as the insulating washer)

P_D = Maximum power dissipation of transistors (This occurs at about 60% of maximum output power) 6.0 W for 10 W, 7.2 W for 12 W

T_A = Maximum ambient temperature

The printed circuit board layout is shown in Figure 7.

MFC8030

HIGH FREQUENCY CIRCUIT

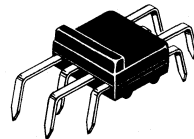
DIFFERENTIAL/CASCODE AMPLIFIER

... designed for applications requiring differential or cascode amplifiers.

- Extremely Flexible Amplifier
- Diode Available for Biasing
- Economical 8-Staggered Lead Package

DIFFERENTIAL/CASCODE AMPLIFIER

Silicon Monolithic
Functional Circuit

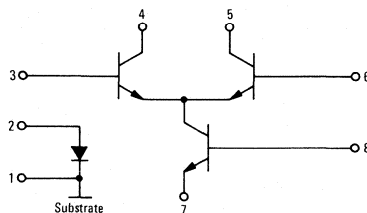


CASE 644A
PLASTIC PACKAGE

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|-----------------|------------|----------------------|
| Power Supply Voltage | V^+ | 20 | Vdc |
| Differential Input Voltage | V_{in} | ± 5.0 | Vdc |
| Power Dissipation @ $T_A = 25^\circ\text{C}$ (Package Limitation) | P_D | 1.0 | Watt |
| Derate above 25°C | $1/\theta_{JA}$ | 10 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -10 to +75 | $^\circ\text{C}$ |

FIGURE 1 - CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MFC8040

AUDIO PREAMPLIFIER

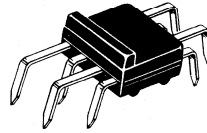
LOW NOISE AUDIO PREAMPLIFIER

... designed for high-gain, low-noise applications.

- Special Monolithic "State-of-the-Art" Process to Insure Low Noise - 1.0 μV (Typ)
- Can be Externally Equalized for NAB, RIAA
- Low Distortion - 0.1% (Typ) @ $A_V = 100$
- Large Dynamic Range - 7.0 V(rms) Out
- Low Output Impedance - 100 Ohms (Max)

LOW NOISE AUDIO PREAMPLIFIER

Silicon Monolithic Functional Circuit

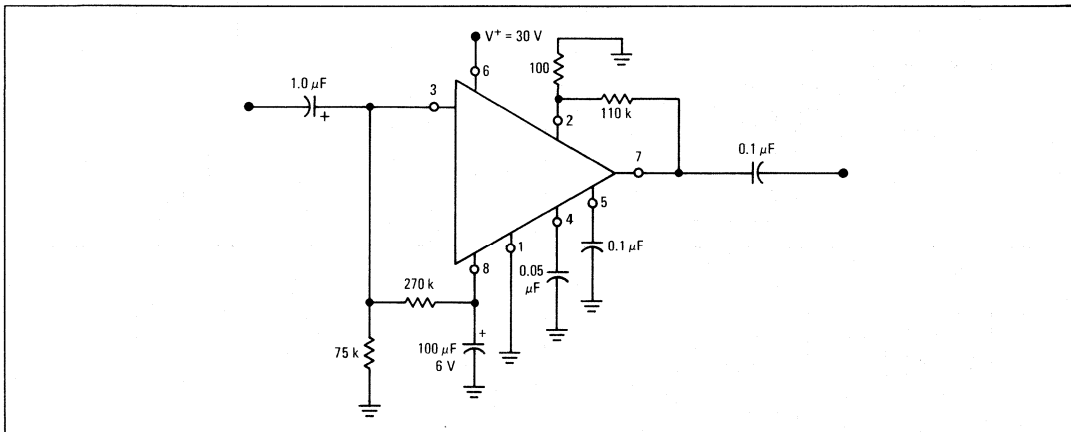


CASE 644A
PLASTIC PACKAGE

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|-----------------|------------|----------------------|
| Power Supply Voltage | V^+ | 33 | Vdc |
| Power Dissipation @ $T_A = 25^\circ\text{C}$ (Package Limitation) | P_D | 1.0 | Watt |
| Derate above $T_A = 25^\circ\text{C}$ | $1/\theta_{JA}$ | 10 | mW/ $^\circ\text{C}$ |
| Operating Temperature Range | T_A | -10 to +75 | $^\circ\text{C}$ |

FIGURE 1 - TYPICAL WIDEBAND AMPLIFIER CIRCUIT ($A_V = 60 \text{ dB}$)



See Packaging Information Section for outline dimensions.

MFC8040 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Circuit | Characteristic | Symbol | Min | Typ | Max | Unit |
|---------|---|-----------|-----|------|------|---------------------|
| | Drain Current | I_D | — | 8.0 | 12 | mA |
| | Total Harmonic Distortion ($v_o = 1.0\text{ V}$, $f = 1.0\text{ kHz}$) | THD | — | <0.1 | 0.25 | % |
| | Input Impedance | Z_{in} | — | 75 | — | k ohms |
| | Output Impedance | Z_{out} | — | 100 | — | ohms |
| | Open Loop Voltage Gain ($v_{in} = 100\mu\text{V(rms)}$ @ $f = 1.0\text{ kHz}$) | A_{VOL} | 80 | — | — | dB |
| | Wideband Input Noise (-3.0 dB Bandwidth, 10 Hz to 16 kHz, $A_V = 60\text{ dB}$ @ 1.0 kHz, $e_n = \frac{e_o}{A_V}$) | e_n | — | 1.0 | 3.0 | $\mu\text{V (rms)}$ |

FIGURE 2 – CIRCUIT SCHEMATIC

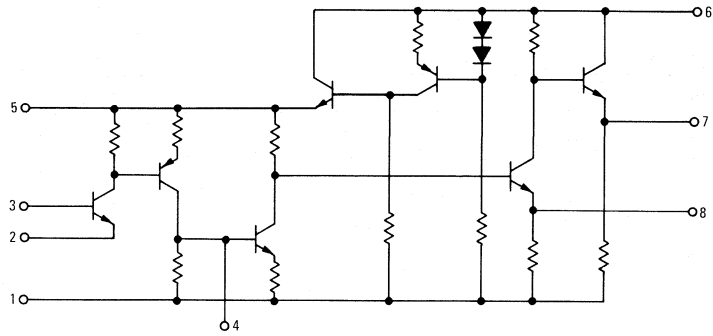


FIGURE 3 – INPUT NOISE

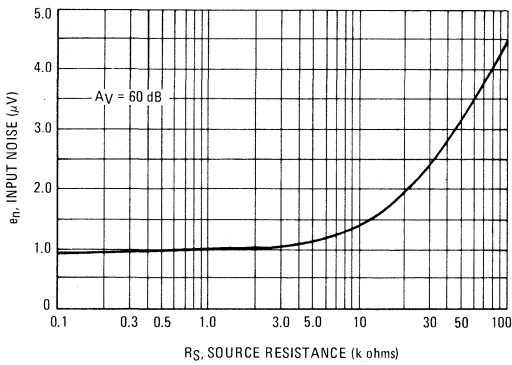


FIGURE 4 – OPEN LOOP TOTAL HARMONIC DISTORTION

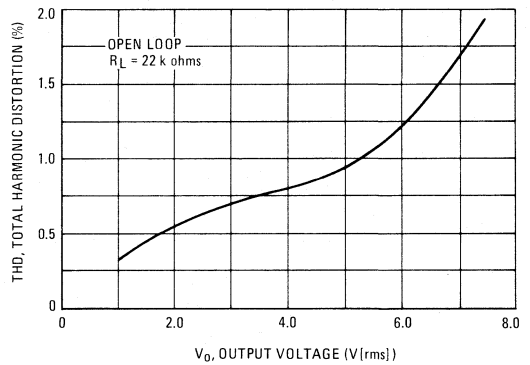
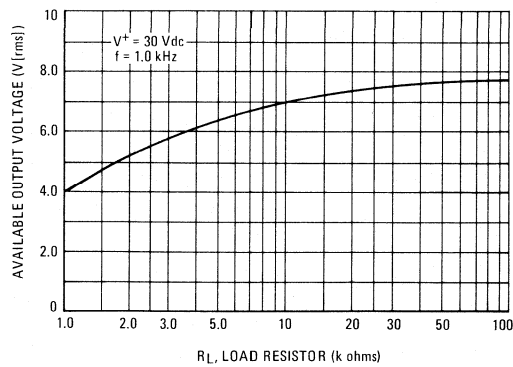


FIGURE 5 – AVAILABLE OUTPUT VOLTAGE



7

MFC8050

J-K FLIP FLOP

J-K FLIP-FLOP

... designed for use in high-level, low-speed logic and timing systems.

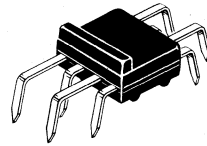
- Wide Operating Voltage Range – 4.0 to 16 Volts
- Regulated Supply Not Required
- Compatible with TTL and DTL
- J and K Inputs Allow Control of Desired State
- Direct Clear (C_D) Allows Reset to Zero at Any Time

J-K FLIP-FLOP

Silicon Monolithic
Functional Circuit

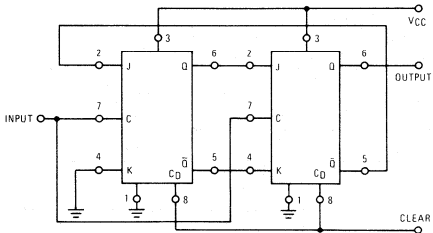
MAXIMUM RATINGS

| Rating | Symbol | Value | Volts |
|--|-------------------------------------|------------|---------------|
| Power Supply Voltage | V _{CC} | 19 | Vdc |
| Output Sinking Current | I _{sink} | 10 | mA |
| Negative Input Voltage | V _{in} | 0.5 | Vdc |
| Power Dissipation @ T _A = 25°C Derate above 25°C | P _D 1/θ _{JA} | 1.0 10 | Watt mW/°C |
| Operating Temperature Range | T _A | -10 to +75 | °C |

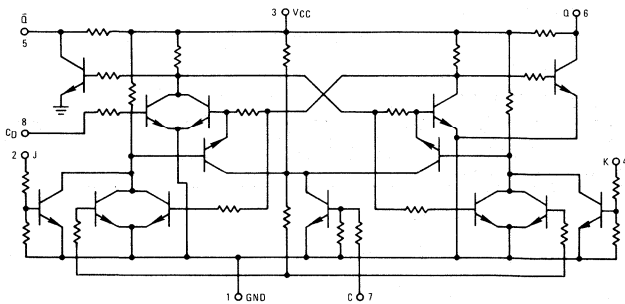


CASE 644A

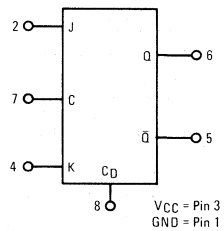
TYPICAL APPLICATION – DIVIDE BY 3 CIRCUIT



CIRCUIT SCHEMATIC



BLOCK DIAGRAM



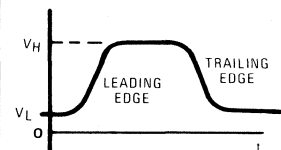
See Packaging Information Section for outline dimensions.

MFC8050 (continued)

ELECTRICAL CHARACTERISTICS (V_{in} = 4.0 V, Square Pulse, f = 10 kHz, 50% Duty Cycle, t_f = 1.0 V/μs (Min), T_A = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-------------------|-------------|--------|------------|------|
| Operating Power Supply Voltage | V _{CC} | 4.0 | — | 16 | Vdc |
| Toggle Frequency | f _{Tog} | — | 3.0 | — | MHz |
| Output Voltage (High) (V _{CC} = 4.0 Vdc) (V _{CC} = 16 Vdc) | V _{OH} | 3.5 15.5 | — — | — — | Vdc |
| Output Voltage (Low) (V _{CC} = 4.0 Vdc) (V _{CC} = 16 Vdc) | V _{OL} | — — | — — | 0.5 1.0 | Vdc |
| Operating Drain Current | I _D | — | — | 20 | mAdc |
| Output Sinking Current (V _O ≤ 1.0 Vdc) | I _{sink} | — | 5.0 | — | mAdc |
| Rise Time | t _r | — | 250 | — | ns |
| Storage Time | t _s | — | 350 | — | ns |
| Fall Time | t _f | — | 60 | — | ns |
| Input Resistance | R _{in} | 10 | — | — | kΩ |
| Output Resistance (Output High) | R _{OH} | — | — | 2.8 | kΩ |

INPUT PULSE REQUIREMENTS

|  | Characteristic | Symbol | Min | Max | Unit | |
|---|-----------------|-----------------|------|------|------|------------------------------------|
| | Pulse Magnitude | V _H | +4.0 | — | — | Volts |
| | Zero Level | V _L | — | +1.0 | — | Volts |
| | Leading Edge | No Requirement | | | | |
| | Trailing Edge | $\frac{dv}{dt}$ | -1.0 | — | — | $\frac{\text{Volts}}{\mu\text{s}}$ |

TRUTH TABLE

| t _n | | t _{n+1} | | Explanation |
|----------------|---|------------------|----------------|--|
| J | K | \overline{Q} | \overline{Q} | |
| 1 | 1 | \overline{Q}_n | Q _n | No change in output |
| 1 | 0 | 1 | 0 | Set to Q = 1 state regardless of previous history |
| 0 | 1 | 0 | 1 | Set to \overline{Q} = 1 state regardless of previous history |
| 0 | 0 | \overline{Q}_n | Q _n | Output reverses (toggle action) |

t_n = time period just before and during the negative transition of the clock pulse (Pin 5).
t_{n+1} = the time subsequent to that transition.
Q_n = state of the Q output in time period t_n.

ZERO VOLTAGE SWITCH

MFC8070

ZERO VOLTAGE SWITCH

... designed for use in ac power switching applications with output drive capable of triggering triacs. Other operational features include:

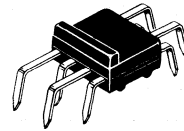
- A built-in voltage regulator that allows direct ac line operation
- A differential input with dual sensor inputs capable of testing the condition of two external sensors and controlling the gate pulse to a triac accordingly. Hysteresis or proportional control to this section may be added if desired.
- Sensor input "open and short" protection. This insures that the triac will never be turned "on" if either of the sensors are shorted or opened.
- A zero crossing detector that synchronizes the triac gate pulses with the zero crossing of the ac line voltage. This eliminates radio frequency interference (rfi) when used with resistive loads.

Typical Applications Include:

- Heater Controls
- Valve Control
- Photo Controls
- ON-OFF Power Controls
- Threshold Detector
- Relay Driver
- Lamp Driver
- Flasher Control

ZERO VOLTAGE SWITCH

Silicon Monolithic
Functional Circuit



PLASTIC PACKAGE
CASE 644A

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|-------------------------------------|-------------|-----------------|
| DC Voltage | V ₅₋₈ | 15 | V _{dc} |
| DC Voltage | V ₄₋₈ | 15 | V _{dc} |
| DC Voltage | V ₇₋₈ | 15 | V _{dc} |
| Power Dissipation @ T _A = 25°C Derate above 25°C | P _D 1/θ _{JA} | 1.0 10 | Watt mW/°C |
| Operating Temperature Range | T _A | -10 to +75 | °C |
| Storage Temperature Range | T _{stg} | -55 to +150 | °C |

See Packaging Information Section for outline dimensions.

MFC8070(continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| | Characteristic | Symbol | Min | Typ | Max | Unit | |
|--|---|------------------|---------------------------|--------------------------|---------------------------|---------------|---------------|
| | V_S with Inhibit Output (Sw. 1: A or B) | V_{SI} | — | 9.0 | 11 | Vdc | |
| | Output Leakage (Sw. 1: A or B) | I_{OL} | — | 5.0 | 100 | μA | |
| | Input Current 1 (Sw. 1: A) | I_1 | — | 5.0 | 15 | μA | |
| | Input Current 2 (Sw. 1: B) | I_2 | — | 5.0 | 15 | μA | |
| | Inhibit Threshold (Sw. 1: A or B) | V_{TI} | $V_{ref} + 100\text{ mV}$ | $V_{ref} + 10\text{ mV}$ | — | — | Vdc |
| | V_S with Pulse Output (Sw. 1: A or B) | V_{SP} | 6.0 | 8.5 | — | Vdc | |
| | Peak Output Current (Sw. 1: A or B) | I_{OP} | 50 | — | — | mA | |
| | Pulse Threshold (Sw. 1: A or B) | V_{TP} | — | $V_{ref} - 10\text{ mV}$ | $V_{ref} - 100\text{ mV}$ | — | Vdc |
| | Output Pulse Width (Sw. 1: A or B) (See Figure 1) | τ_A, τ_B | — | 70 | — | — | μs |
| | Input Short Protection (Sw. 1: A; Sw. 2: B) | I_{OS} | — | 5.0 | 100 | μA | |
| | Input Short Protection (Sw. 1: B; Sw. 2: A) | I_{OS} | — | 5.0 | 100 | μA | |

FIGURE 1 – OUTPUT PULSE DEFINITION

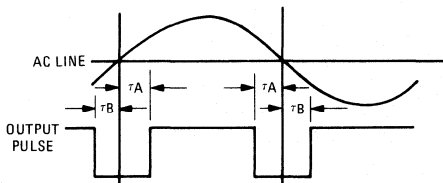
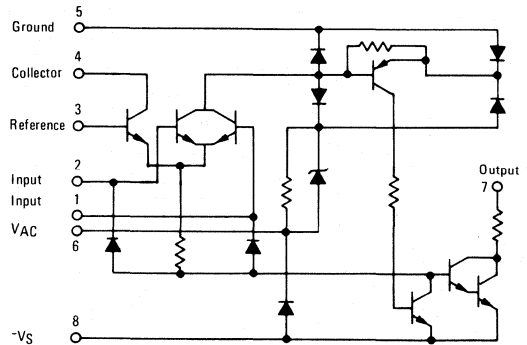


FIGURE 2 – CIRCUIT SCHEMATIC



7

MFC8070 (continued)

FIGURE 3 – CIRCUIT FOR MEASURING OUTPUT PULSE WIDTH versus SOURCE RESISTANCE

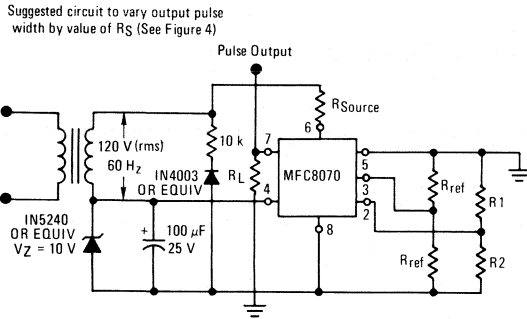
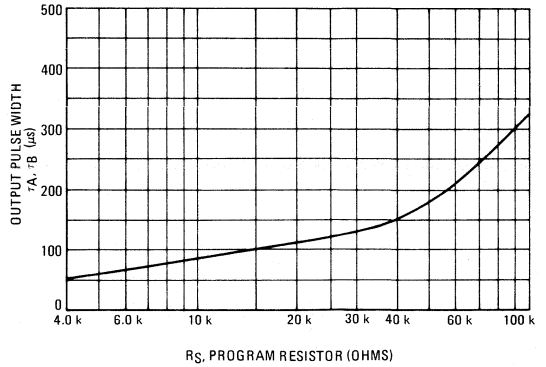
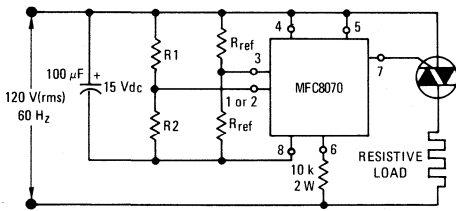


FIGURE 4 – OUTPUT PULSE WIDTH versus SOURCE RESISTANCE



TYPICAL ZERO VOLTAGE SWITCH APPLICATIONS FOR TRIAC CONTROL

FIGURE 5 – TRIAC CONTROL CIRCUIT

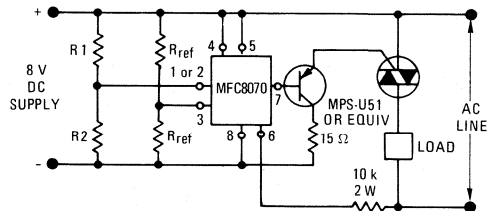


Basic triac trigger circuit utilizing the zero crossing detector and the input comparator to control the gate of the triac.

R_1 is an external sensor

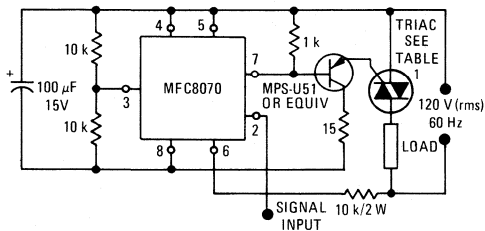
R_2 must be the external sensor for the internal short and open protection to be operative.

FIGURE 6 – TRIAC CONTROL CIRCUIT WITH CURRENT BOOST UTILIZING DC SUPPLY



Basic DC trigger application using the input comparator to control a PNP capable of furnishing gate drive of approximately 0.5 Amp.

FIGURE 7 – TRIAC CONTROL CIRCUIT WITH CURRENT BOOST UTILIZING AC SUPPLY



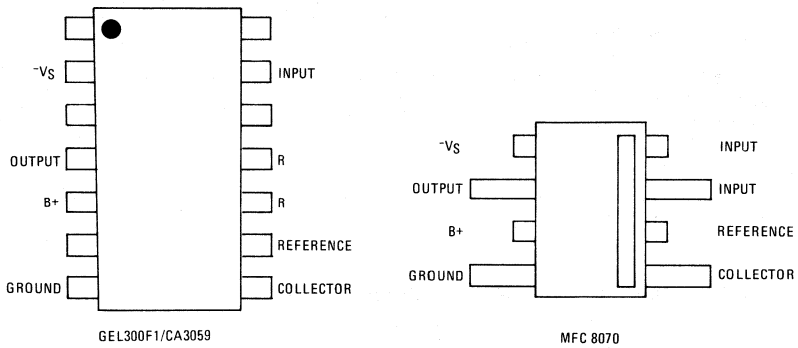
Zero crossing triac control circuit for gate current requirements greater than 50 mA.

Recommended Motorola triacs for use in circuit.

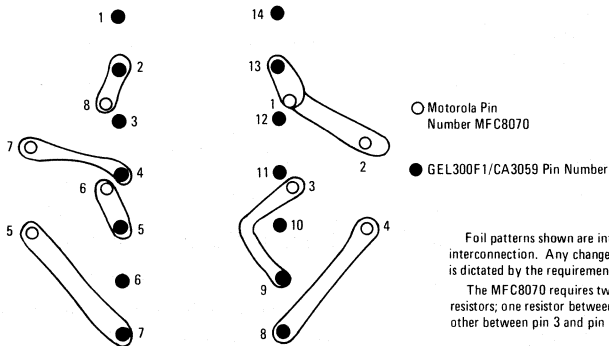
| Maximum Continuous (Current (Amp [rms]) | Triac Family | Case No. |
|--|-----------------------------|--------------|
| 10 | 2N6151/2N6153 (MAC 10) | 90 (Plastic) |
| 10 | 2N6139/2N6144 (MAC 1, 2, 3) | 85, 86, 87L |
| 30 | 2N6157/2N6165 (MAC 35, 36) | 174, 175 |

MFC8070(continued)

PIN COMPARISON OF MFC8070 AND GEL300F1 (PA424)/CA3059



COMPATIBLE PRINTED CIRCUIT FOIL PATTERN FOR MFC8070 FOR MFC8070, GEL300F1 (PA424) AND CA3059



Foil patterns shown are intended to show pin-for-pin interconnection. Any change in the number of components is dictated by the requirements of the individual design.

The MFC8070 requires two external reference resistors; one resistor between pin 3 and 5 and the other between pin 3 and pin 8.

MFC9020

AUDIO AMPLIFIER

2-WATT AUDIO AMPLIFIER

... designed to provide the complete audio system in television, radio and phonograph equipment.

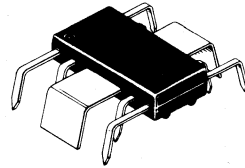
- 2-Watts Continuous Sine Wave Power
- Minimal Heat-Sinking Required for Operation @ $T_A = 55^\circ\text{C}$
- Short Circuit Proof (Short-Term)
- High Gain – 200 mV for 2-Watts Output Power
- High Input Impedance – 500 k Ohms

2-WATT AUDIO AMPLIFIER

Silicon Monolithic Functional Circuit

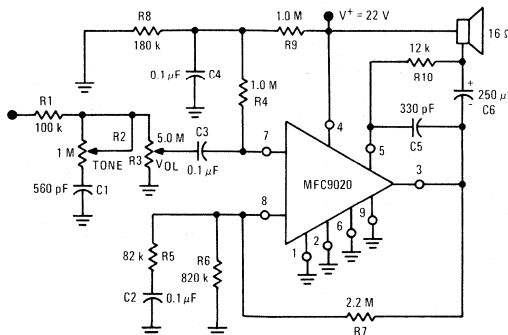
| MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted) | | | |
|---|---------------|-----------|--|
| Rating | Symbol | Value | Unit |
| Power Supply Voltage | V^+ | 24 | Vdc |
| Output Peak Current | I_p | 1.05 | Amperes |
| Maximum Power Output $T_A = 55^\circ\text{C}$ (Free Air Mounting) | P_o | 2.0 | Watts |
| THERMAL CHARACTERISTICS | | | |
| Characteristic | Symbol | Max | Unit |
| Thermal Resistance (Junction to Tab) Derate above 25°C | θ_{JC} | 10 100 | $^\circ\text{C/W}$ $\text{mW}/^\circ\text{C}$ |
| Thermal Resistance (Junction to Ambient) (1) Derate above 25°C | θ_{JA} | 60 8.0 | $^\circ\text{C/W}$ $\text{mW}/^\circ\text{C}$ |

(1) Thermal resistance is measured in still air with fine wires connected to the leads, representing the "worst case" situation.
For a larger power requirement, the tab (pin 9) must be soldered to at least one square inch (effective area) of copper foil on the printed circuit board. The θ_{JA} will be no greater than $+45^\circ\text{C/W}$. Thus, 2.0 Watts of audio power is allowable under "worst case" conditions at an ambient temperature of $+65^\circ\text{C}$, which must be linearly derated at $22.2 \text{ mW}/^\circ\text{C}$ from $+65^\circ\text{C}$ to $+150^\circ\text{C}$.



CASE 641 PLASTIC PACKAGE

FIGURE 1 – TYPICAL CIRCUIT APPLICATION



See Packaging Information Section for outline dimensions.

ELECTRICAL CHARACTERISTICS ($V^+ = 22 \text{ Vdc}$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

| Circuit | Characteristic | Symbol | Min | Typ | Max | Unit | |
|---------|---|----------|-----|-----|-----|------|----|
| | Quiescent Output Voltage | V_O | — | 10 | — | Vdc | |
| | Quiescent Drain Current ($e_{in} = 0$) | I_D | — | 12 | 20 | mA | |
| | Sensitivity Input Voltage ($e_o = 4.0 \text{ V(rms)}$ @ 1.0 kHz, $P_o = 2.0 \text{ W}$) | e_{in} | — | — | 200 | — | mV |
| | Total Harmonic Distortion ($P_o = 2.0 \text{ W}$, 1.0 kHz) ($P_o = 100 \text{ mW}$, 1.0 kHz) | THD | — | — | 1.0 | 10 | % |
| | Hum and Noise * | | — | — | -40 | — | dB |

* IHF STANDARD IHF-A-201 1966

Performance Curves for Circuit Shown Above.

FIGURE 2 – TOTAL HARMONIC DISTORTION

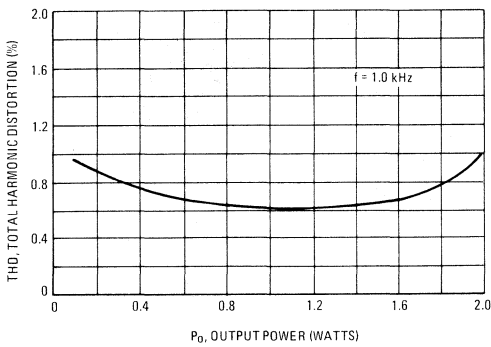


FIGURE 3 – POWER DISSIPATION

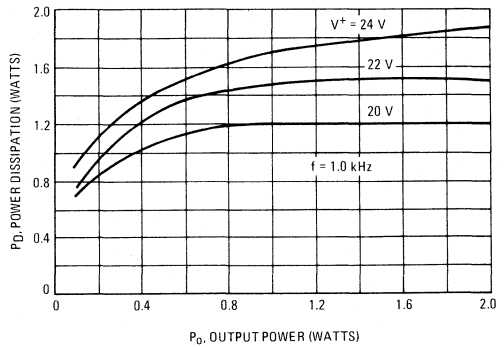


FIGURE 4 – TOTAL HARMONIC DISTORTION

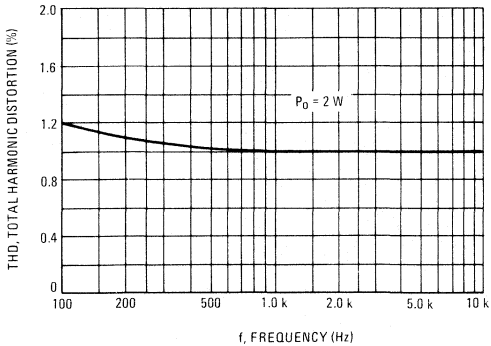
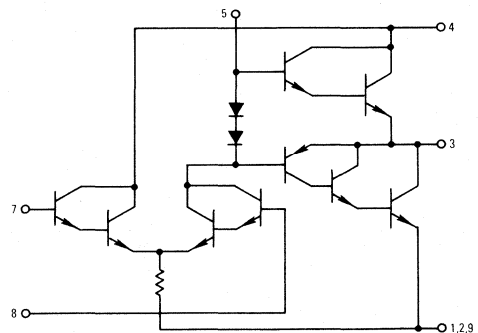


FIGURE 5 – CIRCUIT SCHEMATIC



Applications Information for Circuit Shown in Figure 1.

Figures 7 thru 11 pertain to the 2-watt amplifier with a 16-ohm load connected to V^+ as shown in Figure 1. The sensitivity of this amplifier is approximately 250 mV and the input impedance at 100 Hz is approximately 800 k ohms. $R7/R5$ determines the approximate gain that can be best altered by changing the value of $R5$ and holding $R7$ to a large value. This allows the use of a smaller and less expensive capacitor for $C2$.

The speaker can also be connected to ground as shown in Figure 6, and the printed circuit board art work is shown in Figure 13.

The maximum operation voltage for the amplifier should reflect a consideration of at least a 10% high-line condition. Under high-line conditions, the power supply voltage should be less than the maximum rating of the device.

FIGURE 6 – ALTERNATE SPEAKER CONNECTION FOR SPEAKER TO GROUND

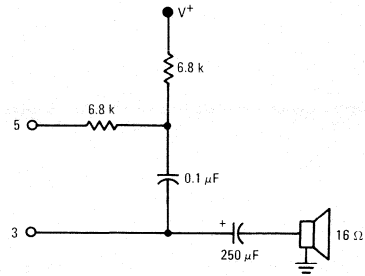


FIGURE 7 – TOTAL HARMONIC DISTORTION

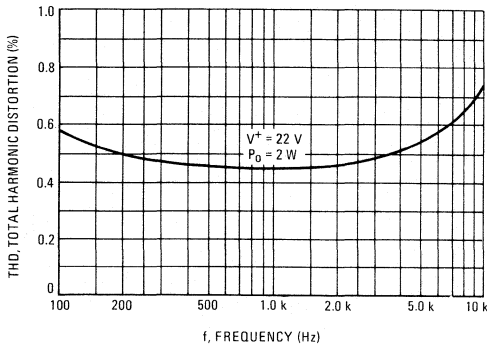


FIGURE 8 – POWER DISSIPATION

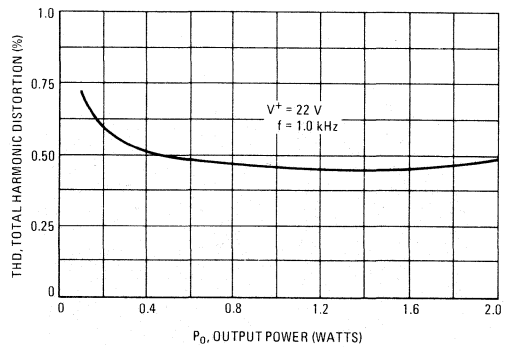


FIGURE 9 – FREQUENCY RESPONSE

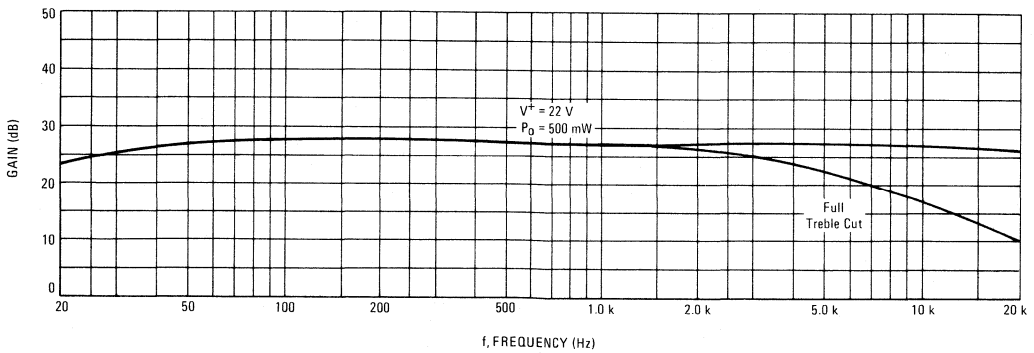


FIGURE 10 – PRINTED CIRCUIT BOARD
1:1 PATTERN (Speaker to V⁺)

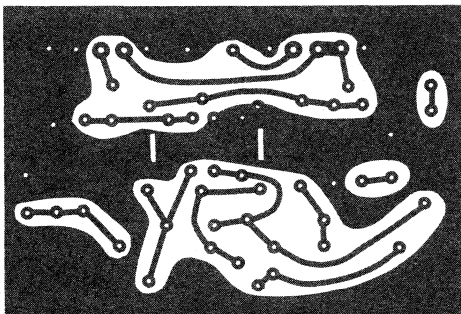


FIGURE 11 – COMPONENT DIAGRAM FOR FIGURE 10

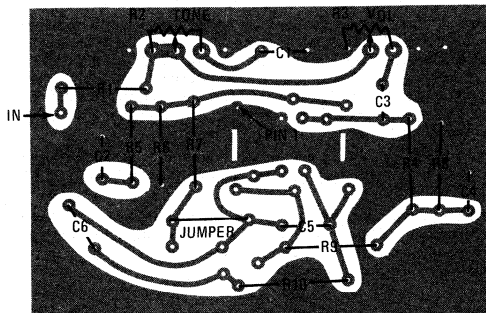


FIGURE 12 – COMPLETED BOARD
(Speaker to V⁺)

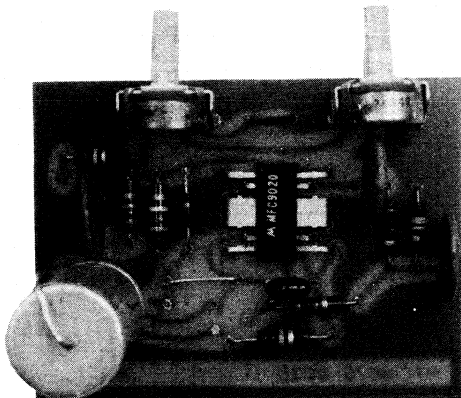
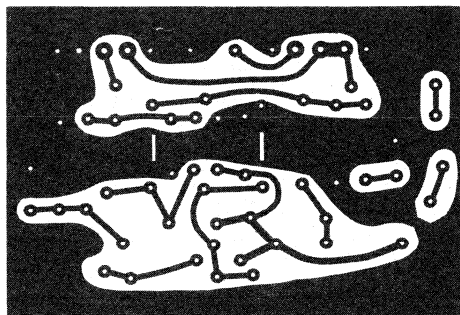


FIGURE 13 – PRINTED CIRCUIT BOARD
1:1 PATTERN (Speaker to Ground)



MHP401

MOS CLOCK DRIVER

TTL TO MOS CLOCK DRIVER HYBRID CIRCUIT

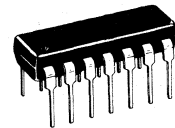
... designed for medium to high capacitive loads.

- High Operating Voltage – $V_2 - V_1 = 32$ Vdc (Max)
- High Clock Rates – 5.0 MHz (Max)
- Fast Switching Times – (Typ)

| C _L pF | R _S Ohms | t _{PLH} ns | t _{TLH} ns | t _{PHL} ns | t _{THL} ns |
|----------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| 500 | 0 | 10 | 30 | 21 | 28 |
| 1000 | 5.0 | 13 | 40 | 23 | 35 |
| 2000 | 10 | 19 | 67 | 28 | 69 |

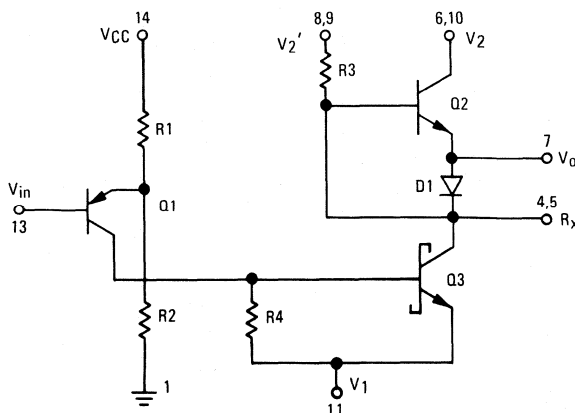
MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|---------------|-------------|-------------------------------|
| Operating Voltage | $V_2 - V_1$ | 32 | Vdc |
| Negative Supply Voltage | V_1 | -3.0 to -32 | Vdc |
| Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 2.0 44 | Watts mW/ $^\circ\text{C}$ |
| Operating Junction Temperature Range | T_J | 0 to +70 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -55 to +150 | $^\circ\text{C}$ |
| Thermal Resistance, Junction to Ambient | θ_{JA} | 0.022 | $^\circ\text{C}/\text{mW}$ |

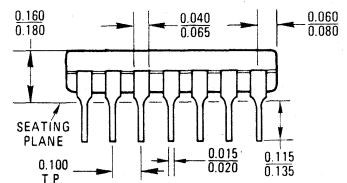
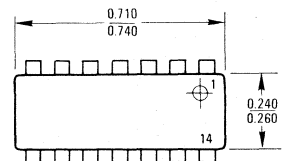
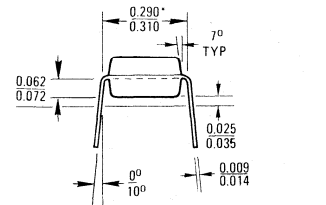


TTL to MOS CLOCK DRIVER HYBRID CIRCUIT

CIRCUIT SCHEMATIC



Pins 2, 3 and 12 are connected internally and must be electrically isolated.



*Dimension is to lead centerline when formed parallel.

CASE 646

MHP401 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

All pins not characterized on this table must be electrically open and isolated from each other for each test, Pin 1 is grounded for all tests.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

STATIC CHARACTERISTICS (V_{CC} = 5.25 Vdc, V₁ = -29 Vdc)

| | | | | | |
|--|------------------|---|---|-----|----|
| Input Forward Current (1) (V _{in} = 0.4 Vdc) | I _{IL} | — | — | 1.6 | mA |
| Input Leakage Current (1) (V _{in} = 5.5 Vdc) | I _{IH} | — | — | 100 | μA |
| Power Supply Drain Current (1) (V _{in} = 0.4 Vdc) (V _{in} = 2.4 Vdc) | I _{CCL} | — | — | 20 | mA |
| | I _{CCH} | — | — | 15 | |

DYNAMIC CHARACTERISTICS (V_{in} supplied by MC7400, V_{CC} = 5.0 Vdc, V₁ = -12 Vdc, V₂ = V₂' = +5.0 Vdc, C_L = 1000 pF, R_S = 5.0 Ohms, 2.0 Watts, Figure 1)

| | | | | | |
|--------------------------|----------------------------------|----|---|----|-----|
| Output Voltage Swing (2) | V _{OH} -V _{OL} | 15 | — | — | Vdc |
| Turn-On Time (2) | t _{on} | — | — | 75 | ns |
| Turn-Off Time (2) | t _{off} | — | — | 75 | ns |

SWITCHING TIMES (V_{in} supplied by MC7400, 1.0 MHz, 20%)

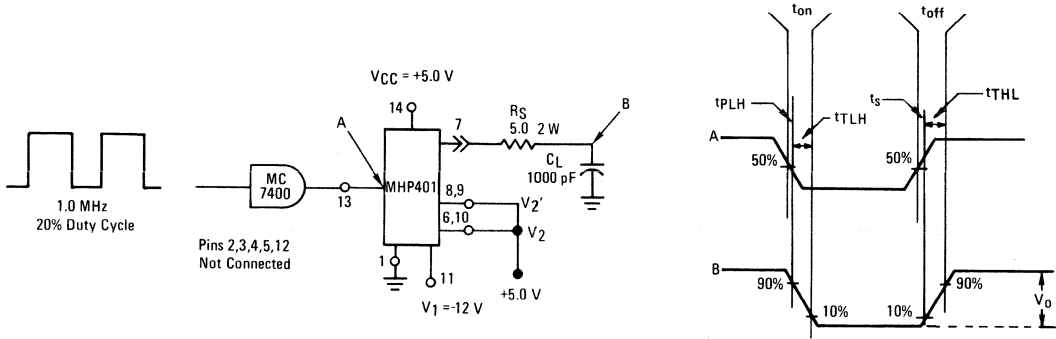
| | | | | | |
|---|------------------|---|----|---|----|
| Delay Time V ₁ = -12 Vdc, V ₂ = V ₂ ' = +5.0 Vdc (C _L = 500 pF, R _S = 0) (C _L = 1000 pF, R _S = 5.0 Ohms) (C _L = 2000 pF, R _S = 10 Ohms) V ₁ = -29 Vdc, V ₂ = V ₂ ' = Gnd (C _L = 500 pF, R _S = 0) (C _L = 1000 pF, R _S = 5.0 Ohms) (C _L = 2000 pF, R _S = 10 Ohms) | t _{PLH} | — | 10 | — | ns |
| | | — | 13 | — | |
| | | — | 19 | — | |
| | | — | 12 | — | |
| | | — | 16 | — | |
| | | — | 23 | — | |
| Rise Time V ₁ = -12 Vdc, V ₂ = V ₂ ' = +5.0 Vdc (C _L = 500 pF, R _S = 0) (C _L = 1000 pF, R _S = 5.0 Ohms) (C _L = 2000 pF, R _S = 10 Ohms) V ₁ = -29 Vdc, V ₂ = V ₂ ' = Gnd (C _L = 500 pF, R _S = 0) (C _L = 1000 pF, R _S = 5.0 Ohms) (C _L = 2000 pF, R _S = 10 Ohms) | t _{TLH} | — | 30 | — | ns |
| | | — | 40 | — | |
| | | — | 67 | — | |
| | | — | 41 | — | |
| | | — | 54 | — | |
| | | — | 89 | — | |
| Storage Time V ₁ = -12 Vdc, V ₂ = V ₂ ' = +5.0 Vdc (C _L = 500 pF, R _S = 0) (C _L = 1000 pF, R _S = 5.0 Ohms) (C _L = 2000 pF, R _S = 10 Ohms) V ₁ = -29 Vdc, V ₂ = V ₂ ' = Gnd (C _L = 500 pF, R _S = 0) (C _L = 1000 pF, R _S = 5.0 Ohms) (C _L = 2000 pF, R _S = 10 Ohms) | t _{PHL} | — | 21 | — | ns |
| | | — | 23 | — | |
| | | — | 28 | — | |
| | | — | 22 | — | |
| | | — | 25 | — | |
| | | — | 32 | — | |
| Fall Time V ₁ = -12 Vdc, V ₂ = V ₂ ' = +5.0 Vdc (C _L = 500 pF, R _S = 0) (C _L = 1000 pF, R _S = 5.0 Ohms) (C _L = 2000 pF, R _S = 10 Ohms) V ₁ = -29 Vdc, V ₂ = V ₂ ' = Gnd (C _L = 500 pF, R _S = 0) (C _L = 1000 pF, R _S = 5.0 Ohms) (C _L = 2000 pF, R _S = 10 Ohms) | t _{THL} | — | 28 | — | ns |
| | | — | 35 | — | |
| | | — | 69 | — | |
| | | — | 46 | — | |
| | | — | 49 | — | |
| | | — | 78 | — | |

(1) Pulse Test: Pulse Width < 50 ms.

(2) MC7400 used in test to be loaded with device under test only.

MHP401 (continued)

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



MAXIMUM OPERATING FREQUENCY

The following limits apply with the unit soldered to a printed circuit board and force air cooled at $T_A = 25^\circ\text{C}$.

$$V_2 - V_1 = 17 \text{ Vdc}$$

- @ 500 pF and 20% Duty Cycle
- @ 1000 pF and 20% Duty Cycle
- @ 2000 pF and 20% Duty Cycle

Maximum Frequency

- 5.0 MHz
- 4.0 MHz
- 2.0 MHz

$$V_2 - V_1 = 29 \text{ Vdc}$$

- @ 500 pF and 20% Duty Cycle
- @ 1000 pF and 20% Duty Cycle
- @ 2000 pF and 20% Duty Cycle

Maximum Frequency

- 3.0 MHz
- 1.5 MHz
- 1.0 MHz

OPERATING CHARACTERISTICS

For best performance, all leads of the MHP401 should be soldered to a printed circuit board or substrate. This results in better heat sinking.

Pins 2 and 3 may be common with each other, but must be electrically open and isolated from all other pins. Pin 12 must be electrically open and isolated from all other pins.

Three pairs of pins in this package are used in circuit operation: V_2' (Pins 8 and 9), V_2 (Pins 6 and 10) and R_x (Pins 4 and 5). Electrical connection to these points may be made at either pin or both. If electrical connection is made to only one pin of a pair, the other pin must be left electrically open and isolated and should be soldered to the substrate for heat sinking.

Series resistance (R_S) is for absorption of switching power . . . failure to use it for loads over 500 pF may result in package overheating.

$$R_S @ 1000 \text{ pF} = 5.0 \text{ ohms, 2.0 watts}$$

$$R_S @ 2000 \text{ pF} = 10 \text{ ohms, 2.0 watts}$$

DYNAMIC OPERATION

For dynamic operation, V_2' (Pins 8 and 9) is tied to V_2 (Pins 6 and 10) and R_x (Pins 4 and 5) is left electrically open and isolated. If desired, V_2' (Pins 8 and 9) may be left electrically open and isolated and an external 2.0 watt resistor to replace R_3 may be tied from R_x (Pins 4 and 5) to V_2 (Pins 6 and 10).

For $V_2 - V_1 < 20 \text{ V}$, the maximum duty cycle is 50%; at $V_2 - V_1 = 20 \text{ to } 30 \text{ V}$, the maximum duty cycle is 20%. By replacing R_3 with a 2.0-watt, 500-ohm resistor, the circuit may be operated in a static mode if the following conditions exist:

$$V_1 \leq -13 \text{ V and } V_2 - V_1 \leq 30 \text{ V}$$

Or, R_3 may be replaced with a 2.0-watt resistor less than 500 ohms to speed fall time.

**MLM101A
MLM201A
MLM301A**

MONOLITHIC OPERATIONAL AMPLIFIER

The MLM101A, MLM201A, and MLM301A are functionally, electrically, and pin-for-pin equivalent to the LM101A, LM201A, and LM301A respectively.

- Low Input Offset Current – 20 nA maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short-Circuit Protection
- Guaranteed Drift Characteristics

OPERATIONAL AMPLIFIER

MONOLITHIC SILICON
INTEGRATED CIRCUIT

**G SUFFIX
METAL PACKAGE
CASE 601
(TO-99)**



Case connected to pin 4 through substrate

**P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MLM301A Only)**

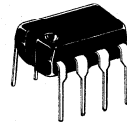


FIGURE 1 – STANDARD COMPENSATING AND OFFSET BALANCING CIRCUIT

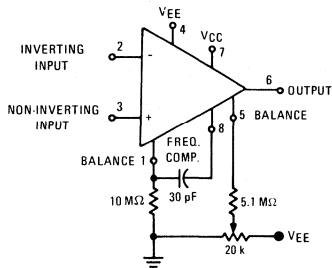


FIGURE 2 – DOUBLE-ENDED LIMIT DETECTOR

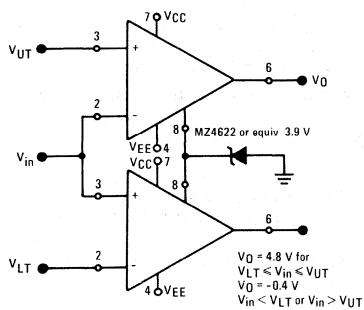
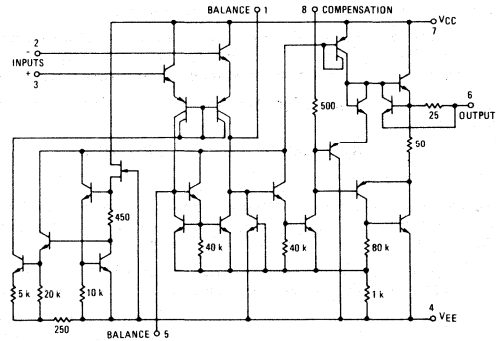


FIGURE 3 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions.

MLM101A, MLM201A, MLM301A (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol* | VALUE | | | Unit |
|---|-----------------------------------|-----------------|------------|----------|----------------------------|
| | | MLM101A | MLM201A | MLM301A | |
| Power Supply Voltage | V _{CC} , V _{EE} | ±22 | ±22 | ±18 | Vdc |
| Differential Input Voltage | V _{in} | ← ±30 → | | | Volts |
| Common-Mode Input Swing (Note 1) | V _{ICR} | ← ±15 → | | | Volts |
| Output Short Circuit Duration | t _S | ← Continuous → | | | |
| Power Dissipation (Package Limitation) | P _D | ← 500 → | | | mW mW/°C mW mW/°C |
| Metal Can | | ← 6.8 → | | | |
| Derate above T _A = +75°C | | - | | | |
| Plastic Dual In-Line Package (MLM301A only) | | - | | | |
| Operating Temperature Range | T _A | -55 to +125 | -25 to +85 | 0 to +75 | °C |
| Storage Temperature Range | T _{stg} | ← -65 to +150 → | | | °C |

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the MLM101A and MLM201A, and from ±5.0 V to ±15 V for the MLM301A.

| Characteristics | Symbol* | MLM101A MLM201A | | | MLM301A | | | Unit |
|--|-----------------|--------------------|-----|-----|---------|-----|-----|---------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage (R _S ≤ 50 kΩ) | V _{IO} | - | 0.7 | 2.0 | - | 2.0 | 7.5 | mV |
| Input Offset Current | I _{IO} | - | 1.5 | 10 | - | 3.0 | 50 | nA |
| Input Bias Current | I _{IB} | - | 30 | 75 | - | 70 | 250 | nA |
| Input Resistance | R _{in} | 1.5 | 4.0 | - | 0.5 | 2.0 | - | Megohms |
| Supply Current V _S = ±20 V V _S = ±15 V | I _D | - | 1.8 | 3.0 | - | 1.8 | 3.0 | mA |
| Large Signal Voltage Gain V _S = ±15 V, V _O = ±10 V, R _L > 2.0 kΩ | A _V | 50 | 160 | - | 25 | 160 | - | V/mV |

The following specifications apply over the operating temperature range.

| | | | | | | | | |
|--|----------------------|------------|--------------|------------|------------|--------------|------------|-------|
| Input Offset Voltage (R _S ≤ 50 kΩ) | V _{IO} | - | - | 3.0 | - | - | 10 | mV |
| Input Offset Current | I _{IO} | - | - | 20 | - | - | 70 | nA |
| Average Temperature Coefficient of Input Offset Voltage T _A (min) ≤ T _A ≤ T _A (max) | ΔV _{IO} /ΔT | - | 3.0 | 15 | - | 6.0 | 30 | μV/°C |
| Average Temperature Coefficient of Input Offset Current +25°C ≤ T _A ≤ T _A (max) T _A (min) ≤ T _A ≤ 25°C | ΔI _{IO} /ΔT | - | 0.01 0.02 | 0.1 0.2 | - | 0.01 0.02 | 0.3 0.6 | nA/°C |
| Input Bias Current | I _{IB} | - | - | 100 | - | - | 300 | nA |
| Large Signal Voltage Gain V _S = ±15 V, V _O = ±10 V, R _L > 2.0 kΩ | A _V | 25 | - | - | 15 | - | - | V/mV |
| Input Voltage Range V _S = ±20 V V _S = ±15 V | V _{in} | ±15 | - | - | - | - | - | V |
| Common-Mode Rejection Ratio R _S ≤ 50 kΩ | CMRR | 80 | 96 | - | 70 | 90 | - | dB |
| Supply Voltage Rejection Ratio R _S ≤ 50 kΩ | PSSR | 80 | 96 | - | 70 | 96 | - | dB |
| Output Voltage Swing V _S = ±15 V, R _L = 10 kΩ R _L = 2.0 kΩ | V _O | ±12 ±10 | ±14 ±13 | - | ±12 ±10 | +14 ±13 | - | V |
| Supply Current (T _A = T _A (max), V _S = ±20 V) | I _D | - | 1.2 | 2.5 | - | - | - | mA |

*Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

MLM104G MLM204G MLM304G

NEGATIVE VOLTAGE REGULATOR

MONOLITHIC NEGATIVE VOLTAGE REGULATOR

The MLM104G, MLM204G, and MLM304G are functionally, electrically, and pin-for-pin equivalent to the LM104, LM204 and LM304 respectively.

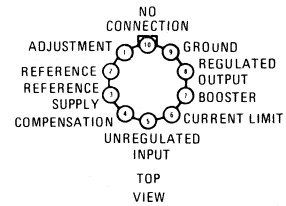
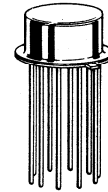
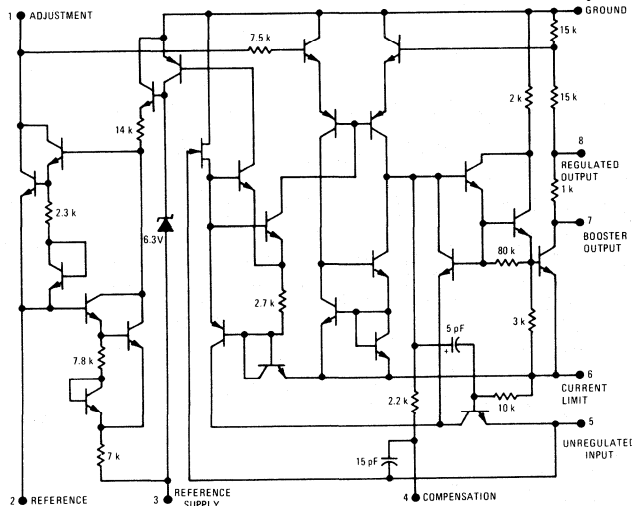
- Regulation No Load to Full Load – 1.0 mV
- Line Regulation – 0.01 %/V
- Ripple Rejection – 0.2 mV/V
- Temperature Stability Over Temperature Range – 0.3%

NEGATIVE VOLTAGE REGULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

NOVEMBER 1971 – DB-103

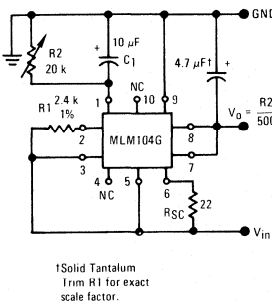
CIRCUIT SCHEMATIC



Pin 5 Electrically Connected to Case Through Substrate

METAL PACKAGE
CASE 603-02
(TO-100)

FIGURE 1 – BASIC REGULATOR CIRCUIT



TYPICAL APPLICATIONS

FIGURE 2 – SEPARATE BIAS SUPPLY OPERATION

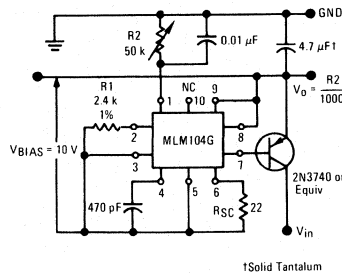
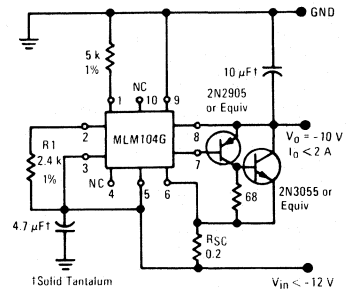


FIGURE 3 – HIGH CURRENT REGULATOR



See Packaging Information Section for outline dimensions.

MLM104G, MLM204G, MLM304G (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | MLM104G | MLM204G | MLM304G | Unit |
|--|----------------|-------------|-------------|-------------|------------------|
| Input Voltage | V_{in} | 50 | 50 | 40 | Vdc |
| Input-Output Voltage Differential | $V_{in} - V_o$ | 50 | 50 | 40 | Vdc |
| Power Dissipation (See Note 1) | P_D | 680 | 680 | 680 | mW |
| Operating Temperature Range | T_A | -55 to +125 | -25 to +85 | 0 to +70 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | -65 to +150 | -65 to +150 | $^\circ\text{C}$ |
| Lead Temperature (soldering, $t = 10$ s) | T_S | 300 | 300 | 300 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS (See Note 2)

| Characteristic | Symbol | MLM104G MLM204G | | | MLM304G | | | Unit |
|---|------------------------------------|--------------------|-----------------|-----------------|-------------|-----------------|-----------------|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage Range | V_{in} | -8.0 | — | -50 | -8.0 | — | -40 | Volts |
| Output Voltage Range | V_o | -0.015 | — | -40 | -0.035 | — | -30 | Volts |
| Output-Input Voltage Differential $I_o = 20$ mA $I_o = 5.0$ mA | $ V_{in} - V_o $ | 2.0 0.5 | — — | 50 50 | 2.0 0.5 | — — | 40 40 | Volts |
| Load Regulation $0 \leq I_o \leq 20$ mA, $R_{SC} = 15\Omega$ | Reg_{load} | — | 1.0 | 5.0 | — | 1.0 | 5.0 | mV |
| Line Regulation $V_o \leq -5.0$ V, $\Delta V_{in} = 0.1$ V | Reg_{in} | — | 0.056 | 0.1 | — | 0.056 | 0.1 | % |
| Ripple Rejection (See Figure 1) $C_1 = 10$ μF , $f = 120$ Hz $V_{in} < -15$ V -7.0 V $\geq V_{in} \geq -15$ V | Rej_R | — — | 0.2 0.5 | 0.5 1.0 | — — | 0.2 0.5 | 0.5 1.0 | mV/V |
| Output Voltage Scale Factor $R_1 = 2.4$ k Ω (See Figures 1,2 and 3) | SF | 1.8 | 2.0 | 2.2 | 1.8 | 2.0 | 2.2 | V/k Ω |
| Temperature Stability $V_o \leq -1.0$ V $V_o \leq -1.0$ V, $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ | TCV_o $\Delta V_o / \Delta T$ | — — | 0.3 — | 1.0 — | — — | — 0.3 | — 1.0 | % |
| Output Noise Voltage (See Figure 1) (10 Hz $\leq f \leq 10$ kHz) $V_o \leq -5.0$ V, $C_1 = 0$ $C_1 = 10$ μF | V_n | — — | 0.007 15 | — — | — — | 0.007 15 | — — | % μV |
| Standby Current Drain ($I_L = 5.0$ mA) $V_o = 0$ $V_o = -40$ V $V_o = -30$ V | I_B | — — — | 1.7 3.6 — | 2.5 5.0 — | — — — | 1.7 — 3.6 | 2.5 — 5.0 | mA |
| Long Term Stability $V_o \leq -1.0$ V | S | — | 0.1 | 1.0 | — | 0.1 | 1.0 | % |

Note 1. The maximum junction temperature of the MLM104G is $+150^\circ\text{C}$, for the MLM204G $+100^\circ\text{C}$, and for the MLM304G $+85^\circ\text{C}$. For operating at elevated temperatures, the package must be derated based on a thermal resistance of $150^\circ\text{C}/\text{W}$ — junction to ambient, or $45^\circ\text{C}/\text{W}$ — junction to case.

Note 2. These specifications apply for junction temperatures of -55°C to $+150^\circ\text{C}$ for the MLM104G; -25°C to $+100^\circ\text{C}$ for the MLM204G; and 0 to $+85^\circ\text{C}$ for the MLM304G. The specifications also apply for input and output voltages within the indicated ranges (unless otherwise specified). Load and line regulation specifications given are for constant junction temperature. Temperature drift effects must be taken into account separately when the device is operating under conditions of high power dissipation.

MLM105G MLM205G MLM305G

POSITIVE VOLTAGE REGULATOR

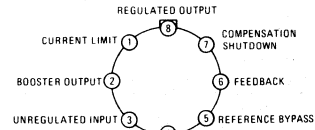
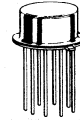
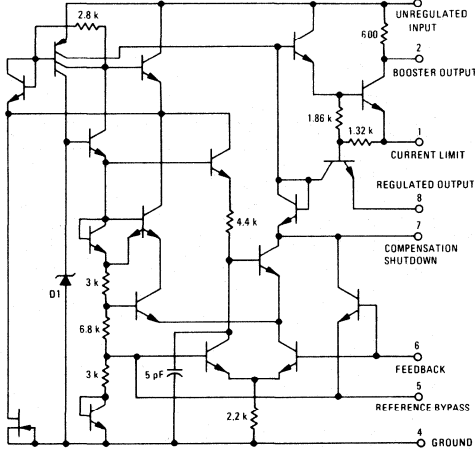
MONOLITHIC POSITIVE VOLTAGE REGULATOR

The MLM105G, MLM205G, and MLM305G are functionally, electrically, and pin-for-pin equivalent to the LM105, LM205, and LM305 respectively.

- Output Voltage Adjustable from 4.5 V to 40 V
- Output Currents in Excess of 10 A Possible by Addition of External Transistors
- Load Regulation Better than 0.1%, Full Load with Current Limiting
- DC Line Regulation, 0.03%/V
- Ripple Rejection, 0.01 %/V

POSITIVE VOLTAGE REGULATOR MONOLITHIC SILICON INTEGRATED CIRCUIT

CIRCUIT SCHEMATIC



**METAL PACKAGE
CASE 601
(TO-99)**

TYPICAL APPLICATIONS

FIGURE 1 – BASIC REGULATOR CIRCUIT

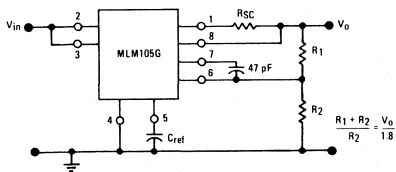


FIGURE 2 – 10 A REGULATOR with FOLDBACK CURRENT LIMITING

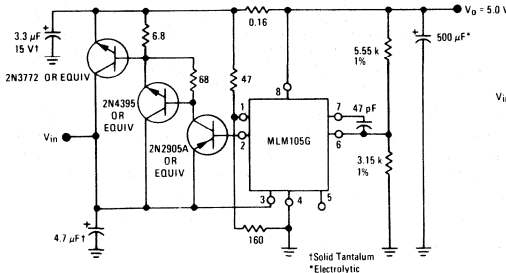
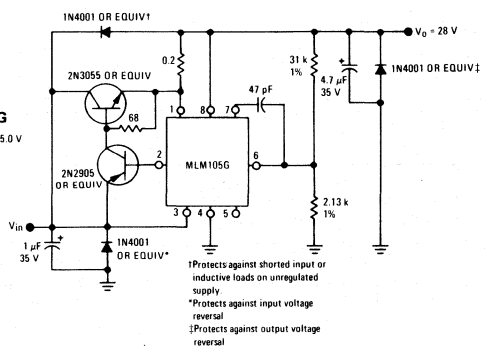


FIGURE 3 – 1.0 A REGULATOR with PROTECTIVE DIODES



- ! Protects against shorted input or inductive loads on unregulated supply
- * Protects against input voltage reversal
- ! Protects against output voltage reversal

See Packaging Information Section for outline dimensions.

MLM105G, MLM205G, MLM305G (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | MLM105G | MLM205G | MLM305G | Unit |
|--|---------------------------------|-------------|-------------|-------------|------|
| Input Voltage | V _{in} | 50 | 50 | 40 | Vdc |
| Input-Output Voltage Differential | V _{in} -V _o | 40 | 40 | 40 | Vdc |
| Power-Dissipation (See Note 1) | P _D | 680 | 680 | 680 | mW |
| Operating Temperature Range | T _A | -55 to +125 | -25 to +85 | 0 to +70 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | -65 to +150 | -65 to +150 | °C |
| Lead Temperature (soldering, t = 10 s) | T _S | 300 | 300 | 300 | °C |

ELECTRICAL CHARACTERISTICS (See Note 2)

| Characteristic | Symbol | MLM105G MLM205G | | | MLM305G | | | Unit |
|--|---|--------------------|----------------------|--------------------|---------|----------------------|--------------------|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage Range | V _{in} | 8.5 | — | 50 | 8.5 | — | 40 | Volts |
| Output Voltage Range | V _o | 4.5 | — | 40 | 4.5 | — | 30 | Volts |
| Output-Input Voltage Differential | V _{in} -V _o | 3.0 | — | 30 | 3.0 | — | 30 | Volts |
| Load Regulation (See Figure 1) (0 ≤ I _o ≤ 12 mA) R _{SC} = 18 Ω, T _A = +25°C R _{SC} = 10 Ω, T _A = T _{high} * R _{SC} = 18 Ω, T _A = T _{low} ** | Reg _{load} | — | 0.02 0.03 0.03 | 0.05 0.1 0.1 | — | 0.02 0.03 0.03 | 0.05 0.1 0.1 | % |
| Line Regulation V _{in} -V _o ≤ 5.0 V V _{in} -V _o > 5.0 V | Reg _{in} | — | 0.025 0.015 | 0.06 0.03 | — | 0.025 0.015 | 0.06 0.03 | %/V |
| Ripple Rejection (See Figure 1) C _{ref} = 10 μF, f = 120 Hz | ΔV _o V _o ΔV _i | — | 0.003 | 0.01 | 1.0 | 0.003 | 0.01 | %/V |
| Temperature Stability T _{low} ** ≤ T _A ≤ T _{high} * | TCV _o | — | 0.3 | 1.0 | — | 0.3 | 1.0 | % |
| Feedback Sense Voltage | V _{ref} | 1.63 | 1.7 | 1.81 | 1.63 | 1.7 | 1.81 | Volts |
| Output Noise Voltage (See Figure 1) (10 Hz ≤ f ≤ 10 kHz) C _{Ref} = 0 C _{Ref} > 0.1 μF | V _n | — | 0.005 0.002 | — | — | 0.005 0.002 | — | % |
| Standby Current Drain V _{in} = 50 V V _{in} = 40 V | I _B | — | 0.8 | 2.0 | — | — 0.8 | — 2.0 | mA |
| Long Term Stability | S | — | 0.1 | 1.0 | — | 0.1 | 1.0 | % |

*T_{high} = +125°C for MLM105G
+85°C for MLM205G
+70°C for MLM305G

**T_{low} = -55°C for MLM105G
-25°C for MLM205G
0°C for MLM305G

Note 1. The maximum junction temperature of the MLM105G is +150°C, for the MLM205G - +100°C, and for the MLM305G - +85°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance of 150°C/W - junction to ambient, or 45°C/W - junction to case.

Note 2. These specifications apply for junction temperatures of -55°C to +150°C for the MLM105G, -25°C to +85°C for the MLM205G, and 0 to +70°C for the MLM305G. Specifications also apply for input and output voltages within the indicated ranges and for a divider impedance sensed by the feedback terminal of 2.0 kilohms (unless otherwise specified). Load and line regulation specifications given are for constant junction temperature. Temperature drift effects must be taken into account separately when the device is operating under conditions of high power dissipation.

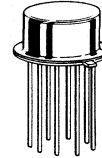
**MLM107G
MLM207G
MLM307G**

**INTERNALLY COMPENSATED
MONOLITHIC OPERATIONAL AMPLIFIER**

The MLM107G, MLM207G, and MLM307G are functionally, electrically, and pin-for-pin equivalent to the National Semiconductor LM107, LM207, and LM307 respectively.

- Internally Compensated
- Low Offset Voltage: 2.0 mV max (MLM107G)
- Low Input Offset Current: 10 nA max (MLM107G)
- Low Input Bias Current: 75 nA max (MLM107G)

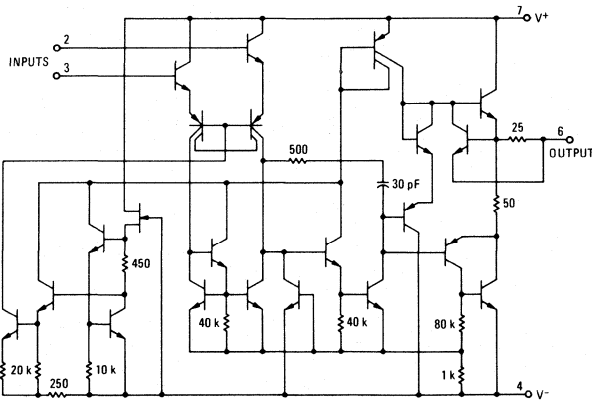
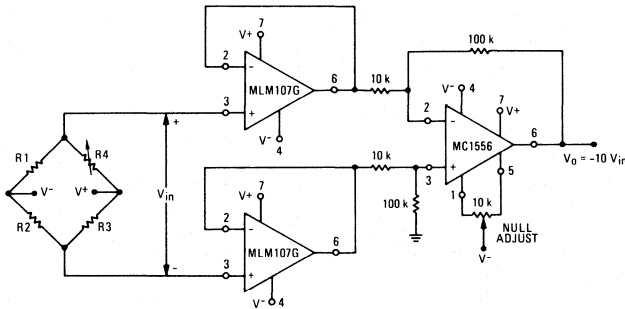
**OPERATIONAL AMPLIFIER
INTEGRATED CIRCUIT
EPITAXIAL PASSIVATED**



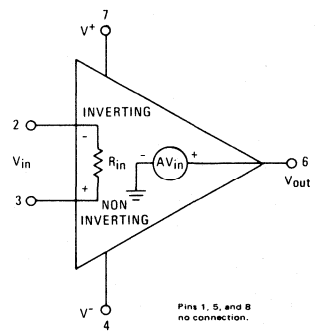
**METAL PACKAGE
CASE 601
TO-99**

Pin 4 connected to case.

**TYPICAL APPLICATION
HIGH IMPEDANCE BRIDGE AMPLIFIER**



EQUIVALENT CIRCUIT



See Packaging Information Section for outline dimensions.

MLM107G, MLM207G, MLM307G (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

| Rating | Symbol | MLM107G | MLM207G | MLM307G | Unit |
|---|-------------------|-------------|-------------|-------------|-------|
| Power Supply Voltage | V+ | +22 | +22 | +18 | Vdc |
| | V- | -22 | -22 | -18 | |
| Differential Input Signal | V _{in} | ±30 | ±30 | ±30 | Volts |
| Common-Mode Input Swing (Note 1) | CMV _{in} | ±15 | ±15 | ±15 | Volts |
| Output Short Circuit Duration | T _{SC} | Indefinite | | | |
| Power Dissipation (Package Limitation) (Note 2) | P _D | 500 | 500 | 500 | mW |
| Operating Temperature Range | T _A | -55 to +125 | -25 to +85 | 0 to +70 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | -65 to +150 | -65 to +150 | °C |

ELECTRICAL CHARACTERISTICS T_A = +25°C unless otherwise noted, See Note 3

| Characteristics | Symbol | MLM107G MLM207G | | | MLM307G | | | Unit |
|--|---------------------------------|--------------------|------|-----|---------|------|-----|---------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage R _S ≤ 10 kΩ, T _A = +25°C R _S ≤ 10 kΩ, T _A = T _{low} to T _{high} R _S ≤ 50 kΩ, T _A = +25°C R _S ≤ 50 kΩ, T _A = T _{low} to T _{high} | V _{io} | — | 0.7 | 2.0 | — | — | — | mV |
| | | — | — | 3.0 | — | — | — | |
| | | — | — | — | — | 2.0 | 7.5 | |
| | | — | — | — | — | — | 10 | |
| Input Offset Current T _A = +25°C T _A = T _{low} to T _{high} | I _{io} | — | 1.5 | 10 | — | 3.0 | 50 | nA |
| | | — | — | 20 | — | — | 70 | |
| Input Bias Current T _A = +25°C T _A = T _{low} to T _{high} | I _b | — | 30 | 75 | — | 70 | 250 | nA |
| | | — | — | 100 | — | — | 300 | |
| Input Resistance | R _{in} | 1.5 | 4.0 | — | 0.5 | 2.0 | — | Megohms |
| Supply Current V _S = ±20 V, T _A = +25°C V _S = ±20 V, T _A = T _{high} V _S = ±15 V, T _A = +25°C | I _D | — | 1.8 | 3.0 | — | — | — | mA |
| | | — | 1.2 | 2.5 | — | — | — | |
| | | — | — | — | — | 1.8 | 3.0 | |
| Large Signal Voltage Gain V _S = ±15 V, V _O = ±10 V, R _L > 2.0 kΩ, T _A = +25°C V _S = ±15 V, V _O = ±10 V, R _L ≥ 2.0 kΩ, T _A = T _{low} | A _v | 50 | 160 | — | 25 | 160 | — | V/mV |
| | | 25 | — | — | 15 | — | — | |
| Average Temperature Coefficient of Input Offset Voltage T _{low} ≤ T _A ≤ T _{high} | TC _{Vio} | — | 3.0 | 15 | — | 6.0 | 30 | μV/°C |
| Average Temperature Coefficient of Input Offset Current +25°C ≤ T _A ≤ T _{high} T _{low} ≤ T _A ≤ +25°C | TC _{Iio} | — | 0.01 | 0.1 | — | 0.01 | 0.3 | nA/°C |
| | | — | 0.02 | 0.2 | — | 0.02 | 0.6 | |
| Output Voltage Swing (T _A = T _{low} to T _{high}) V _S = ±15 V, R _L = 10 kΩ R _L = 2.0 kΩ | V _O | ±12 | ±14 | — | ±12 | ±14 | — | V |
| | | ±10 | ±13 | — | ±10 | ±13 | — | |
| Input Voltage Range (T _A = T _{low} to T _{high}) V _S = ±20 V V _S = ±15 V | V _{in} | ±15 | — | — | — | — | — | V |
| | | — | — | — | ±12 | — | — | |
| Common-Mode Rejection Ratio (T _A = T _{low} to T _{high}) R _S ≤ 10 kΩ R _S ≤ 50 kΩ | CM _{rej} | 80 | 96 | — | — | — | — | dB |
| | | — | — | — | 70 | 90 | — | |
| Supply Voltage Rejection Ratio (T _A = T _{low} to T _{high}) R _S ≤ 10 kΩ R _S ≤ 50 kΩ | S ⁺ , S ⁻ | 80 | 96 | — | — | — | — | dB |
| | | — | — | — | 70 | 96 | — | |

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. For operating at elevated temperatures, the device must be derated based on a maximum junction temperature of +150°C for the MLM107G, and 100°C for the MLM207G and MLM307G. The TO-99 package is derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

Note 3. Unless otherwise noted, these specifications apply for:

±5.0 V ≤ V_S ≤ ±20 V, T_{low} -55°C ≤ T_A ≤ +125°C, MLM107G
 ±5.0 V ≤ V_S ≤ ±20 V, -25°C ≤ T_A ≤ +85°C, MLM207G
 ±5.0 V ≤ V_S ≤ ±15 V, 0°C ≤ T_A ≤ +70°C, MLM307G

MLM109K MLM209K MLM309K

VOLTAGE REGULATOR

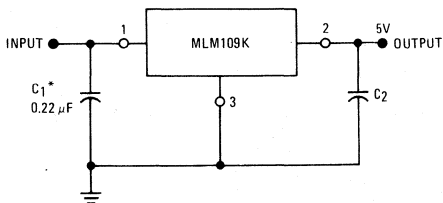
MONOLITHIC VOLTAGE REGULATOR

The MLM109K, MLM209K, and MLM309K are functionally, electrically, and pin-for-pin equivalent to the National Semiconductor LM109, LM209, and LM309 respectively.

- Fixed 5.0 Volt Output Voltage
- Output Current in Excess of 1.0 Ampere
- Internal Thermal Overload Protection

VOLTAGE REGULATOR MONOLITHIC SILICON INTEGRATED CIRCUIT

FIXED 5.0 V REGULATOR



NOTES:

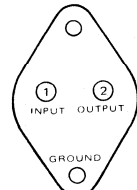
* Required if regulator is located an appreciable distance from power supply filter. Although no output capacitor is needed for stability, it does improve transient response.



METAL PACKAGE

CASE 11

(TO-3)



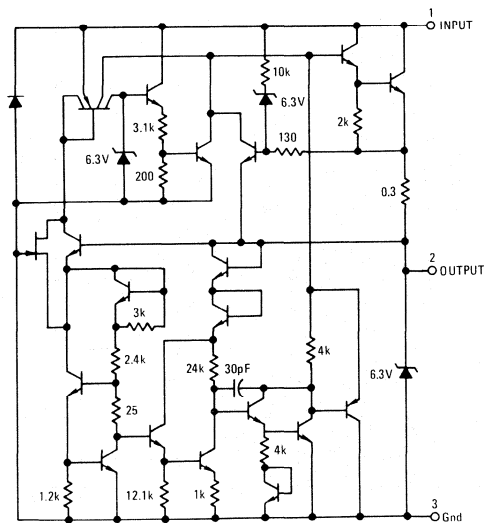
BOTTOM VIEW

Leads 1 and 2 electrically isolated from case.

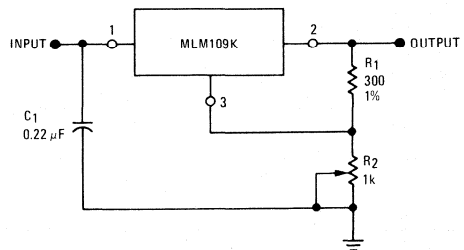
Case is third electrical connection.

Leads are gold-plated copper cored kovar. Package weight \approx 7.4 grams.

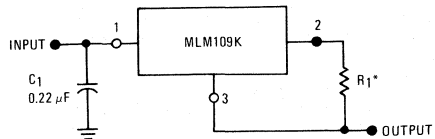
CIRCUIT SCHEMATIC



ADJUSTABLE OUTPUT REGULATOR



CURRENT REGULATOR



* Determines output current.

See Packaging Information Section for outline dimensions.

MLM109K, MLM209K, MLM309K (continued)

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|-----------|---|------|
| Input Voltage | V_{in} | 35 | Vdc |
| Power Dissipation | P_D | Internally Limited | |
| Operating Temperature Range MLM109K MLM209K MLM309K | T_A | -55 to +150 -25 to +150 0 to +125 | °C |
| Storage Temperature Range | T_{stg} | -65 to +150 | °C |
| Lead Temperature (soldering, $t = 60$ s) | T_S | 300 | °C |

ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | MLM109K/MLM209K ① | | | MLM309K ② | | | Unit |
|--|---------------------|-------------------|------|-----|-----------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J = +25^\circ\text{C}$) | V_o | 4.7 | 5.05 | 5.3 | 4.8 | 5.05 | 5.2 | Vdc |
| Input Regulation ($T_J = +25^\circ\text{C}$) $7.0\text{V} \leq V_{in} \leq 25\text{V}$ | Reg_{in} | — | 4.0 | 50 | — | 4.0 | 50 | mV |
| Load Regulation ($T_J = +25^\circ\text{C}$) $5.0\text{mA} \leq I_o \leq 1.5\text{A}$ | Reg_{load} | — | 50 | 100 | — | 50 | 100 | mV |
| Output Voltage Range $7.0\text{V} \leq V_{in} \leq 25\text{V}$ $5.0\text{mA} \leq I_o \leq I_{max}$, $P \leq P_{max}$ | V_o | 4.6 | — | 5.4 | 4.75 | — | 5.25 | Vdc |
| Quiescent Current ($7.0\text{V} \leq V_{in} \leq 25\text{V}$) | I_b | — | 5.2 | 10 | — | 5.2 | 10 | mAdc |
| Quiescent Current Change ($7.0\text{V} \leq V_{in} \leq 25\text{V}$) $5.0\text{mA} \leq I_o \leq I_{max}$ | ΔI_b | — | — | 0.5 | — | — | 0.8 | |
| Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{Hz} \leq f \leq 100\text{kHz}$ | V_n | — | 40 | — | — | 40 | — | μV |
| Long Term Stability | S | — | — | 10 | — | — | 20 | mV |
| Thermal Resistance, Junction to Case ③ | θ_{JC} | — | 3.0 | — | — | 3.0 | — | °C/W |

NOTES:

- ① Unless otherwise specified, these specifications apply for $-55^\circ\text{C} \leq T_j \leq +150^\circ\text{C}$ ($-25^\circ\text{C} \leq T_j \leq +150^\circ\text{C}$ for the MLM209K), $V_{in} = 10\text{V}$ and $I_o = 0.5\text{A}$. $I_{max} = 1.0\text{A}$ and $P_{max} = 20\text{W}$.
- ② Unless otherwise specified, these specifications apply for $0^\circ\text{C} \leq T_j \leq +125^\circ\text{C}$, $V_{in} = 10\text{V}$ and $I_{out} = 0.5\text{A}$. $I_{max} = 1.0\text{A}$ and $P_{max} = 20\text{W}$.
- ③ Without a heat sink, the thermal resistance is approximately $35^\circ\text{C}/\text{W}$. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the heat sink.

MLM210G MLM310G

OPERATIONAL AMPLIFIER

MONOLITHIC OPERATIONAL AMPLIFIER VOLTAGE FOLLOWER

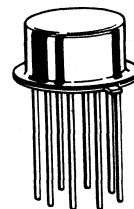
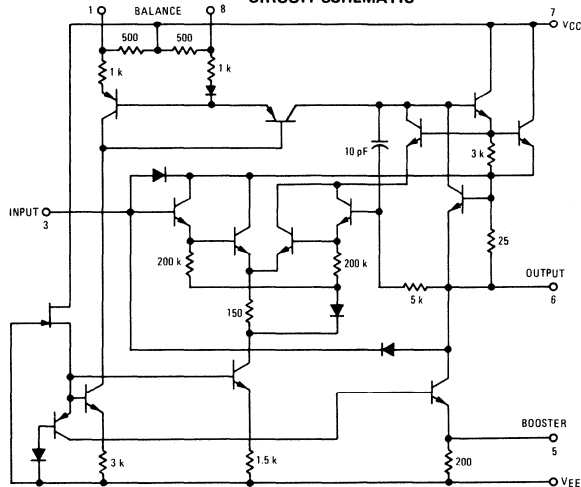
The MLM210G and MLM310G are functionally, electrically, and pin-for-pin equivalent to the LM210 and LM310, respectively.

- Input Bias Current: 10 nA maximum over Temperature Range
- Small-Signal Bandwidth: 20 MHz typical
- Slew Rate: 30 Volts/ μ s typical
- Supply Voltage Range: ± 5.0 V to ± 18 V

OPERATIONAL AMPLIFIER VOLTAGE FOLLOWER INTEGRATED CIRCUIT

EPITAXIAL PASSIVATED

CIRCUIT SCHEMATIC



Case connected to pin 4 through substrate.

METAL PACKAGE
CASE 601
TO-99

TYPICAL APPLICATIONS

FIGURE 1 – OFFSET BALANCING CIRCUIT

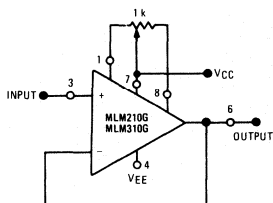
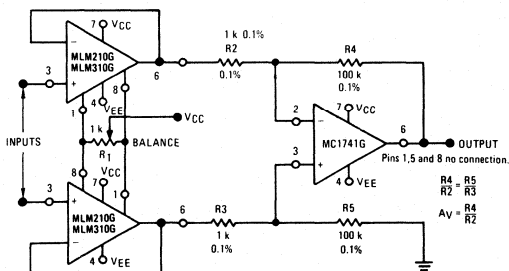


FIGURE 2 – DIFFERENTIAL INPUT INSTRUMENTATION
AMPLIFIER



See Packaging Information Section for outline dimensions.

MLM210G, MLM310G (continued)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

| Rating | Symbol† | MLM210G | MLM310G | Unit |
|---|--|-------------|-------------|-------|
| Power Supply Voltage | V _{CC} (max) V _{EE} (max) | +18 -18 | +18 -18 | Vdc |
| Input Voltage (Note 1) | V _{IC} | ± 15 | ± 15 | Volts |
| Output Short Circuit Duration (Note 2) | T _{sc} | Indefinite | | |
| Power Dissipation (Package Limitation) (Note 3) | P _D | 500 | 500 | mW |
| Operating Temperature Range | T _A | -25 to +85 | 0 to +70 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | -65 to +150 | °C |
| Lead Temperature (soldering, t = 10 s) | T _S | 300 | 300 | °C |

ELECTRICAL CHARACTERISTICS (See Note 4)

| Characteristic | Symbol† | MLM210G | | | MLM310G | | | Unit |
|--|----------------------|------------------|------------------|-------------|------------------|------------------|-------------|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage T _A = +25°C T _A = T _{low} * to T _{high} ** | V _{IO} | — | 1.5 | 4.0 | — | 2.5 | 7.5 | mV |
| Input Bias Current T _A = +25°C T _A = T _{low} to T _{high} | I _{IB} | — | 1.0 | 3.0 | — | 2.0 | 7.0 | nA |
| Input Resistance | r _i | 10 ¹⁰ | 10 ¹² | — | 10 ¹⁰ | 10 ¹² | — | ohms |
| Input Capacitance | C _i | — | 1.5 | — | — | 1.5 | — | pF |
| Large-Signal Voltage Gain (V _S = ± 15 V, V _O = +10 V) T _A = +25°C, R _L = 8.0 k ohms T _A = T _{low} to T _{high} , R _L = 10 k ohms | A _{VS} | 0.999 0.999 | 0.9999 — | — — | 0.999 0.999 | 0.9999 — | — — | V/V |
| Output Resistance T _A = +25°C | r _o | — | 0.75 | 2.5 | — | 0.75 | 2.5 | ohms |
| Small-Signal Bandwidth | BW | — | 20 | — | — | 20 | — | MHz |
| Slew Rate | SR | — | 30 | — | — | 30 | — | V/μs |
| Supply Current T _A = +25°C T _A = T _{high} | I _D | — | 3.9 2.0 | 5.5 4.0 | — | 3.9 — | 5.5 — | mA |
| Offset Voltage Temperature Drift -55°C ≤ T _A ≤ +85°C T _A = +125°C 0°C ≤ T _A ≤ +70°C | ΔV _{IO} /ΔT | — | 6.0 12 — | — — — | — | — — 10 | — — — | μV/°C |
| Output Voltage Swing V _S = ± 15 V, R _L = 10 k ohms | V _O | ± 10 | — | — | ± 10 | — | — | Volts |
| Supply Voltage Rejection Ratio ± 5/0 V ≤ V _S ≤ ± 18 V | PSRR | 70 | 80 | — | 70 | 80 | — | dB |

*T_{low} = -25°C for MLM210G
= 0°C for MLM310G

**T_{high} = +85°C for MLM210G
= +70°C for MLM310G

†Symbols conform to JEDEC Bulletin No. 1 where applicable.

Note 1. For supply voltages less than ± 15 volts, the absolute maximum input voltage is equal to the supply voltage.

Note 2. A continuous short circuit duration capability is specified for MLM210G as follows: case temperatures up to +125°C and ambient temperatures up to +70°C; for the MLM310G up to +70°C case temperature and +55°C ambient temperature apply. A resistor (greater than 2.0 kilohms) must be inserted in series with the input when the amplifier is driven from a low impedance source, thus preventing damage when the output is shorted.

Note 3. The maximum junction temperature of the MLM210G is +100°C, and for the MLM310G - +85°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance of 150°C/W - junction to ambient, or 45°C - junction to case.

Note 4. All listed specifications apply for ± 5.0 V ≤ V_S ≤ ± 18 V and T_A = +25°C unless otherwise noted.

Note 5. Increased output swing under load can be obtained by connecting an external resistor between the booster and V_{EE} terminals (pins 4 and 5).

CASE OUTLINE DIMENSIONS

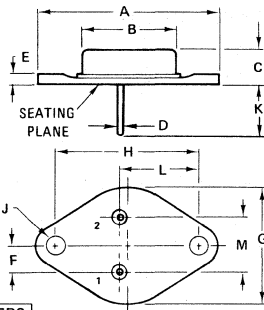
DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED.

The packaging availability for each device type is indicated on the individual data sheets and the Linear Selector Guide. All of the outline dimensions for the packages are given in this section. Outline dimensions for non-encapsulated standard linear device chips, flip-chips, and beam-lead devices are found on the individual data sheets (see MCC, MCF, or MCBC prefix followed by type number).

CASE 11(TO-3)

Weight \approx 7.4 grams

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR



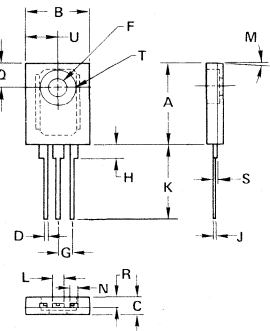
| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|--------|
| | MIN | MAX | MIN | MAX |
| A | — | 1.550 | — | 39.370 |
| B | — | 0.830 | — | 21.080 |
| C | 0.250 | 0.300 | 6.350 | 7.620 |
| D | 0.039 | 0.043 | 0.991 | 1.090 |
| E | — | 0.135 | — | 3.430 |
| F | 0.205 | 0.225 | 5.210 | 5.720 |
| G | — | 1.050 | — | 26.670 |
| H | 1.177 | 1.197 | 29.900 | 30.400 |
| J | 0.151 | 0.161 | 3.840 | 4.090 |
| K | 0.440 | 0.480 | 11.180 | 12.190 |
| L | 0.655 | 0.675 | 16.640 | 17.150 |
| M | 0.420 | 0.440 | 10.670 | 11.180 |

All JEDEC dimensions and notes apply

CASE 199-04

Weight \approx 2.48 grams

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 16.08 | 16.33 | 0.633 | 0.643 |
| B | 12.57 | 12.83 | 0.495 | 0.505 |
| C | 3.18 | 3.43 | 0.125 | 0.135 |
| D | 0.51 | 0.76 | 0.020 | 0.030 |
| F | 3.61 | 3.86 | 0.142 | 0.152 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 2.67 | 2.92 | 0.105 | 0.115 |
| J | 0.43 | 0.69 | 0.017 | 0.027 |
| K | 14.73 | 14.99 | 0.580 | 0.590 |
| L | 2.16 | 2.41 | 0.085 | 0.095 |
| M | 30° TYP | | 30° TYP | |
| N | 1.47 | 1.73 | 0.058 | 0.068 |
| Q | 4.78 | 5.03 | 0.188 | 0.198 |
| R | 1.91 | 2.16 | 0.075 | 0.085 |
| S | 0.81 | 0.86 | 0.032 | 0.034 |
| T | 6.99 | 7.24 | 0.275 | 0.285 |
| U | 6.22 | 6.48 | 0.245 | 0.255 |

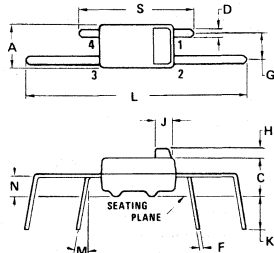


NOTES:
1. DIM "G" IS TO CENTER OF LEADS

CASE 206A

Plastic Package

Weight \approx 0.2 gram

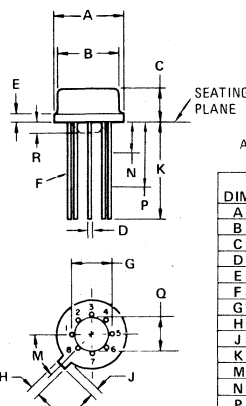


| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 3.30 | 3.81 | 0.130 | 0.150 |
| C | 3.43 | 3.94 | 0.135 | 0.155 |
| D | 0.64 | 0.89 | 0.025 | 0.035 |
| F | 0.20 | 0.30 | 0.008 | 0.012 |
| G | 1.88 | 2.18 | 0.074 | 0.086 |
| H | 0.64 | 0.89 | 0.025 | 0.035 |
| J | 1.50 | 1.75 | 0.059 | 0.069 |
| K | 2.92 | 3.18 | 0.115 | 0.125 |
| L | 15.75 | 16.76 | 0.620 | 0.660 |
| M | — | 1.04 | — | 10° |
| N | 1.78 | 2.03 | 0.070 | 0.080 |
| S | 8.64 | 9.65 | 0.340 | 0.380 |

CASE 601-02 TO-99

G Suffix
Metal Package

Weight \approx 0.92 gram



STYLE 1: 601
ALL PINS USED
STYLE 2: (WAS 601B)
PINS 5 & 7 OMITTED
STYLE 3: (WAS 601C)
PINS 2 & 6 OMITTED

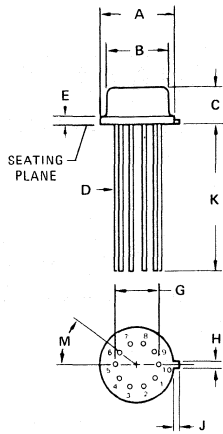
All JEDEC dimensions and notes apply

| DIM | INCHES | | MILLIMETERS | |
|-----|----------|-------|-------------|--------|
| | MIN | MAX | MIN | MAX |
| A | 0.335 | 0.370 | 8.510 | 9.390 |
| B | 0.305 | 0.335 | 7.750 | 8.500 |
| C | 0.165 | 0.185 | 4.200 | 4.690 |
| D | 0.016 | 0.021 | 0.4070 | 0.533 |
| E | — | 0.040 | — | 1.020 |
| F | 0.016 | 0.019 | 0.406 | 0.482 |
| G | 0.200 TP | | 5.080 TP | |
| H | 0.028 | 0.034 | 0.712 | 0.864 |
| J | 0.029 | 0.045 | 0.737 | 1.140 |
| K | — | — | — | 12.700 |
| L | 45° TYP | | 45° TYP | |
| M | — | 0.050 | — | 1.270 |
| N | 0.250 | 0.500 | 6.350 | 12.700 |
| Q | 0.140 | 0.160 | 3.560 | 4.060 |
| R | 0.010 | 0.040 | 0.254 | 1.010 |

CASE 602A

Weight \approx 0.918 gram

| DIM | INCHES | | MILLIMETERS | |
|-----|----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.335 | 0.370 | 8.510 | 9.390 |
| B | 0.305 | 0.335 | 7.750 | 8.500 |
| C | — | 0.180 | — | 4.570 |
| D | 0.016 | 0.019 | 0.407 | 0.482 |
| E | — | 0.040 | — | 1.010 |
| G | 0.230 TP | | 5.840 TP | |
| H | 0.028 | 0.034 | 0.712 | 0.863 |
| J | 0.029 | 0.045 | 0.736 | 1.140 |
| K | 0.500 | — | 12.700 | — |
| M | 36° TP | | 36° TP | |

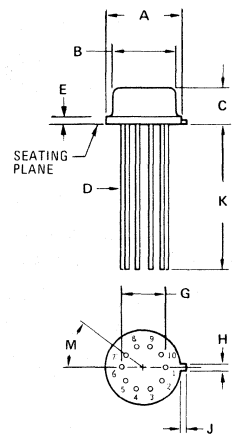


CASE 602B

G Suffix
Metal Package

Weight \approx 0.918 gram

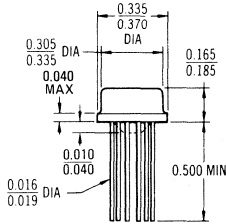
| DIM | INCHES | | MILLIMETERS | |
|-----|----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.335 | 0.370 | 8.510 | 9.390 |
| B | 0.305 | 0.335 | 7.750 | 8.500 |
| C | — | 0.180 | — | 4.570 |
| D | 0.016 | 0.019 | 0.407 | 0.482 |
| E | — | 0.040 | — | 1.010 |
| G | 0.230 TP | | 5.840 TP | |
| H | 0.028 | 0.034 | 0.712 | 0.863 |
| J | 0.029 | 0.045 | 0.736 | 1.140 |
| K | 0.750 | — | 19.050 | — |
| M | 36° TP | | 36° TP | |



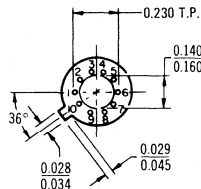
CASE 603-02 TO-100

G Suffix
Metal Package

Weight \approx 0.918 gram



All JEDEC dimensions and notes apply



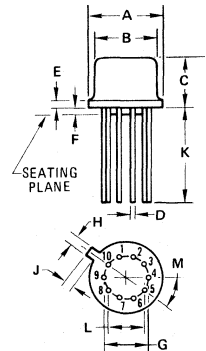
Weight \approx 0.918 gram

CASE 603-03

G Suffix
Metal Package

Weight \approx 0.918 gram

| DIM | INCHES | | MILLIMETERS | |
|-----|----------|------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | .335 | .370 | 8.51 | 9.39 |
| B | .305 | .335 | 7.75 | 8.50 |
| C | .240 | .260 | 6.09 | 6.60 |
| D | .016 | .019 | .407 | .482 |
| E | — | .040 | — | 1.01 |
| F | — | .040 | — | 1.01 |
| G | .230 TYP | | 5.84 TYP | |
| H | .028 | .034 | .712 | .863 |
| J | .029 | .045 | .736 | 1.14 |
| K | .500 | — | 12.70 | — |
| L | .140 | .160 | 3.56 | 4.06 |
| M | 36° TP | | 36° TP | |



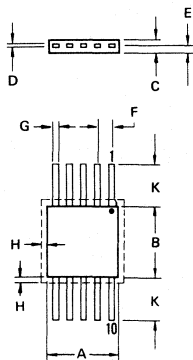
CASE 606 TO-91

F Suffix
Ceramic Package

Weight \approx 0.127 gram

All JEDEC dimensions and notes apply

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.240 | 0.290 | 6.100 | 7.360 |
| B | 0.240 | 0.260 | 6.100 | 6.600 |
| C | 0.030 | 0.070 | 0.762 | 1.770 |
| D | 0.003 | 0.006 | 0.077 | 0.152 |
| E | 0.005 | 0.035 | 0.127 | 0.889 |
| F | 0.045 | 0.055 | 1.150 | 1.390 |
| G | 0.010 | 0.019 | 0.254 | 0.482 |
| H | — | 0.015 | — | 0.381 |
| K | 0.070 | — | 1.780 | — |



NOTE:
1. LEAD "1" IS IDENTIFIED BY A TAB ON THAT LEAD.

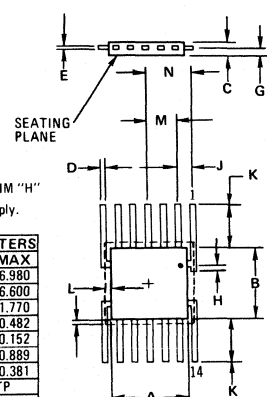
CASE 607 TO-86

F Suffix
Ceramic Package

Weight \approx 0.218 gram

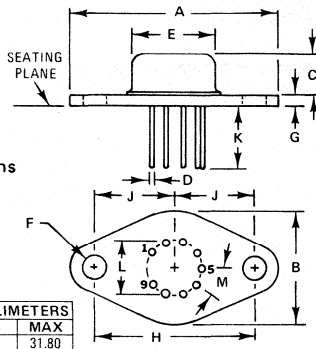
NOTE:
LEAD #1 IDENTIFIED BY A TAB DIM "H"
All JEDEC dimensions and notes apply.

| DIM | INCHES | | MILLIMETERS | |
|-----|----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.240 | 0.275 | 6.100 | 6.980 |
| B | 0.240 | 0.260 | 6.100 | 6.600 |
| C | 0.030 | 0.070 | 0.762 | 1.770 |
| D | 0.010 | 0.019 | 0.254 | 0.482 |
| E | 0.003 | 0.006 | 0.077 | 0.152 |
| G | 0.005 | 0.035 | 0.127 | 0.889 |
| H | — | 0.015 | — | 0.381 |
| J | 0.050 TP | | 1.270 TP | |
| K | 0.070 | — | 1.770 | — |
| L | — | 0.015 | — | 0.381 |
| M | 0.100 TP | | 2.540 TP | |
| N | 0.150 TP | | 3.810 TP | |



CASE 614

R Suffix
Metal Package



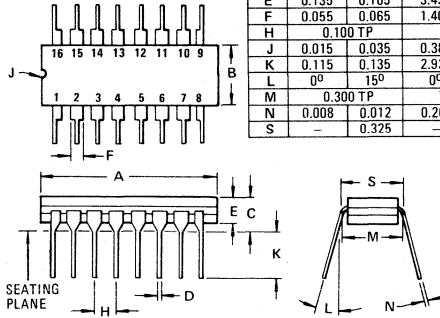
Weight \approx 6.315 grams

| DIM | INCHES | | MILLIMETERS | |
|-----|------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | — | 1.252 | — | 31.80 |
| B | — | .700 | — | 17.78 |
| C | .200 | .265 | 5.08 | 6.73 |
| D | .028 | .032 | .711 | .813 |
| E | .470 | .500 | 11.94 | 12.70 |
| F | .142 | .152D | 3.61 | 3.86 |
| G | .050 | .075 | 1.27 | 1.90 |
| H | .958 | .962 | 24.33 | 24.43 |
| J | .477 | .483 | 12.12 | 12.27 |
| K | .360 | — | 9.14 | — |
| L | .325 TYP R | — | 8.25 TYP | — |
| M | .36° TYP | — | 36° TYP | — |

CASE 620

L Suffix
Ceramic Package

| DIM | INCHES | | MILLIMETERS | |
|-----|----------|-------|-------------|--------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.780 | 18.790 | 19.810 |
| B | 0.240 | 0.275 | 6.100 | 6.990 |
| C | 0.170 | 0.200 | 4.320 | 5.080 |
| D | 0.015 | 0.020 | 0.381 | 0.508 |
| E | 0.135 | 0.165 | 3.430 | 4.190 |
| F | 0.065 | 0.065 | 1.400 | 1.650 |
| H | 0.100 TP | | 2.54 TP | |
| J | 0.015 | 0.035 | 0.381 | 0.889 |
| K | 0.115 | 0.135 | 2.930 | 3.430 |
| L | 0° | 15° | 0° | 15° |
| M | 0.300 TP | | 7.620 TP | |
| N | 0.008 | 0.012 | 0.203 | 0.305 |
| S | — | 0.325 | — | 8.260 |



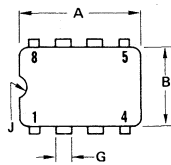
- NOTES:
1. DIM. "M" IS MEASURED AT CENTER OF LEADS WHEN FORMED PARALLEL.
2. "J" INDEX: NOTCH IN LEAD, INK DOT, OR NOTCH IN CERAMIC.

Weight \approx 1.97 grams

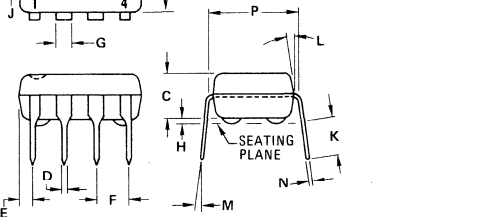
CASE 626

P Suffix
Plastic Package

Weight \approx 0.446 gram



| DIM | INCHES | | MILLIMETERS | |
|-----|----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | .370 | .390 | 9.39 | 9.90 |
| B | .240 | .250 | 6.09 | 6.35 |
| C | .135 | .155 | 3.43 | 3.94 |
| D | .015 | .019 | .381 | .483 |
| E | — | .045 | — | 1.14 |
| F | 0.100 TP | | 2.54 TP | |
| G | .030 | .060 | .762 | 1.52 |
| H | .020 NOM | | 508 NOM | |
| J | .030 | .040R | .762 | 1.02R |
| K | .115 | .135 | 2.92 | 3.43 |
| L | .70° TYP | | .70° TYP | |
| M | 0° | 10° | 0° | 10° |
| N | .008 | .011 | .203 | .279 |
| P | .290 | .310 | 7.37 | 7.87 |



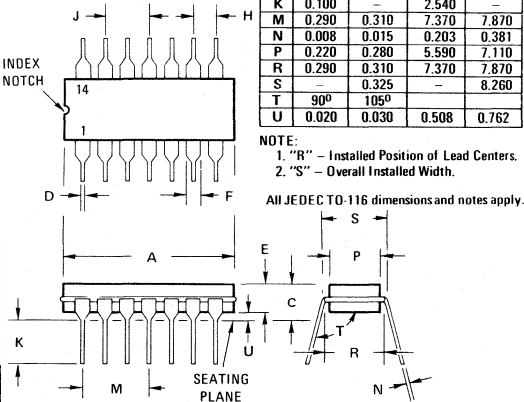
- NOTES: 1. DIMENSION "P" IS TO LEAD CENTERLINE WHEN FORMED PARALLEL.
2. FOUR (4) INSULATING STANDOFFS ARE PROVIDED.

CASE 632 TO-116

L Suffix
Ceramic Package

Weight \approx 1.954 grams

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|--------|
| | MIN | MAX | MIN | MAX |
| A | 0.660 | 0.780 | 17.400 | 19.900 |
| C | — | 0.200 | — | 5.080 |
| D | 0.015 | 0.023 | 0.381 | 0.584 |
| F | 0.030 | 0.070 | 0.770 | 1.770 |
| H | 0.090 | 0.110 | 2.290 | 2.790 |
| J | 0.190 | 0.210 | 4.830 | 5.330 |
| K | 0.100 | — | 2.540 | — |
| M | 0.290 | 0.310 | 7.370 | 7.870 |
| N | 0.008 | 0.015 | 0.203 | 0.381 |
| P | 0.220 | 0.280 | 5.590 | 7.110 |
| R | 0.290 | 0.310 | 7.370 | 7.870 |
| S | — | 0.325 | — | 8.260 |
| T | 90° | 105° | — | — |
| U | 0.020 | 0.030 | 0.508 | 0.762 |



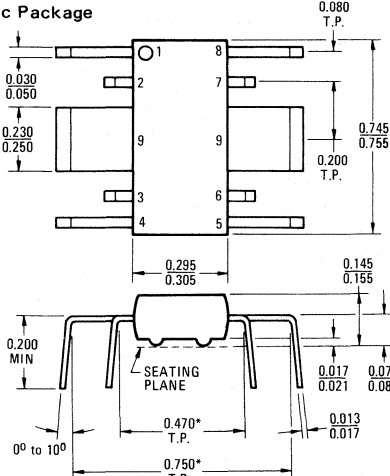
- NOTE:
1. "R" — Installed Position of Lead Centers.
2. "S" — Overall Installed Width.

All JEDEC TO-116 dimensions and notes apply.

CASE 641

Plastic Package

Weight \approx 1.85 grams

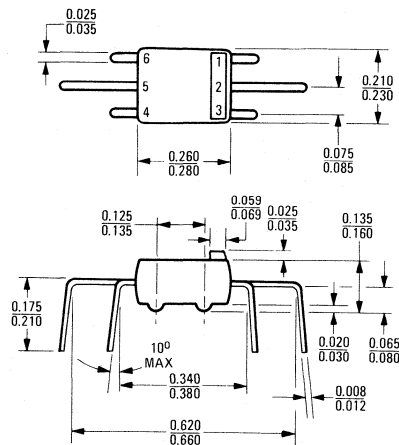


*Dimension is to lead centerline when formed parallel.

CASE 643A

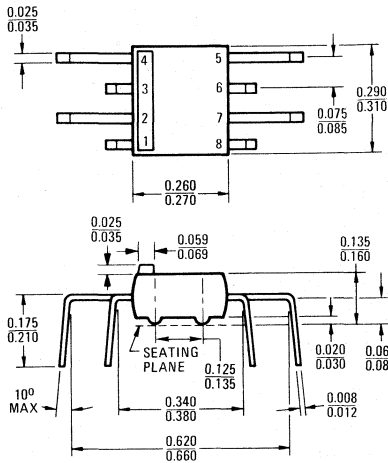
Plastic Package

Weight \approx 0.31 gram



CASE 644A
Plastic Package

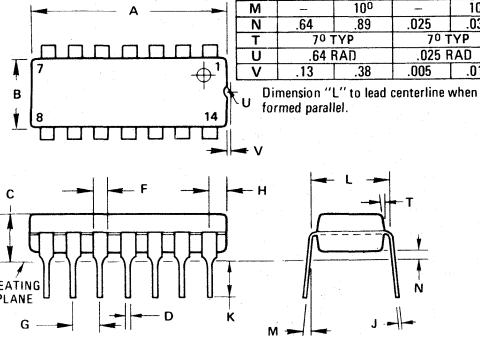
Weight \approx 0.45 gram



CASE 646

P Suffix
Plastic Package
Weight \approx 0.911 gram

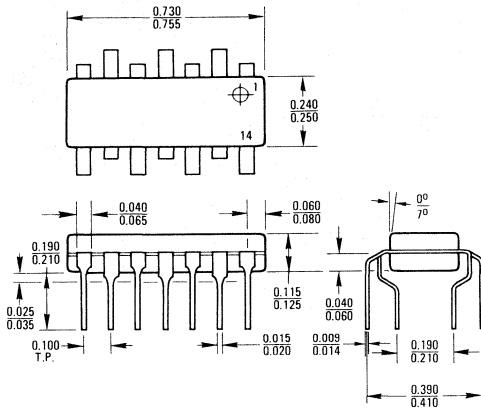
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| A | 18.03 | 18.79 | .710 | .740 |
| B | 6.09 | 6.60 | .240 | .260 |
| C | 4.06 | 4.57 | .160 | .180 |
| D | .38 | .51 | .015 | .020 |
| F | 1.02 | 1.65 | .040 | .065 |
| G | 2.54 BSC | | .100 BSC | |
| H | 1.32 | 1.83 | .052 | .072 |
| J | .23 | .36 | .009 | .014 |
| K | 2.92 | 3.43 | .115 | .135 |
| L | 7.37 | 7.87 | .290 | .310 |
| M | - | 10° | - | 10° |
| N | .64 | .89 | .025 | .035 |
| T | 7° TYP | | 7° TYP | |
| U | .64 RAD | | .025 RAD | |
| V | .13 | .38 | .005 | .015 |



CASE 647

PQ Suffix
Plastic Package

Weight \approx 0.911 gram

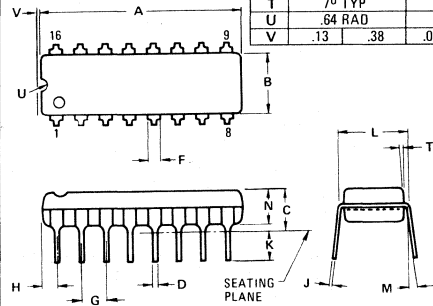


CASE 648

Weight \approx 0.93 gram

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| A | 20.70 | 21.21 | .815 | .835 |
| B | 6.09 | 6.60 | .240 | .260 |
| C | 4.07 | 4.57 | .160 | .180 |
| D | .38 | .51 | .015 | .020 |
| F | 1.14 | 1.40 | .045 | .055 |
| G | 2.54 BSC | | .100 BSC | |
| H | 1.32 | 1.83 | .052 | .072 |
| J | .20 | .30 | .008 | .012 |
| K | 2.92 | 3.43 | .115 | .135 |
| L | 7.37 | 7.87 | .290 | .310 |
| M | - | 10° | - | 10° |
| N | .64 | .89 | .025 | .035 |
| T | 7° TYP | | 7° TYP | |
| U | .64 RAD | | .025 RAD | |
| V | .13 | .38 | .005 | .015 |

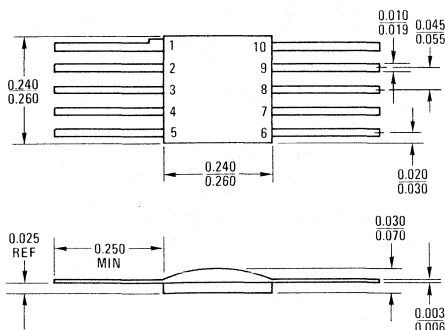
NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.



CASE 665

F Suffix
Ceramic Package

Weight \approx 0.188 gram

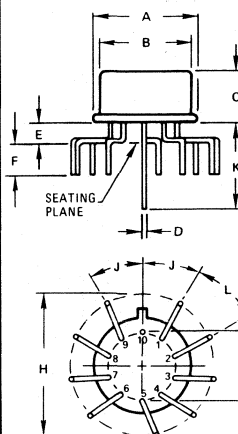


CASE 686

G Suffix
Metal Package

Weight \approx 0.918 gram

| DIM | INCHES | | MILLIMETERS | |
|-----|----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.335 | 0.370 | 8.51 | 9.40 |
| B | 0.305 | 0.335 | 7.75 | 8.51 |
| C | - | 0.180 | - | 4.57 |
| D | 0.016 | 0.019 | 0.406 | 0.483 |
| E | 0.070 | 0.100 | 1.78 | 2.54 |
| F | 0.120 | 0.150 | 3.05 | 3.81 |
| G | 0.230 TP | | 5.84 TP | |
| H | 0.480 TP | | 12.19 TP | |
| J | 31° TP | | 31° TP | |
| K | 0.235 | 0.265 | 5.97 | 6.73 |
| L | 34° TP | | 34° TP | |



*Seven places; (between all leads except 5 & 6, 9 & 10, 10 & 1)

APPLICATION NOTE ABSTRACTS

The application notes listed in this section have been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications. To obtain copies of the notes, simply list the AN number or numbers and send your request on your company letterhead to: Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

AN-204A The MC1530, MC1531 Integrated Operational Amplifiers

Two monolithic operational amplifiers feature exceptionally high input impedance and high open loop gain. This note describes the function of each stage in the circuit, methods of frequency compensating and dc biasing. Four applications are discussed: a summing circuit, an integrator, a dc comparator, and transfer function simulation.

AN-245A An Integrated Sense Amplifier for Core Memories

This application note discusses core memories and related design considerations for a sense amplifier. Performance and environmental specifications for the amplifier design are carefully established so that the circuit will work with any computer using core memories. The final circuit design is then analyzed and measured performance is discussed. The amplifier features a small uncertainty region (6 mV max.), adjustable threshold and fast cycle time (0.5 μ s).

AN-247 An Integrated Circuit RF-IF Amplifier

A new, versatile integrated circuit for RF-IF applications is introduced which offers high gain, extremely low internal feedback and wide AGC range. The circuit is a common-emitter, common-base pair (the cascade connection) with an AGC transistor and associated biasing circuitry. The amplifier is built on a very small die and is economically comparable to a single transistor, yet it offers performance advantages unobtainable with a single device. This application note describes the AC and DC operation of the circuit, a discussion of Y-parameters for calculating optimum power and voltage gain, and a variety of applications as an IF single-tuned amplifier, IF stagger-tuned amplifier, oscillator, video-audio amplifier and modulator. A discussion of noise figure is also included.

AN-248 A High Voltage Monolithic Operational Amplifier

This note introduces a high voltage monolithic operational amplifier featuring high open loop gain,

large common mode input signal, and low drift. The function of each stage in the circuit is analyzed, and methods for frequency compensating the amplifier are discussed. DC biasing parameters are also examined. Four applications using the amplifier are discussed: a source follower, a twin tee filter and oscillator, a voltage regulator, and a high input impedance voltmeter.

AN261A Transistor Logarithmic Conversion Using An Integrated Operational Amplifier

The design of a log amplifier using a common base transistor configuration as the feedback element of an integrated circuit operational amplifier circuit is discussed in this application note. Five decades of logarithmic conversion are obtained with less than 1% error of output voltage. The MC1556 op amp proves superior in this application due to its very low bias current. A design using the MC1539 op amp is also discussed.

AN-273A Getting More Value Out of An Integrated Operational Amplifier Data Sheet

The operational amplifier has become a basic building block in present day solid state electronic systems. The purpose of this application note is to provide a better understanding of the open loop characteristics of the amplifier and their significance to overall circuit operation. Also each parameter is defined and reviewed with respect to closed loop considerations. The importance of loop gain stability and bandwidth is discussed at length. Input offset voltage and current and resultant drift effects in the circuit are also reviewed with respect to closed loop operation.

AN-299 An IC Wideband Video Amplifier With AGC

This application describes the use of the MC1550 as a wideband video amplifier with AGC. The analysis of a single stage amplifier with 28 dB of gain and 22 MHz bandwidth is given with the results extended to a 78 dB video amplifier with 10 MHz bandwidth.

APPLICATION NOTE ABSTRACTS (continued)

AN-400 An Operational Amplifier Tester

A simple and inexpensive tester for Motorola's line of operational amplifiers is described which will measure the open loop voltage gain, the equivalent input offset voltage, the maximum positive and negative output voltage swing, and a view of the transfer function which shows the linearity of the device.

Included is an elementary discussion of the parameters measured and their relationship to closed loop performance.

AN-401 The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier

This application note discusses four different applications for the MC1554, along with a circuit description including dc characteristics, frequency response, and distortion. A section of the note is also devoted to package power dissipation calculations including the use of the curves on the power amplifier data sheet.

AN-403 Single Power Supply Operation of IC Op Amps

A split zener biasing technique that permits use of the MC1530/1531, MC1533, and MC1709 operational amplifiers and their restricted temperature counterparts MC1430/1431, MC1433 and MC1709C from a single power supply voltage is discussed in detail. General circuit considerations as well as specific ac and dc device considerations are outlined to minimize operating and design problems.

AN-404 A Wideband Monolithic Video Amplifier

This note describes the basic principles of ac and dc operation of the MC1552G and MC1553G, characteristics obtained as a function of the device operating modes, and typical circuit applications.

AN-405 DC Comparator Operations Utilizing Monolithic IC Amplifiers

The use of the MC1533 operational amplifier and the MC1710 differential comparator are discussed. The capabilities and performance are given along with typical operating curves for both devices.

AN-407 A General Purpose IC Differential Output Operational Amplifier

This application note discusses four different applications for the MC1520 and a complete descrip-

tion of the device itself. The final sections of the note discuss such topics as operation from single and split power supplies, frequency compensation, and various feedback schemes.

AN-411 The MC1535 Monolithic Dual Op Amp

This note discusses two dual operational amplifier applications and an input compensation scheme for fast slew rate for the MC1535. A complete ac and dc circuit analysis is presented in addition to many of the pertinent electrical characteristics and how they might affect the system performance.

AN-421 Semiconductor Noise Figure Considerations

A summary of many of the important noise figure considerations related with the design of low noise amplifiers is presented. The basic fundamentals involving noise, noise figure, and noise figure-frequency characteristics are then discussed with the emphasis on characteristics common to all semiconductors. A brief introduction is made to various methods of data sheet presentation of noise figure and a summary is given for the various methods of measurement. A discussion of low noise circuit design, utilizing many of the previously discussed considerations, is included.

AN-432B Integrated Circuit FM Stereo Decoding

Present day monolithic stereo demodulators in addition to decoding the audio information, provide many auxiliary functions. This note describes the basic demodulator and several interesting accessory capabilities available on the MC1304, MC1305, and MC1307.

AN-439 MC1539 Op Amp and its Applications

This application note discusses the MC1539, a second generation operational amplifier. The general use and operation of the amplifier is discussed with special mention made of improved operation over that of its first generation predecessor—the 709 type amplifier.

In addition to the detailed discussion on the dc and ac operation of the device, considerable emphasis is placed on operational performance. Many applications are offered to demonstrate the device capability, including a high frequency feed-forward scheme, and a source follower application.

APPLICATION NOTE ABSTRACTS (continued)

AN-459 A Simple Technique for Extending Op Amp Power Bandwidth

The design of fast response amplifiers is presented without the use of "tricky" compensation procedures or calculations using data sheet information. Circuit analysis for compensation procedure is given.

AN-460 Using Transient Response to Determine Operational Amplifier Stability

This application note describes a technique for evaluating the stability of any particular feedback amplifier configuration by analyzing its response to a step-function input. A theoretical analysis is given along with an example.

AN-471 Analog-To-Digital Conversion Techniques

The subject of analog-to-digital conversion and many of the techniques that can be used to accomplish it are discussed. The paper is written in general terms, from a system point of view, and is intended to assist the reader in determining which conversion technique is best suited for a given application.

AN-473 The MC1561 – A Monolithic High Power Series Voltage Regulator

A complete series voltage regulator circuit capable of delivering 1/2 ampere of current has been built on a single 63 x 66-mil die using the conventional all-diffused processing technology. Improved performance has been achieved by using an internal low-power voltage regulator to supply the desired dc output voltage reference directly to a second main regulator. This permits the dc and ac characteristics of the regulator to be separately optimized with the result that excellent transient characteristics are realized simultaneously with low drift and excellent regulation.

AN-474 The MC1541 – A Gated Dual-Channel Sense Amplifier for Core Memories

The MC1541 sense amplifier can provide many magnetic core memory systems with lower system cycle times and a lower package count than previous sense amplifiers. The MC1541 circuit operation, design considerations, interface problems, and typical applications are herein discussed.

AN-475 Using the MC1545 – A Monolithic, Gated-Video Amplifier

Because of the unique design of the MC1545, this amplifier can be used as a gated video amplifier, sense amplifier, amplitude modulator, frequency shift keyer, balanced modulator, pulse amplifier, and many other applications. This note describes the ac and dc operation of the circuit and presents applications of the device as a video switch, amplitude modulator, balanced modulator, pulse amplifier, and others.

AN-480 Regulators Using Operational Amplifiers

The theory of op amp voltage regulator design is discussed. The problem areas associated with such designs are also detailed. The MC1560 is used as a OTC voltage reference in the op amp regulator designs that are shown. It is shown that regulation from 0.01% to 0.001% is possible.

AN-489 Analysis and Basic Operation of the MC1595

The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given along with performance that is characteristic of the device. A few basic applications are given to assist the designer in system design.

AN-491 Gated Video Amplifier Applications The MC1545

This application note reviews the basic operation of the MC1545 and discusses some of the more popular applications for the MC1545. Included are several modulator types, temperature compensation of the active gate, AGC, gated oscillators, FSK systems, and single supply operation.

AN-513 A High Gain Integrated Circuit RF-IF Amplifier With Wide Range AGC

This note describes the operation and application of the MC1590G, a monolithic RF-IF amplifier. Included are several applications for IF amplifiers, a mixer, video amplifiers, single and two-stage RF amplifiers.

AN-522 The MC1556 Operational Amplifier and its Applications

This application note discusses the MC1556, a second generation, internally compensated monolithic operational amplifier. Particular emphasis is placed

APPLICATION NOTE ABSTRACTS (continued)

on its distinct advantages over the early 709-type amplifier and the more recent 741-type amplifier.

Along with a description of its operation this note presents a discussion on various applications of the MC1556, highlighting its capabilities, and points out its characteristics so the reader may make effective use of the device.

AN-531 MC1596 Balanced Modulator

The MC1596 monolithic circuit is a highly versatile communications building block. In this note, both theoretical and practical information are given to aid the designer in the use of this part. Applications include modulators for AM, SSB, and suppressed carrier AM; demodulators for the previously mentioned modulation forms; frequency doublers and HF/VHF double balanced mixers.

AN-533 Semiconductor for Plated-Wire Memories

An introduction to the operation and electrical characteristics of plated-wire memories is provided in conjunction with the applications of semiconductors that interface with the plated-wire memories.

Devices discussed include drivers, sense amplifiers, and decoders. Memory organization and memory-related semiconductor applications are also mentioned.

AN-543 Integrated Circuit IF Amplifiers For AM/FM and FM Radios

This application note discusses the design and performance of four IF amplifiers using integrated circuits. The IF amplifiers discussed include a high performance circuit, a circuit utilizing a quadrature detector, a composite AM/FM circuit, and an economy model for use with an external discriminator.

AN-545 Television Video IF Amplifier Using Integrated Circuits

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, MC1353 and the MC1330.

AN-547 The MC1514 – A High Speed Dual Differential Comparator

This application note discusses a few of the many uses for the MC1514 dual comparator. Many applications such as sense amplifiers, multivibrators, peak level detectors are presented.

AN-557 Analog-to-Digital Cyclic Converter

The A/D cyclic converter discussed in this note provides medium speed (1.5 μ s/bit) and medium accuracy (7 or 8 bits) operation. A cyclic converter uses the successive approximation technique in which an unknown analog input voltage is successively compared to a reference voltage to determine each bit of the digital output.

The cyclic converter offers continuous operation, automatic generation of the digital output in Gray-code form, and a building block structure. This structure uses a separate but identical circuit for each resolution bit. The cyclic converter finds use primarily in control and process applications.

AN-559 A Single Ramp Analog-to-Digital Converter

A simple single ramp A/D converter which incorporates a calibration cycle to insure an accuracy of 12 bits is discussed. The circuit uses standard ICs and requires only one precision part – the reference voltage used in the calibration. This converter is useful in a number of instrumentation and measurement applications.

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